Preliminary *4M X 4 CMOS DYNAMIC RAM WITH EDO PAGE MODE*

Document Title

4M X 4 CMOS DYNAMIC RAM WITH EDO PAGE MODE

Revision History

Rev. No.	History	Issue Date	Remark
0.0	Initial issue	June 13, 2001	Preliminary

Preliminary — 4M X 4 CMOS DYNAMIC RAM WITH EDO PAGE MODE

Features

- Organization: 4,194,304 words X 4 bits
- Part Identification
  - A42U2604 (2K Ref.)
- Single 2.5V power supply/built-in VBB generator
- Low power consumption
  - Operating: 120mA (-50 max)
  - Standby: 1mA (TTL), 0.2mA (CMOS), 250µA (Self-refresh current)
- High speed
  - 50/60/80 ns $\overline{RAS}$ access time
  - 25/30/40 ns column address access time
  - 13/15/20 ns $\overline{CAS}$ access time
  - 20/25/35 ns EDO Page Mode Cycle Time
- Fast Page Mode with Extended Data Out
- Read-modify-write, $\overline{RAS}$ -only, $\overline{CAS}$ -before- $\overline{RAS}$, Hidden refresh capability
- TTL-compatible, three-state I/O
- JEDEC standard packages
  - 300mil, 24/26-pin SOJ
  - 300mil, 24/26-pin TSOP type II package

General Description

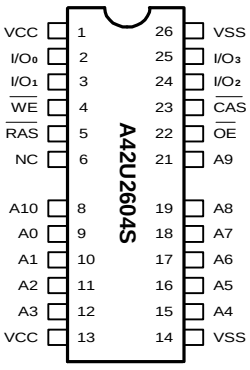
The A42U2604 is a new generation randomly accessed memory for graphics, organized in a 4,194,304-word by 4-bit configuration. This product can execute Write and Read operation via $\overline{CAS}$ pin.

The A42U2604 offers an accelerated Fast Page Mode cycle with a feature called Extended Data Out (EDO).

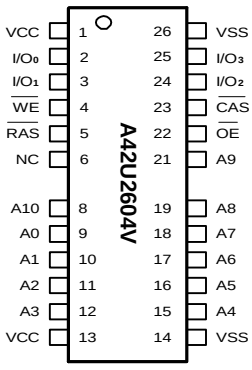
This allow random access of up to 2048(2K Ref.) words within a row at a 50/40/28 MHz EDO cycle, making the A42U2604 ideally suited for graphics, digital signal processing and high performance computing systems.

Pin Configuration

■ **SOJ**



■ **TSOP**



Pin Descriptions

Symbol	Description
A0 - A10	Address Inputs (2K product)
I/O0 - I/O3	Data Input/Output
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
VCC	2.5V Power Supply
VSS	Ground
NC	No Connection

Selection Guide

Symbol	Description	-50	-60	-80	Unit
t_{RAC}	Maximum $\overline{RAS}$ Access Time	50	60	80	ns
t_{AA}	Maximum Column Address Access Time	25	30	40	ns
t_{CAC}	Maximum $\overline{CAS}$ Access Time	13	15	20	ns
t_{OEA}	Maximum Output Enable ($\overline{OE}$) Access Time	13	15	20	ns
t_{RC}	Minimum Read or Write Cycle Time	84	104	134	ns
t_{PC}	Minimum EDO Cycle Time	20	25	35	ns

Functional Description

The A42U2604 reads and writes data by multiplexing an 22-bit address into a 11-bit(2K) row and column address. $\overline{RAS}$ and $\overline{CAS}$ are used to strobe the row address and the column address, respectively.

A Read cycle is performed by holding the $\overline{WE}$ signal high during $\overline{RAS}$/$\overline{CAS}$ operation. A Write cycle is executed by holding the $\overline{WE}$ signal low during $\overline{RAS}$/$\overline{CAS}$ operation; the input data is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs later. The data inputs and outputs are routed through 4 common I/O pins, with $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and $\overline{OE}$ controlling the in direction.

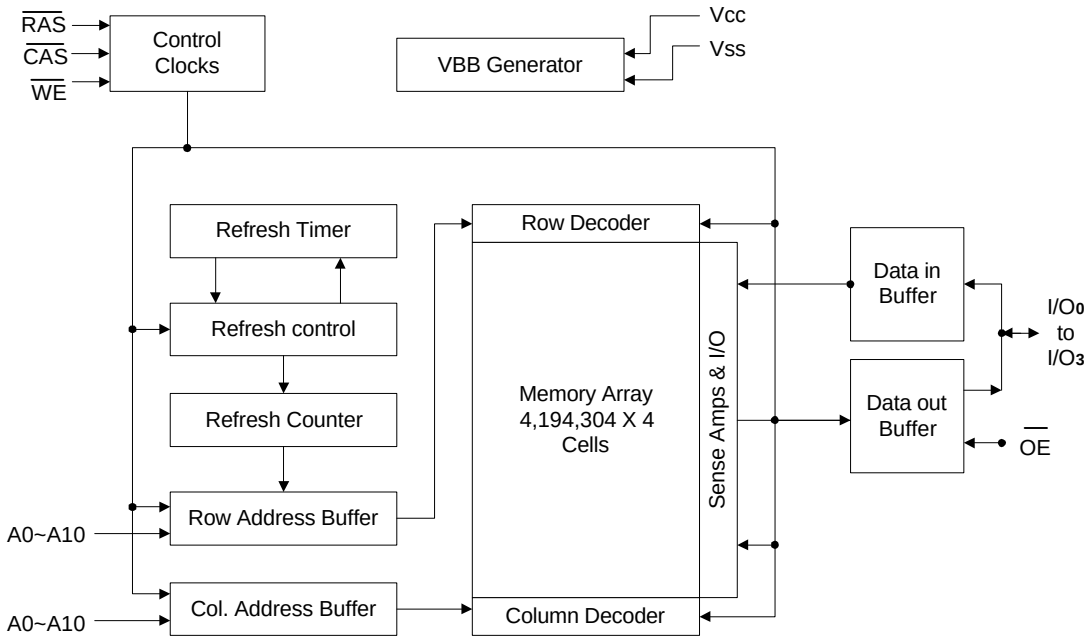
EDO Page Mode operation all 2048(2K) columns within a selected row to be randomly accessed at a high data rate. A EDO Page Mode cycle is initiated with a row address latched by $\overline{RAS}$ followed by a column address latched by $\overline{CAS}$. While holding $\overline{RAS}$ low, $\overline{CAS}$ can be toggled to strobe changing column addresses, thus achieving shorter cycle times.
The A42U2604 offers an accelerated Fast Page Mode cycle through a feature called Extended Data Out, which keeps the output drivers on during the $\overline{CAS}$ precharge time (t_{cp}). Since data can be output after $\overline{CAS}$ goes high, the user is not required to wait for valid data to appear before starting the next access cycle. Data-out will remain valid as long as $\overline{RAS}$ and $\overline{OE}$ are low, and $\overline{WE}$ is high; this is the only characteristic which differentiates Extended Data Out operation from a standard Read or Fast Page Read.

A memory cycle is terminated by returning both $\overline{RAS}$ and $\overline{CAS}$ high. Memory cell data will retain its correct state by maintaining power and accessing all 2048(2K) combinations of the 11-bit(2K) row addresses, regardless of sequence, at least once every 32ms through any $\overline{RAS}$ cycle (Read, Write) or $\overline{RAS}$ Refresh cycle ($\overline{RAS}$-only, CBR, or Hidden). The CBR Refresh cycle automatically controls the row addresses by invoking the refresh counter and controller.

Power-On

The initial application of the VCC supply requires a 200 µs wait followed by a minimum of any eight initialization cycles containing a $\overline{RAS}$ clock. During Power-On, the VCC current is dependent on the input levels of $\overline{RAS}$ and $\overline{CAS}$. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with VCC or be held at a valid V_{IH} during Power-On to avoid current surges.

Block Diagram



Recommended Operating Conditions (Ta = 0°C to +70°C)

Symbol	Description	Min.	Typ.	Max.	Unit
VCC	Power Supply	2.25	2.5	2.75	V
VSS	Input High Voltage	0	0	0	V
V_{IH}	Input High Voltage	1.8	-	VCC + 0.2	V
V_{IL}	Input Low Voltage	-1.0	-	0.8	V

Truth Table

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	Address	I/Os
Standby	H	H	X	X	X	High-Z
Read: Word	L	L	H	L	Row/Col.	Data Out
Read	L	L	H	L	Row/Col.	Data Out
Write: Word (Early)	L	L	L	X	Row/Col.	Data In
Write (Early)	L	L	L	X	Row/Col.	Data In
Read-Write	L	L	H→L	L→H	Row/Col.	Data Out → Data In
EDO-Page-Mode Read: Hi-Z						
-First cycle	L	H→L	H	H→L	Row/Col.	Data Out
-Subsequent Cycles	L	H→L	H	H→L	Col.	Data Out
EDO-Page-Mode Write(Early)						
-First cycle	L	H→L	L	X	Row/Col.	Data In
-Subsequent Cycles	L	H→L	L	X	Col.	Data In
EDO-Page-Mode Read-Write						
-First cycle	L	H→L	H→L	L→H	Row/Col.	Data Out → Data In
-Subsequent Cycles	L	H→L	H→L	L→H	Col.	Data Out → Data In
Hidden Refresh Read	L→H→L	L	H	L	Row/Col.	Data Out
Hidden Refresh Write	L→H→L	L	L	X	Row/Col.	Data In → High-Z
$\overline{RAS}$-Only Refresh	L	H	X	X	Row	High-Z
CBR Refresh	H→L	L	X	X	X	High-Z
Self Refresh	H→L	L	H	X	X	High-Z

Absolute Maximum Ratings*

Input Voltage (Vin) . . . . . -0.5V to VCC+0.5V
Output Voltage (Vout) . . . . . -0.5V to VCC+0.5V
Power Supply Voltage (VCC) . . . . . -0.5V to VCC+0.5V
Operating Temperature (T_{OPR}) . . . . . 0°C to +70°C
Storage Temperature (T_{STG}) . . . . . -55°C to +150°C
Soldering Temperature X Time (T_{SOLDER}) . . . . . 260°C X 10sec
Power Dissipation (P_D) 1W
Short Circuit Output Current (Iout) 50mA
Latch-up Current 200mA

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of these specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (VCC = 2.5V ± 10%, VSS = 0V, Ta = 0°C to +70°C)

Symbol	Parameter	-50		-60		-80		Unit	Test Conditions	Notes
		Min.	Max.	Min.	Max.	Min.	Max.			
I_{IL}	Input Leakage Current	-5	+5	-5	+5	-5	+5	µA	0V ≤ Vin ≤ Vin + 0.2V Pins not under Test = 0V	
I_{OL}	Output Leakage Current	-5	+5	-5	+5	-5	+5	µA	D_{OUT} disabled, 0V ≤ Vout ≤ + VCC	
I_{CC1}	Operating Power Supply Current	-	120	-	110	-	100	mA	$\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$ Address cycling; t_{RC} = min.	1, 2
I_{CC2}	TTL Standby Power Supply Current	-	1	-	1	-	1	mA	$\overline{RAS}$ = $\overline{UCAS}$ = $\overline{LCAS}$ = V_{IH}	
I_{CC3}	Average Power Supply Current, $\overline{RAS}$ Refresh Mode	-	120	-	110	-	100	mA	$\overline{RAS}$ cycling, $\overline{UCAS}$ = $\overline{LCAS}$ = V_{IH}, t_{RC} = min.	1
I_{CC4}	EDO Page Mode Average Power Supply Current	-	100	-	90	-	80	mA	$\overline{RAS}$ = V_{IL}, $\overline{UCAS}$, $\overline{LCAS}$ Address cycling; t_{PC} = min.	1, 2
I_{CC5}	$\overline{CAS}$-before-$\overline{RAS}$ Refresh Power Supply Current	-	110	-	100	-	90	mA	$\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$ cycling; t_{RC} = min.	1
I_{CC6}	CMOS Standby Power Supply Current	-	0.2	-	0.2	-	0.2	mA	$\overline{RAS}$ = $\overline{UCAS}$ = $\overline{LCAS}$ = VCC - 0.2V	
I_{CC7}	Self Refresh Mode Current	-	250	-	250	-	250	µA	$\overline{RAS}$ = $\overline{CAS}$ ≤ VSS+0.2V All other input high levels are VCC-0.2V or input low levels are VSS +0.2V	
V_{OH}	Output Voltage	2.0	-	2.0	-	2.0	-	V	I_{OUT} = -2mA	
V_{OL}		-	0.4	-	0.4	-	0.4	V	I_{OUT} = 2mA	

AC Characteristics (VCC = 2.5V ±10%, VSS = 0V, Ta = 0°C to +70°C)

Test Conditions:

Input timing reference level: V_{IH}/V_{IL}=1.8V/0.8V
Output reference level: V_{OH}/V_{OL}=1.6V/0.8V
Output Load: 1TTL gate + CL (100pF)
Assumed t_T=2ns

#	Std Symbol	Parameter		-50		-60		-80		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.		
	t_T	Transition Time (Rise and Fall)		1	50	1	50	1	50	ns	4, 5
	t_{REF}	Refresh Period	2K	-	32	-	32	-	32	ms	3
			Self-REF	-	128	-	128	-	128	ms	3
1	t_{RC}	Random Read or Write Cycle Time		84	-	104	-	134	-	ns	
2	t_{RP}	$\overline{RAS}$ Precharge Time		30	-	40	-	50	-	ns	
3	t_{RAS}	$\overline{RAS}$ Pulse Width		50	10K	60	10K	80	10K	ns	
4	t_{CAS}	$\overline{CAS}$ Pulse Width		7	10K	10	10K	15	10K	ns	
5	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time		11	37	14	45	20	60	ns	6
6	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time		9	25	12	30	15	40	ns	7
7	t_{RSH}	$\overline{CAS}$ to $\overline{RAS}$ Hold Time		7	-	10	-	10	-	ns	
8	t_{CSH}	$\overline{CAS}$ Hold Time		37	-	40	-	50	-	ns	
9	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time		5	-	5	-	5	-	ns	
10	t_{ASR}	Row Address Setup Time		0	-	0	-	0	-	ns	
11	t_{RAH}	Row Address Hold Time		7	-	10	-	10	-	ns	
12	t_{CLZ}	$\overline{CAS}$ to Output in Low Z		0	-	0	-	0	-	ns	8
13	t_{RAC}	Access Time from $\overline{RAS}$		-	50	-	60	-	80	ns	6,7
14	t_{CAC}	Access Time from $\overline{CAS}$		-	13	-	15	-	20	ns	6, 12
15	t_{AA}	Access Time from Column Address		-	25	-	30	-	40	ns	7, 12
16	t_{AR}	Column Address Hold Time from $\overline{RAS}$		44	-	55	-	70	-	ns	
17	t_{RCS}	Read Command Setup Time		0	-	0	-	0	-	ns	
18	t_{RCH}	Read Command Hold Time		0	-	0	-	0	-	ns	9

AC Characteristics (continued) (VCC = 2.5V ±10%, VSS = 0V, Ta = 0°C to +70°C)

Test Conditions:

Input timing reference level: V_{IH}/V_{IL}=1.8V/0.8V
Output reference level: V_{OH}/V_{OL}=1.6V/0.8V
Output Load: 1TTL gate + CL (100pF)
Assumed t_T=2ns

#	Std Symbol	Parameter	-50		-60		-80		Unit	Notes
			Min.	Max.	Min.	Max.	Min.	Max.		
19	t_{RRH}	Read Command Hold Time Reference to $\overline{RAS}$	0	-	0	-	0	-	ns	9
20	t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	25	-	30	-	40	-	ns	
21	t_{COH}	Output Hold After $\overline{CAS}$ Low	5	-	5	-	3	-	ns	
22	t_{ODS}	Output Disable Setup Time	0	-	0	-	0	-	ns	
23	t_{OFF}	Output Buffer Turn-Off Delay Time	0	13	0	15	0	20	ns	8, 10
24	t_{ASC}	Column Address Setup Time	0	-	0	-	0	-	ns	
25	t_{CAH}	Column Address Hold Time	7	-	10	-	10	-	ns	
26	t_{OES}	$\overline{OE}$ Low to $\overline{CAS}$ High Set Up	5	-	5	-	10	-	ns	
27	t_{WCS}	Write Command Setup Time	0	-	0	-	0	-	ns	11
28	t_{WCH}	Write Command Hold Time	7	-	10	-	10	-	ns	11
29	t_{WCR}	Write Command Hold Time to $\overline{RAS}$	44	-	55	-	70	-	ns	
30	t_{WP}	Write Command Pulse Width	7	-	10	-	10	-	ns	
31	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	13	-	15	-	20	-	ns	
32	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	7	-	10	-	10	-	ns	
33	t_{DS}	Data-in setup Time	0	-	0	-	0	-	ns	
34	t_{DH}	Data-in Hold Time	7	-	10	-	15	-	ns	
35	t_{DHR}	Data-in Hold Time to $\overline{RAS}$	44	-	55	-	70	-	ns	
36	t_{RWC}	Read-Modify-Write Cycle Time	110	-	135	-	180	-	ns	
37	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time (Read-Modify-Write)	67	-	79	-	107	-	ns	11
38	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time (Read-Modify-Write)	30	-	34	-	47	-	ns	11

AC Characteristics (continued) (VCC = 2.5V ± 10%, VSS = 0V, Ta = 0°C to +70°C)

Test Conditions:

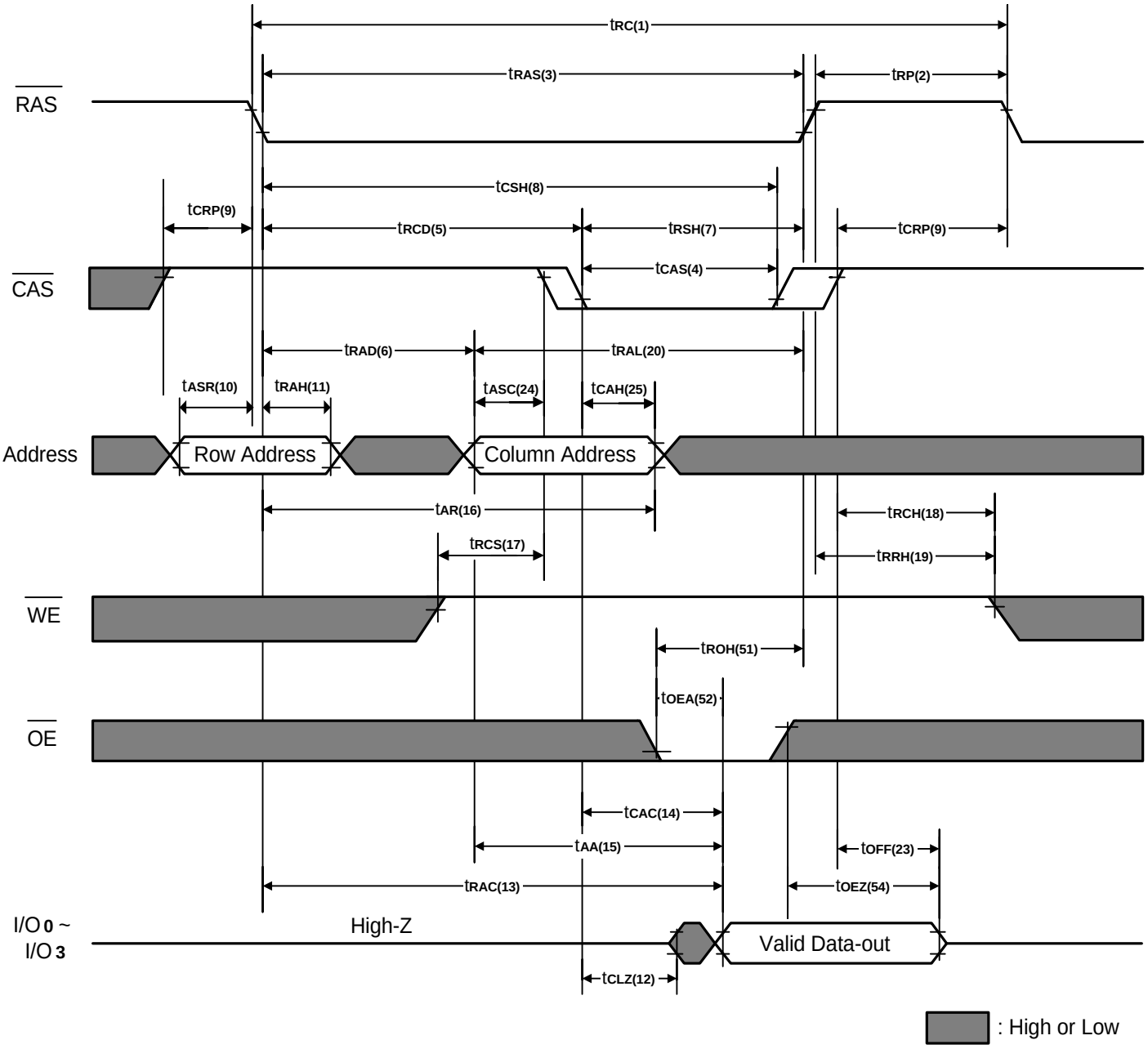
Input timing reference level: V_{IH}/V_{IL}=1.8V/0.8V
Output reference level: V_{OH}/V_{OL}=1.6V/0.8V
Output Load: 1TTL gate + CL (100pF)
Assumed t_T=2ns

#	Std Symbol	Parameter	-50		-60		-80		Unit	Notes
			Min.	Max.	Min.	Max.	Min.	Max.		
39	t_{AWD}	Column Address to $\overline{WE}$ Delay Time (Read-Modify-Write)	42	-	49	-	67	-	ns	11
40	t_{OEH}	$\overline{OE}$ Hold Time from $\overline{WE}$	7	-	10	-	20	-	ns	
41	t_{OEP}	$\overline{OE}$ High Pulse Width	2	-	2	-	5	-	ns	
42	t_{PC}	Read or Write Cycle Time (EDO Page)	20	-	25	-	35	-	ns	13
43	t_{CPA}	Access Time from $\overline{CAS}$ Precharge (EDO Page)	-	28	-	33	-	45	ns	12
44	t_{CP}	$\overline{CAS}$ Precharge Time (EDO Page)	7	-	10	-	10	-	ns	
45	t_{PCM}	EDO Page Mode RMW Cycle Time	58	-	68	-	80	-	ns	
46	t_{CRW}	EDO Page Mode $\overline{CAS}$ Pulse Width (RMW)	34	-	38	-	42	-	ns	
47	t_{RASP}	$\overline{RAS}$ Pulse Width (EDO Page)	50	100K	60	100K	80	100K	ns	
48	t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$-before-$\overline{RAS}$)	5	-	5	-	5	-	ns	3
49	t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$-before-$\overline{RAS}$)	10	-	10	-	15	-	ns	3
50	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time ($\overline{CAS}$-before-$\overline{RAS}$)	5	-	5	-	5	-	ns	
51	t_{ROH}	$\overline{RAS}$ Hold Time Reference to $\overline{OE}$	5	-	5	-	5	-	ns	
52	t_{OEA}	$\overline{OE}$ Access Time	-	13	-	15	-	20	ns	
53	t_{OED}	$\overline{OE}$ to Data Delay	13	-	15	-	20	-	ns	
54	t_{OEZ}	Output Buffer Turn-off Delay from $\overline{OE}$	0	13	0	15	0	20	ns	8
55	t_{RASS}	$\overline{RAS}$ pulse width ($\overline{C}$-B-$\overline{R}$ self-refresh)	100	-	100	-	100	-	µs	
56	t_{RPS}	$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self-refresh)	84	-	104	-	134	-	ns	
57	t_{CHS}	$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self-refresh)	-	50	-	50	-	50	ns	

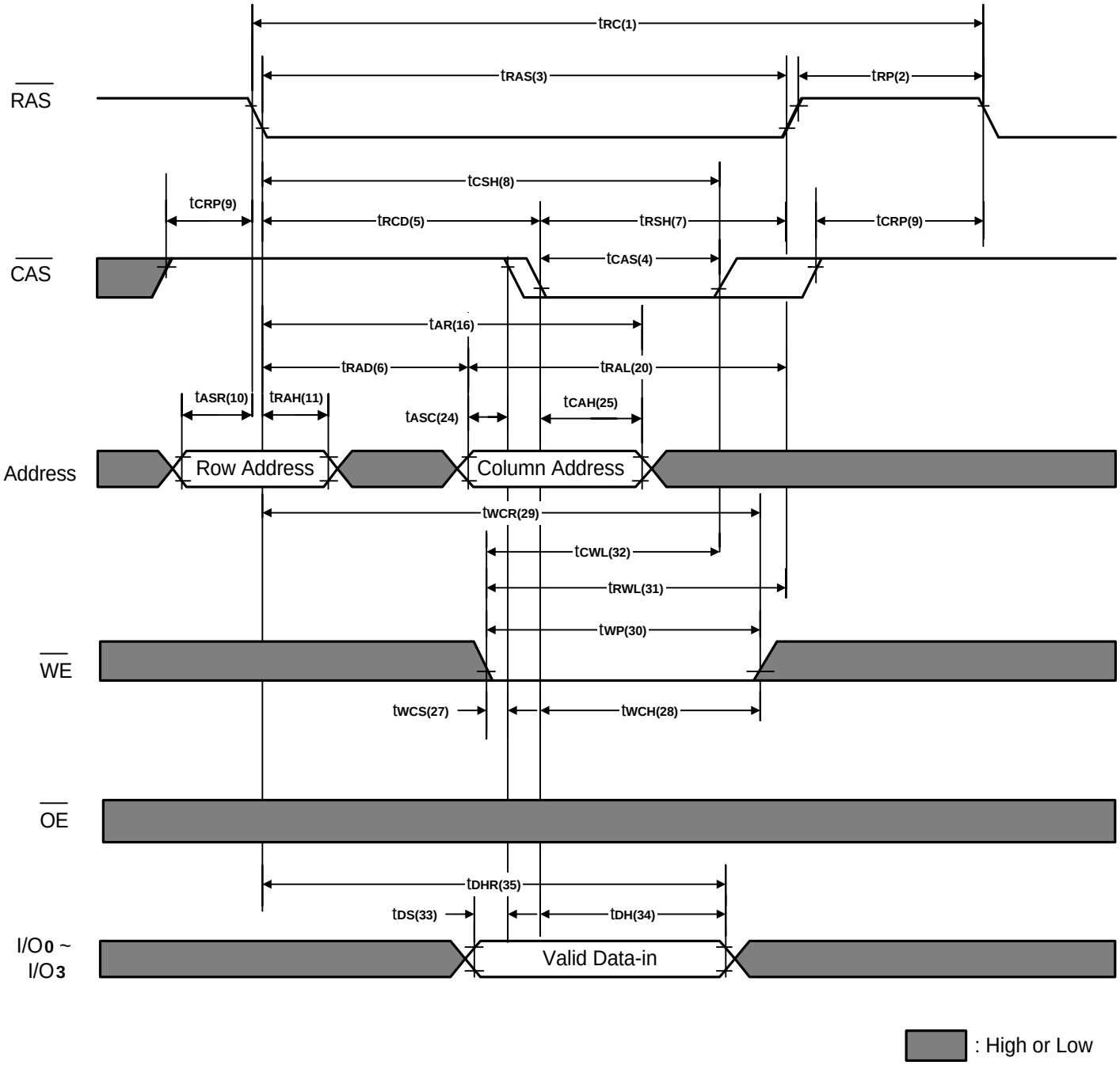
Notes:

1. I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on cycle rate.
2. I_{CC1} and I_{CC4} depend on output loading. Specified values are obtained with the outputs open.
3. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved. In the case of an internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required. 8 initialization cycles are required after extended periods of bias without.
4. AC Characteristics assume t_T = 2ns. All AC parameters are measured with a load equivalent to one TTL load and 100pF, V_{IL} (min.) ≥ GND and V_{IH} (max.) ≤ VCC.
5. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.
7. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled exclusively by t_{AA}.
8. Assumes three state test load (5pF and a 500Ω Thevenin equivalent).
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. t_{OFF} (max.) defines the time at which the output achieves the open circuit condition; it is not referenced to output voltage levels.
11. t_{WCS}, t_{WCH}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If t_{WCS} ≥ t_{WCS} (min.) and t_{WCH} ≥ t_{WCH} (min.), the cycle is an early write cycle and data-out pins will remain open circuit, high impedance, throughout the entire cycle. If t_{RWD} ≥ t_{RWD} (min.) , t_{CWD} ≥ t_{CWD} (min.) and t_{AWD} ≥ t_{AWD} (min.), the cycle is a read-modify-write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is satisfied, the condition of the data out at access time is indeterminate.
12. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{CPA}.
13. t_{ASC} ≥ t_{CP} to achieve t_{PC} (min.) and t_{CPA} (max.) values.

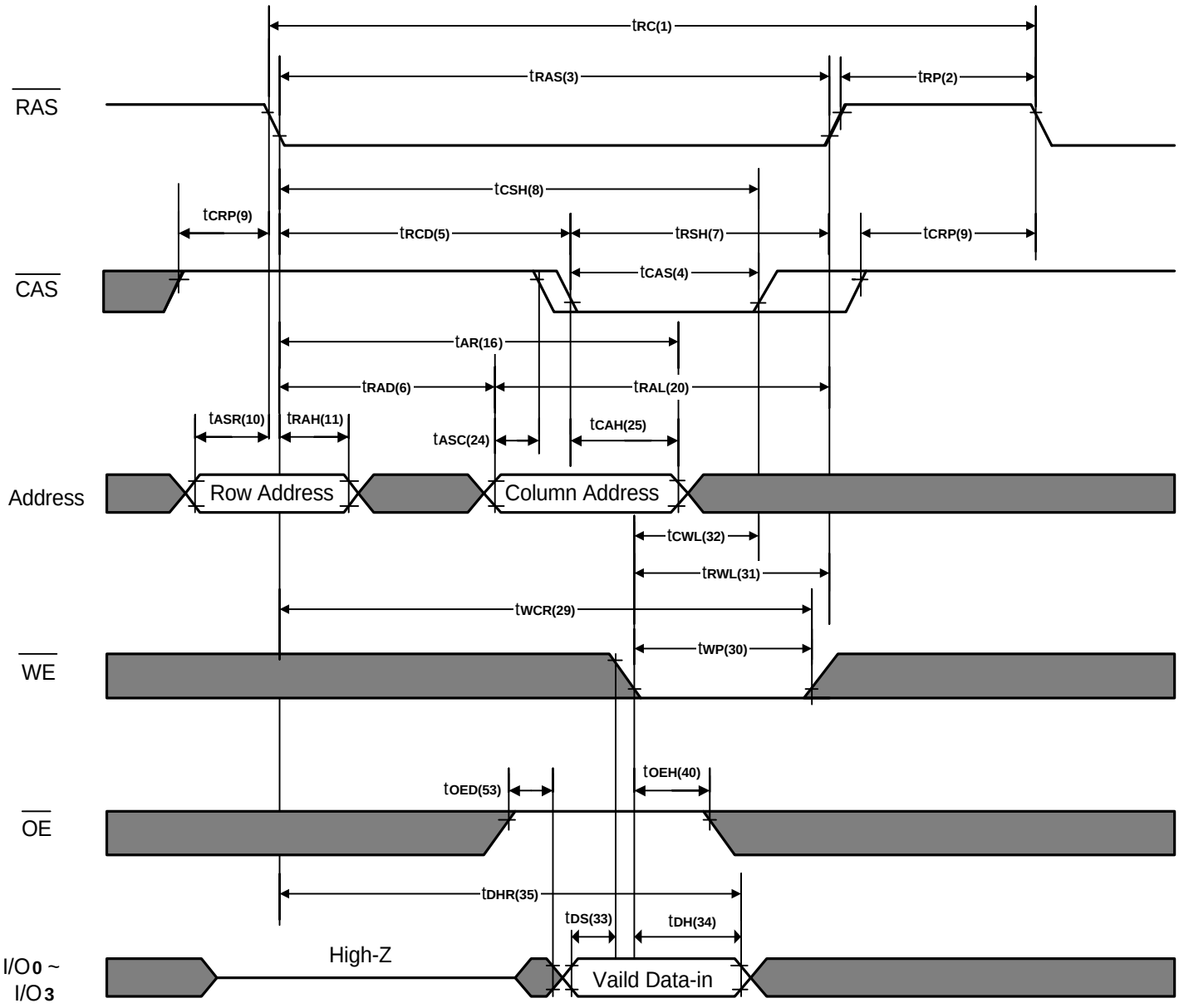
Word Read Cycle



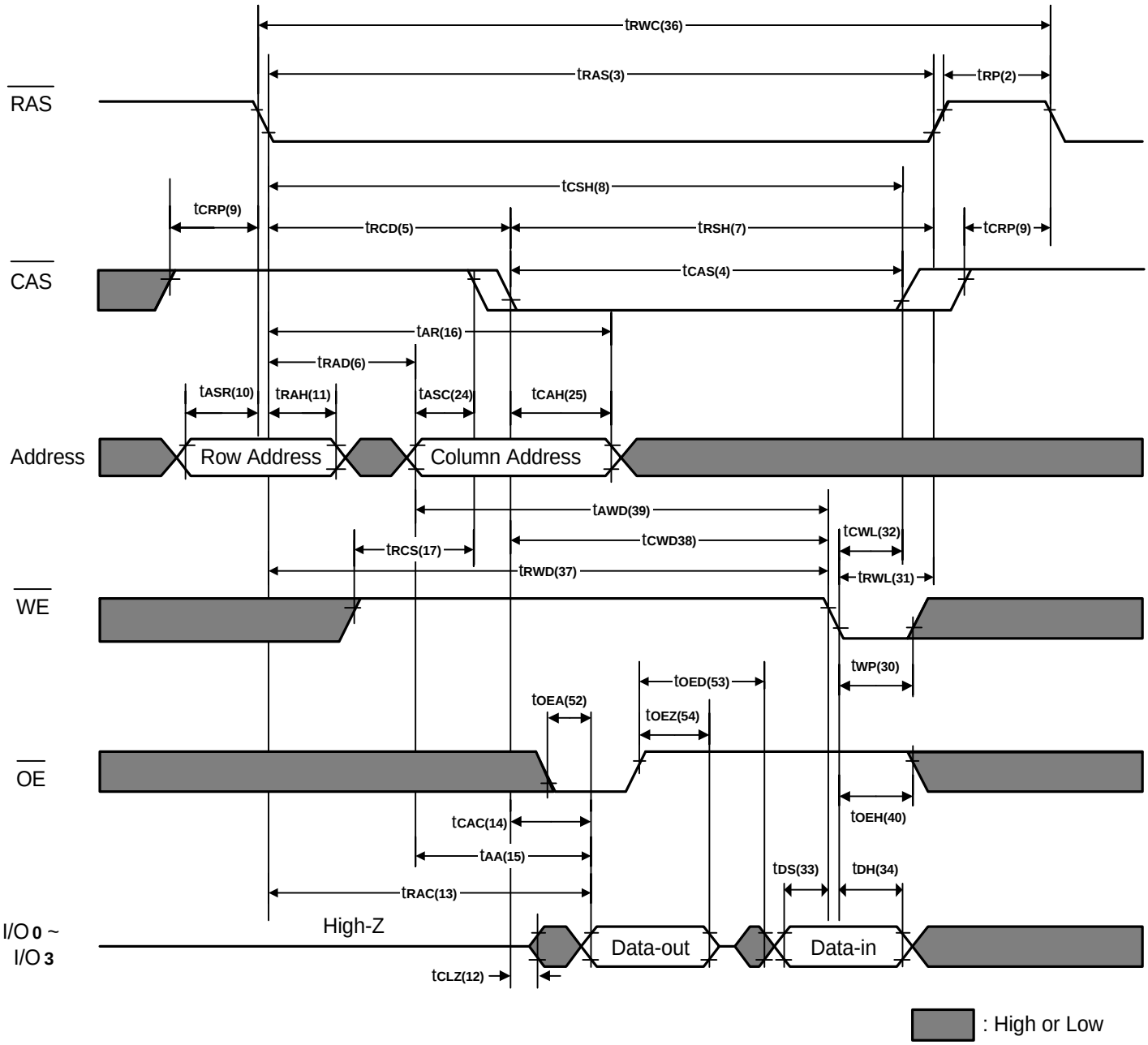
Word Write Cycle (Early Write)



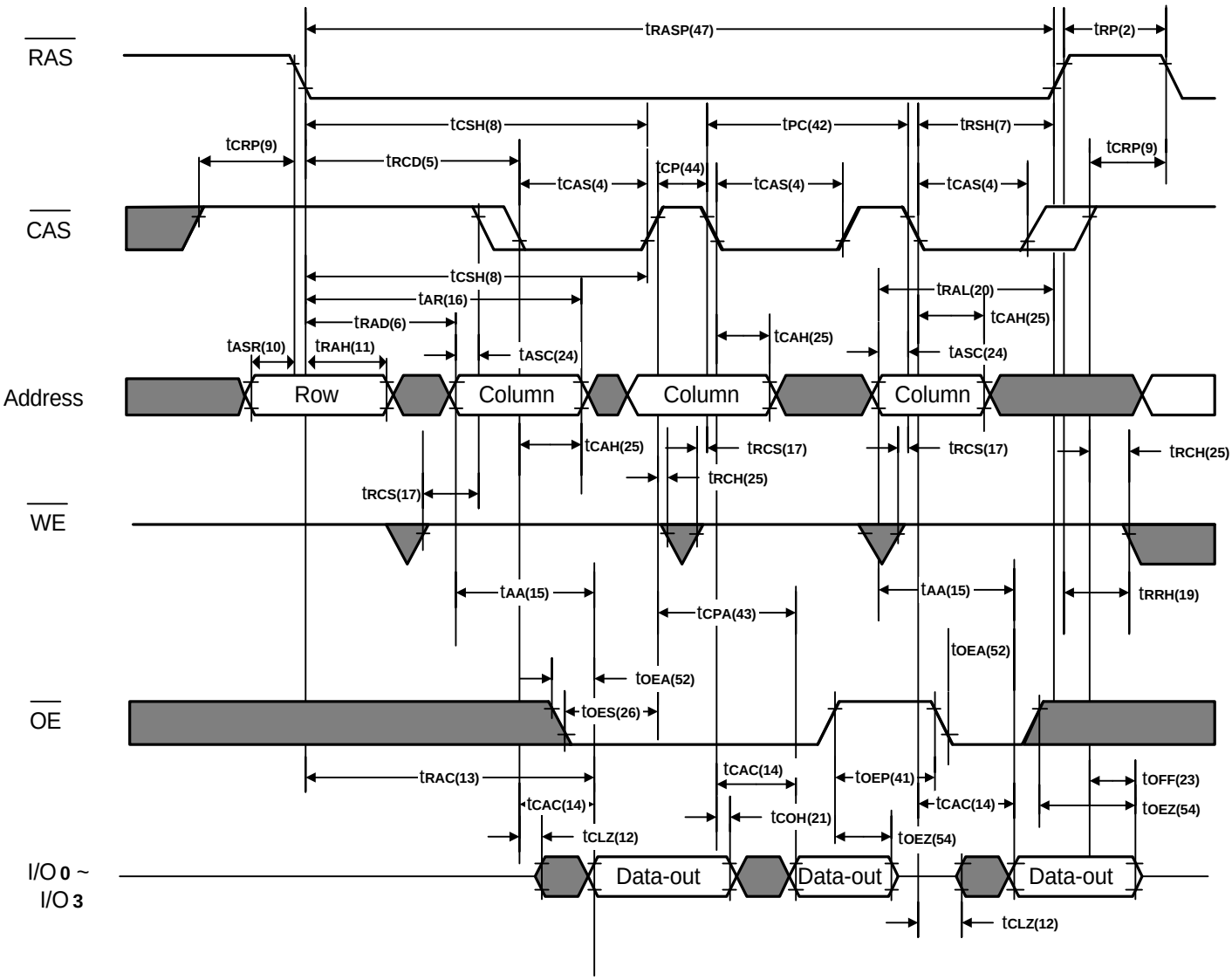
Word Write Cycle (Late Write)



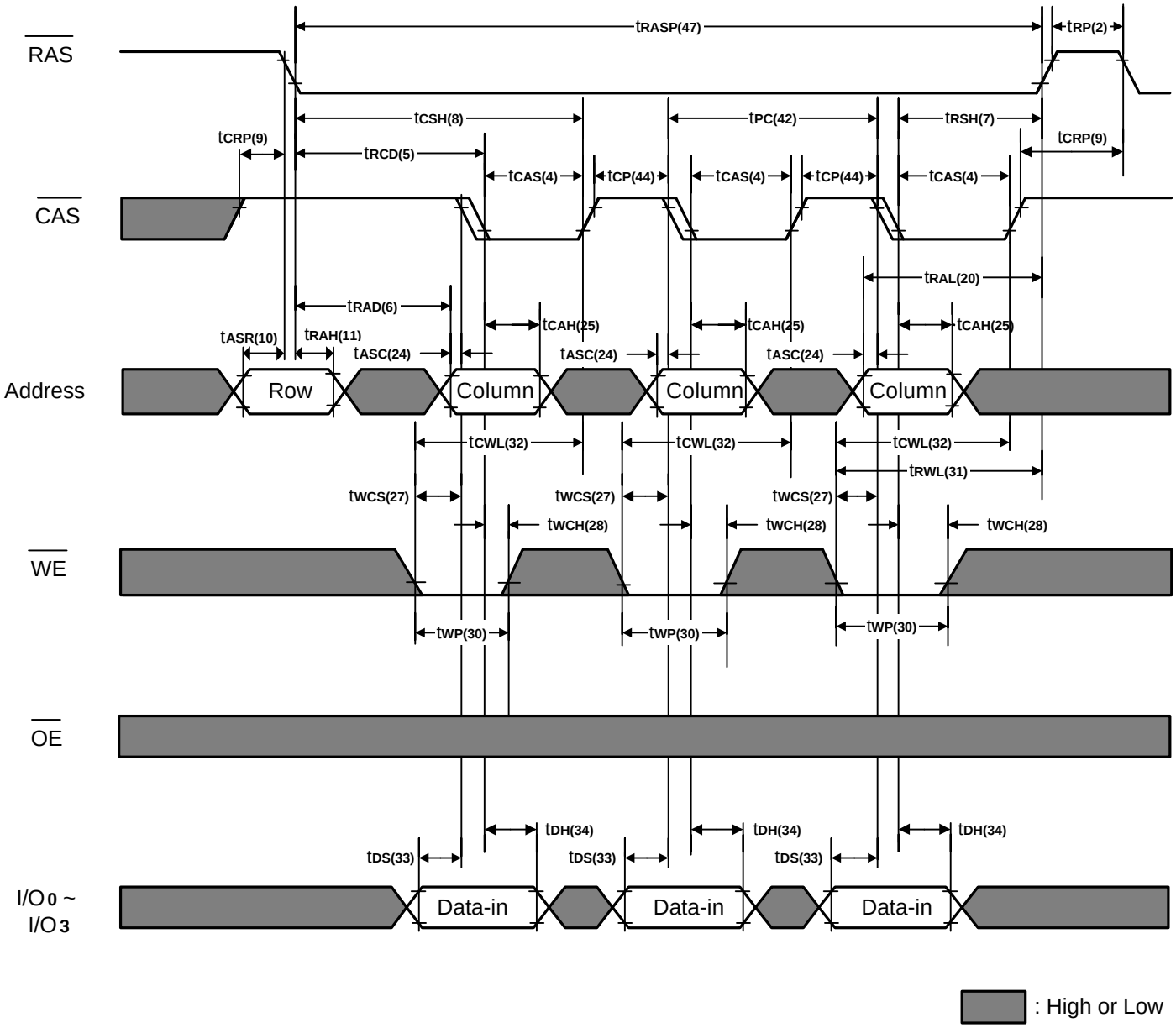
Word Read-Modify-Write Cycle



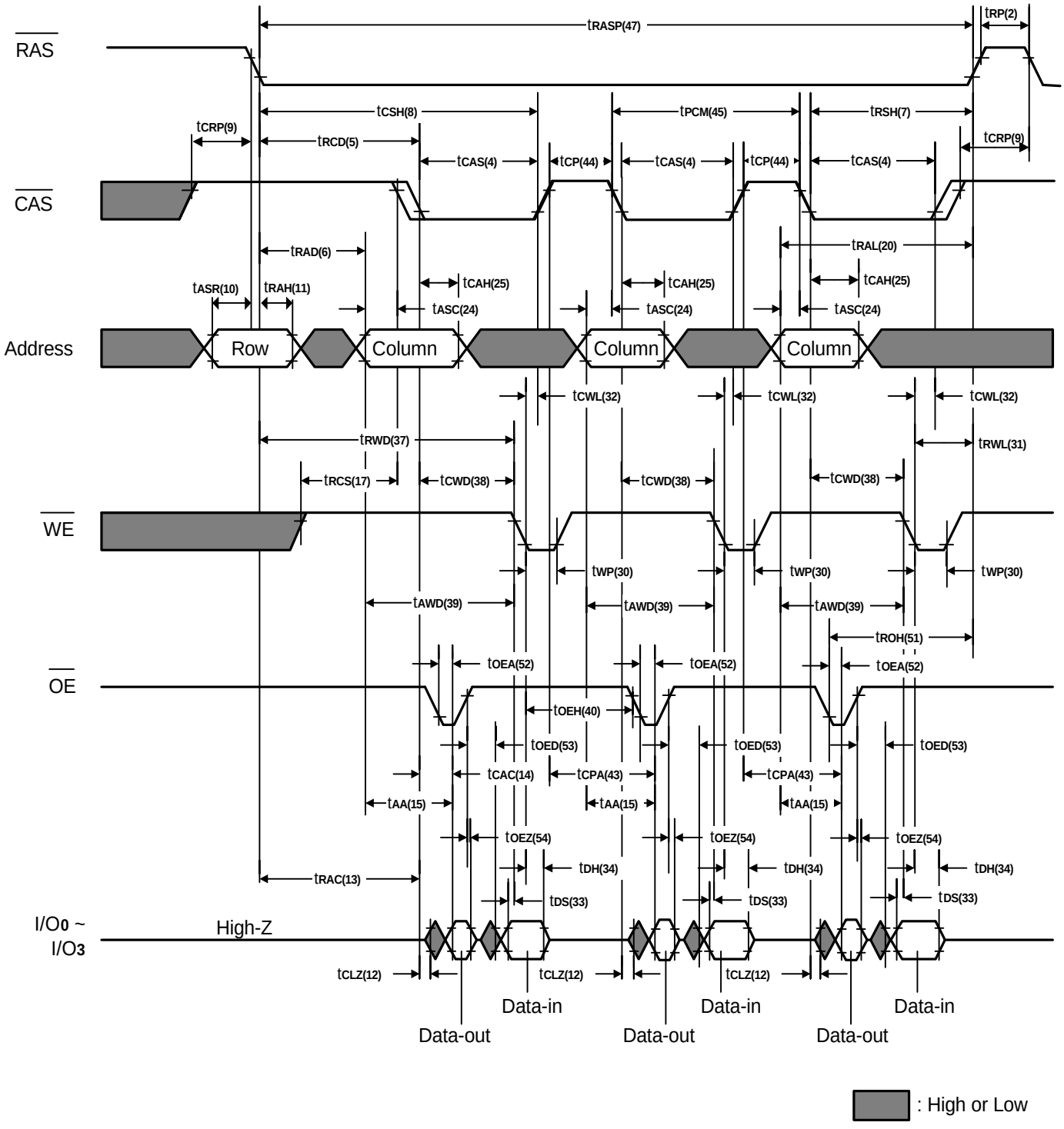
EDO Page Mode Word Read Cycle



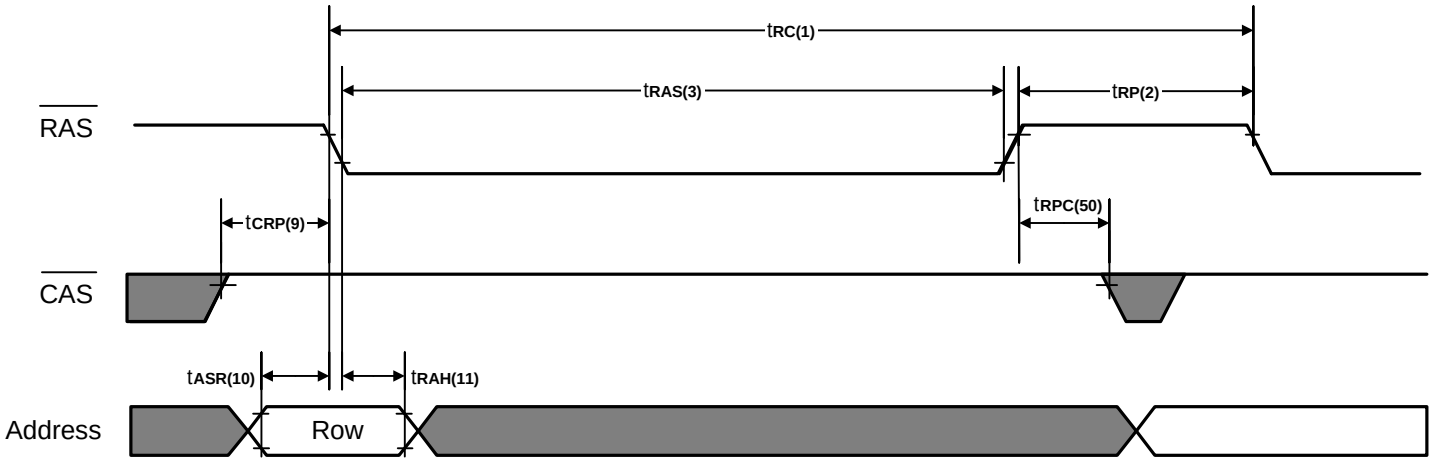
EDO Page Mode Early Word Write Cycle



EDO Page Mode Word Read-Modify-Write Cycle



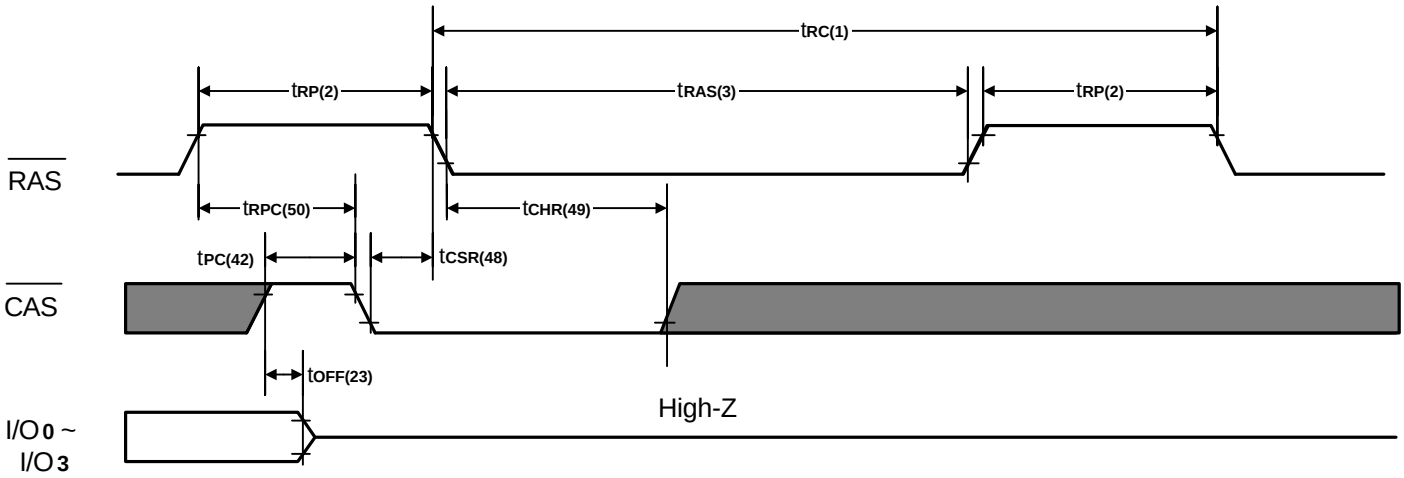
$\overline{RAS}$ Only Refresh Cycle



Note: $\overline{WE}$, $\overline{OE}$ = Don't care.

: High or Low

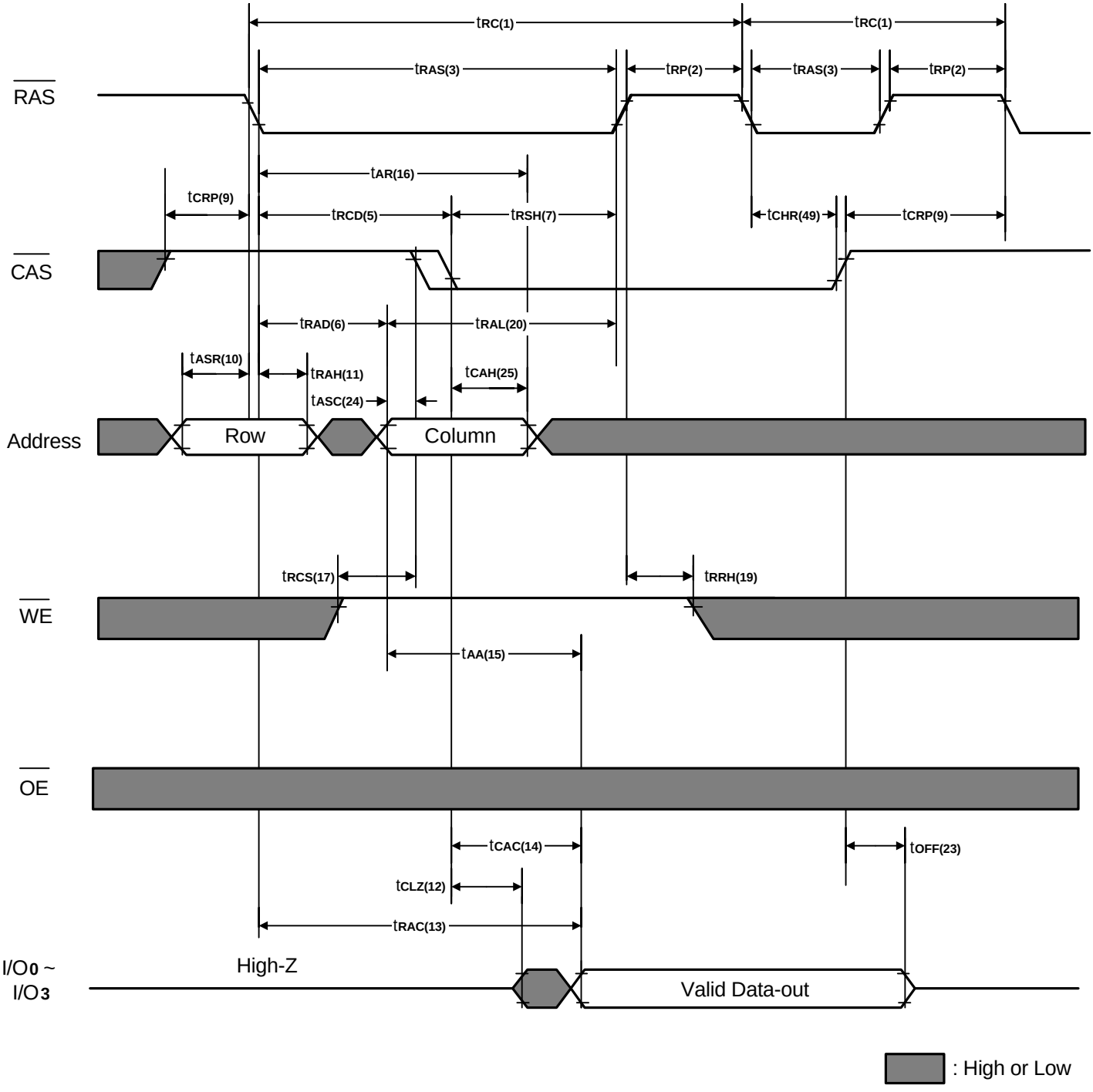
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



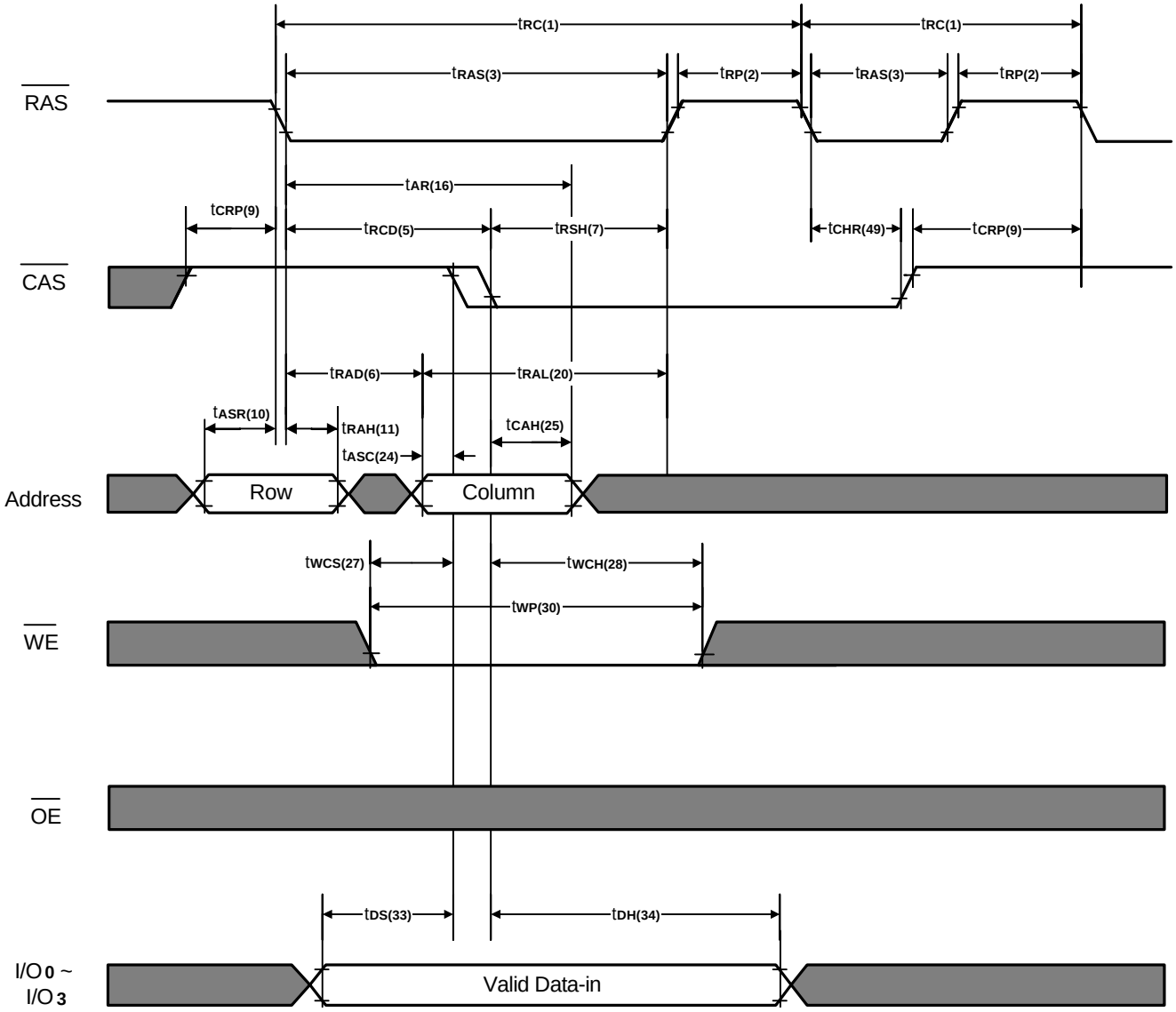
Note: $\overline{WE}$, $\overline{OE}$, Address = Don't care.

: High or Low

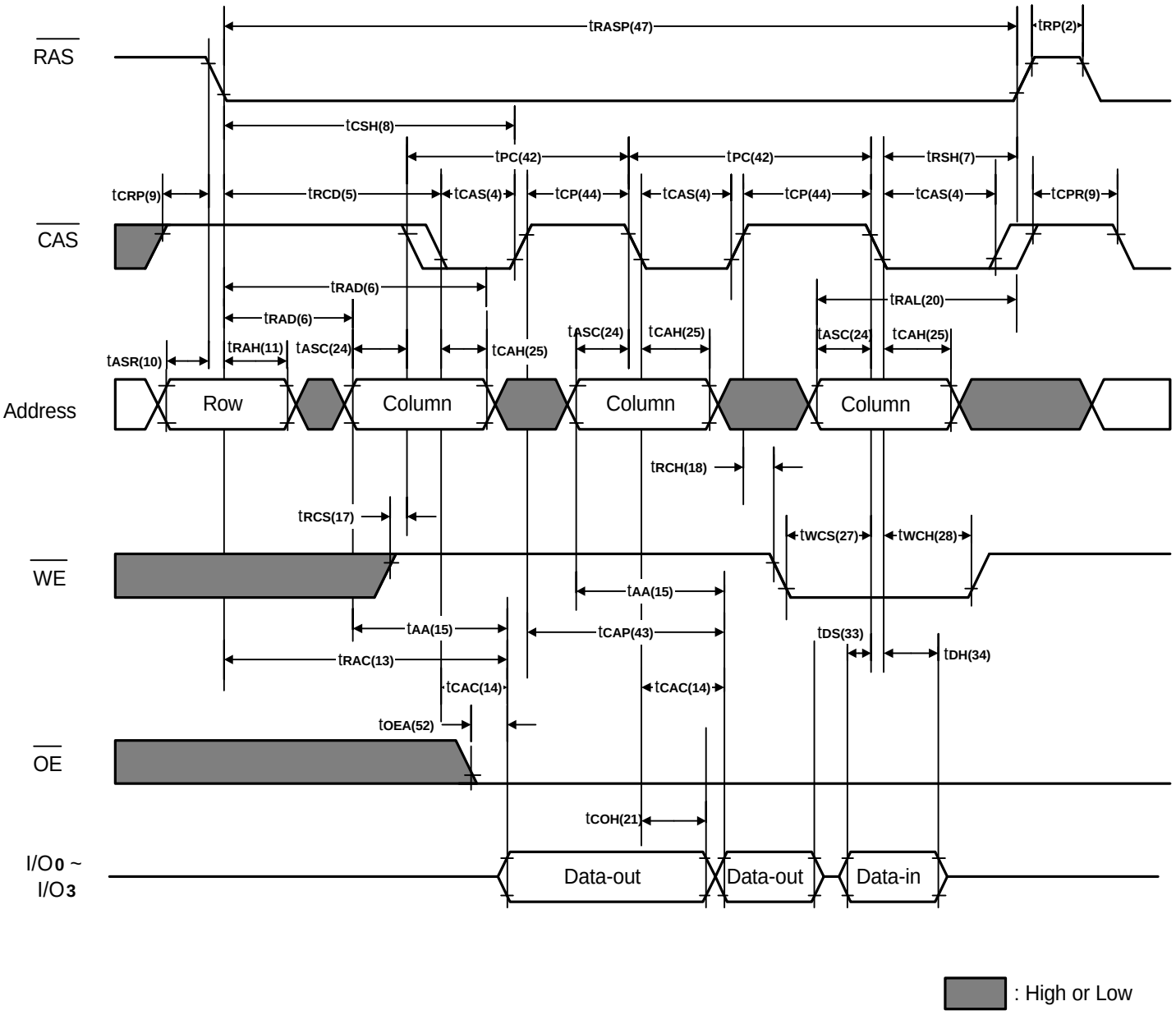
Hidden Refresh Cycle (Word Read)



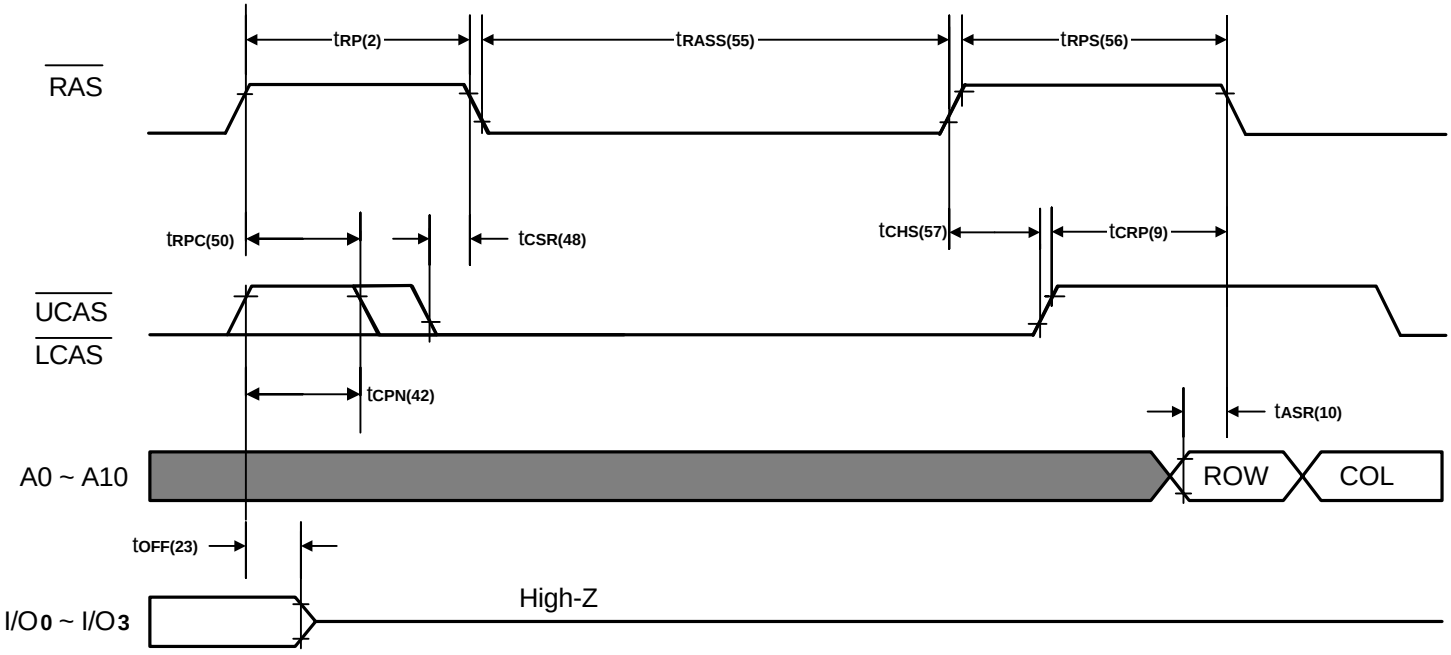
Hidden Refresh Cycle (Early Word Write)



EDO Page Mode Read-Early-Write Cycle (Pseudo Read-Modify-Write)



Self Refresh Mode



Note: $\overline{WE}$, $\overline{OE}$ = Don't care.

: High or Low

■ Self Refresh Mode.

a. Entering the Self Refresh Mode:

The A42U2604 Self Refresh Mode is entered by using $\overline{CAS}$ before $\overline{RAS}$ cycle and holding $\overline{RAS}$ and $\overline{CAS}$ signal "low" longer than 100μs.

b. Continuing the Self Refresh Mode:

The Self Refresh Mode is continued by holding $\overline{RAS}$ "low" after entering the Self Refresh Mode.

It does not depend on $\overline{CAS}$ being "high" or "low" after entering the Self Refresh Mode continue the Self Refresh Mode.

c. Exiting the Self Refresh Mode:

The A42U2604 exits the Self Refresh Mode when the $\overline{RAS}$ signal is brought "high".

Capacitance (Ta = Room Temperature, VCC = 2.5V ± 10%)

Symbol	Signals	Parameter	Max.	Unit	Test Conditions
C_{IN1}	A0 - A10	Input Capacitance	5	pF	Vin = 0V
C_{IN2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$		7	pF	Vin = 0V
$C_{I/O}$	I/O_0 - I/O_3	I/O Capacitance	10	pF	Vin = Vout = 0V

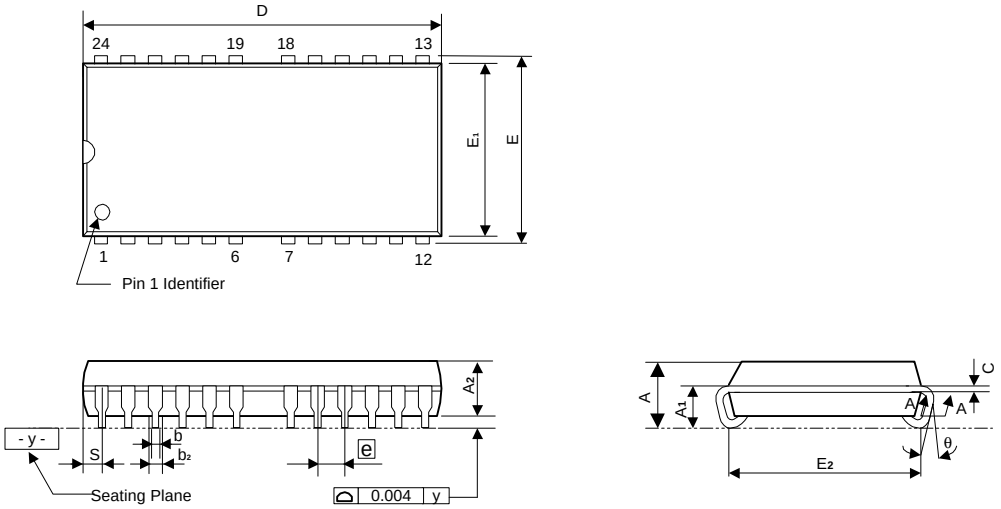
Ordering Codes

Package\ $\overline{RAS}$ Access Time	50ns	60ns	80ns	Refresh Cycle	Self-Refresh
24/26L SOJ (300mil)	A42U2604S-50	A42U2604S-60	A42U2604S-80	2K	Yes
24/26L TSOP type II (300mil)	A42U2604V-50	A42U2604V-60	A42U2604V-80	2K	Yes

Package Information

SOJ 24L/26L (300mil) Outline Dimensions

unit: inches/mm



Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.140	-	-	3.56
A_1	0.070	0.080	0.090	1.78	2.03	2.29
A_2	0.095	0.100	0.105	2.41	2.54	2.67
b	0.016	0.018	0.022	0.41	0.46	0.56
b_2	0.026	0.028	0.032	0.66	0.71	0.81
C	0.008	0.010	0.014	0.20	0.25	0.36
D	-	0.675	0.686	-	17.15	17.42
E	0.327	0.337	0.347	8.31	8.56	8.81
E_1	0.295	0.300	0.305	7.49	7.62	7.75
E_2	0.245	0.265	0.285	6.22	6.73	7.24
e	0.044	0.050	0.056	1.12	1.27	1.42
S	-	-	0.048	-	-	1.22
θ	0°	-	10°	0°	-	10°

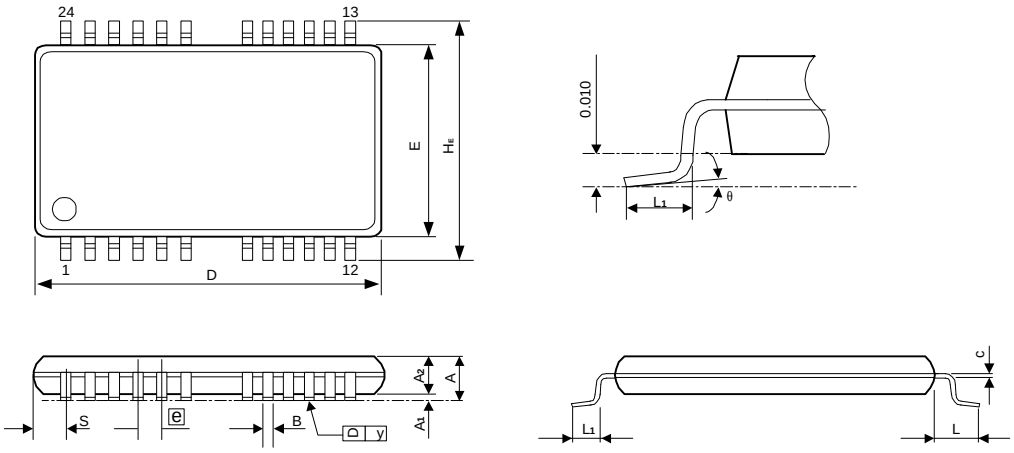
Notes:

1. The maximum value of dimension D includes end flash.
2. Dimension E_1 does not include resin fins.
3. Dimension E_2 is for PC Board surface mount pad pitch design reference only.
4. Dimension S includes end flash.

Package Information

TSOP 24/26L (TYPE II) Outline Dimensions

unit: inches/mm



Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.047	-	-	1.20
A_1	0.002	-	-	0.05	-	-
A_2	0.037	0.039	0.041	0.95	1.00	1.05
B	0.012	0.016	0.020	0.30	0.40	0.50
c	-	0.005	-	-	0.127	-
D	0.671	0.675	0.679	17.04	17.14	17.24
E	0.298	0.300	0.302	7.57	7.62	7.67
e	-	0.050	-	-	1.27	-
H_E	0.359	0.363	0.367	9.12	9.22	9.32
L	-	0.031	-	-	0.80	-
L_1	0.016	0.020	0.024	0.40	0.50	0.60
S	-	0.037	-	-	0.95	-
y	-	-	0.004	-	-	0.10
θ	0°	-	5°	0°	-	5°

Notes:
1. Dimension D&E do not included interiead flash.
2. Dimension B does not included dambar protrusion / intrusion.
3. Dimension S includes end flash.