Document Title

64K X 16 BIT HIGH SPEED CMOS SRAM

Revision History

Rev. No.	History	Issue Date	Remark
0.0	Initial issue	July 14, 2000	Preliminary
1.0	Final spec. release	May 8, 2001	Final
	Add -10 spec.		
	Change I_{CC1} from 120mA to 220mA (-12)		
	Change I_{CC1} from 100mA to 210mA (-15)		
	Change I_{SB1} from 8mA to 12mA		
	Change I_{CDR} from 1mA to 5mA		
	Add t_{BE}, t_{BLZ}, t_{BHZ}, t_{BW} parameters		

64K X 16 BIT HIGH SPEED CMOS SRAM

Features

- Center power pinout
- Supply voltage: -10: 3.3V+10%, -5%
  -12, -15: 3.3V±10%
- Access times: 10/12/15 ns (max.)
- Current: Operating: -10: 230mA (max)
  -12: 220mA (max.)
  -15: 210mA (max.)
  Standby: TTL: 25mA (max.)
  CMOS: 12mA (max.)
- Full static operation, no clock or refreshing required
- All inputs and outputs are directly TTL-compatible
- Common I/O using three-state output
- Data retention voltage: 2V (min.)
- Available in 44-pin 400mil SOJ and 44-pin 400mil TSOP(II) forward packages.

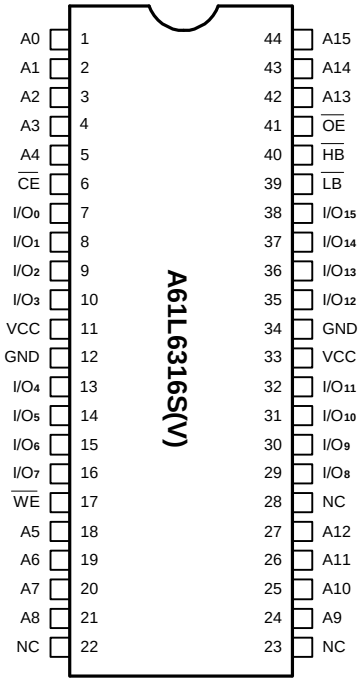
General Description

The A61L6316 is a high speed 1,048,576-bit static random access memory organized as 65,536 words by 16 bits and operates on low power supply voltage from 3.0V to 3.6V. It is built using AMIC's high performance CMOS process.
Inputs and three-state outputs are TTL compatible and allow for direct interfacing with common system bus structures.

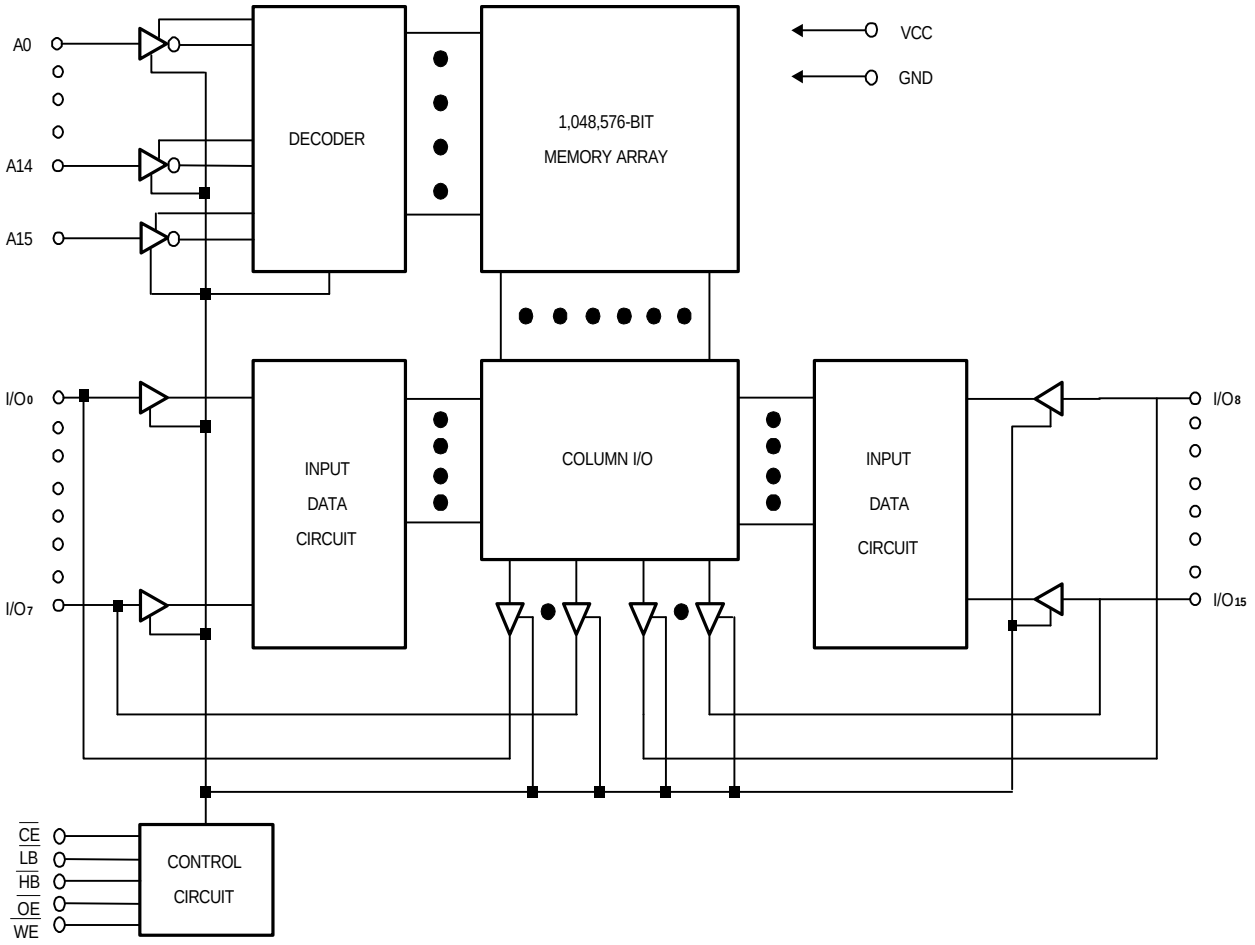
The chip enable input is provided for POWER-DOWN, to disable the device. Two byte enable inputs and an output enable input are included for easy interfacing.
Data retention is guaranteed at a power supply voltage as low as 2V.

Pin Configuration

■ **SOJ / TSOP(II)**



Block Diagram



Pin Description - SOJ/TSOP(II)

Pin No.	Symbol	Description
1 - 5, 18 - 21, 24 - 27,42 - 44	A0 - A15	Address Inputs
6	$\overline{CE}$	Chip Enable Input
7 - 10, 13 - 16, 29 - 32, 35 - 38	I/O_0 - I/O_{15}	Data Input/Outputs
17	$\overline{WE}$	Write Enable Input
39	$\overline{LB}$	Byte Enable Input (I/O_0 to I/O_7)
40	$\overline{HB}$	Byte Enable Input (I/O_8 to I/O_{15})
41	$\overline{OE}$	Output Enable Input
11, 33	VCC	Power
12, 34	GND	Ground
22 , 23, 28	NC	No Connection

Recommended DC Operating Conditions

(T_A = 0°C to + 70°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit
*VCC	Supply Voltage	3.0	3.3	3.6	V
GND	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	-	VCC + 0.3	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	V
C_L	Output Load	-	-	30	pF

* -10 V_{ccmin}: 3.135V

Absolute Maximum Ratings*

VCC to GND . . . . . -0.5V to +4.6V
IN, IN/OUT Volt to GND . . . . . -0.5V to VCC + 0.5V
Operating Temperature, Topr . . . . . 0°C to +70°C
Storage Temperature, Tstg . . . . . -55°C to +125°C
Power Dissipation, P_T 0.7W
Soldering Temp. & Time . . . . . 260°C, 10 sec

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (T_A = 0°C to + 70°C, -10: 3.3V+10%, -5%; -12, -15: 3.3V±10%)

Symbol	Parameter	A61L6316-10		A61L6316-12		A61L6316-15		Unit	Conditions
		Min.	Max.	Min.	Max.	Min.	Max.		
$\|I_{LI}\|$	Input Leakage	-	2	-	2	-	2	µA	V_{IN} = GND to VCC
$\|I_{LO}\|$	Output Leakage	-	2	-	2	-	2	µA	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IH} $V_{I/O}$ = GND to VCC
I_{CC1} (2)	Dynamic Operating Current	-	230	-	220	-	210	mA	$\overline{CE}$ = V_{IL}, $I_{I/O}$ = 0 mA Min. Cycle, Duty = 100%
I_{SB}	Standby Power Supply Current	-	25	-	25	-	25	mA	$\overline{CE}$ = V_{IH}
I_{SB1}		-	12	-	12	-	12	mA	$\overline{CE}$ ≥ VCC - 0.2V, V_{IN} ≥ VCC -0.2V or V_{IN} ≤ 0.2V
V_{OL}	Output Low Voltage	-	0.4	-	0.4	-	0.4	V	I_{OL} = 8 mA
V_{OH}	Output High Voltage	2.4	-	2.4	-	2.4	-	V	I_{OH} = -4 mA

Notes: 1. V_{IL} = -3.0V for pulses less than 20 ns.
2. I_{CC1} is dependent on output loading, cycle rates, and Read/Write patterns.

Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{HB}$	I/O_0 to I/O_7 Mode	I/O_8 to I/O_{15} Mode	VCC Current
H	X	X	X	X	Not selected	Not selected	I_{SB1}, I_{SB}
L	L	H	L	L	Read	Read	I_{CC1}, I_{CC2}, I_{CC}
			L	H	Read	High - Z	I_{CC1}, I_{CC2}, I_{CC}
			H	L	High - Z	Read	I_{CC1}, I_{CC2}, I_{CC}
L	X	L	L	L	Write	Write	I_{CC1}, I_{CC2}, I_{CC}
			L	H	Write	Not Write/Hi - Z	I_{CC1}, I_{CC2}, I_{CC}
			H	L	Not Write/Hi - Z	Write	I_{CC1}, I_{CC2}, I_{CC}
L	H	H	L	X	High - Z	High - Z	I_{CC1}, I_{CC2}, I_{CC}
			X	L	High - Z	High - Z	I_{CC1}, I_{CC2}, I_{CC}
X	X	X	H	H	Not selected	Not selected	I_{SB1}, I_{SB}

Note: X = H or L

Capacitance (T_A = 25°C, f = 1.0MHz)

Symbol	Parameter	Min.	Max.	Unit	Conditions
C_{IN}*	Input Capacitance	-	6	pF	V_{IN} = 0V
$C_{I/O}$*	Input/Output Capacitance	-	8	pF	$V_{I/O}$ = 0V

* These parameters are sampled and not 100% tested.

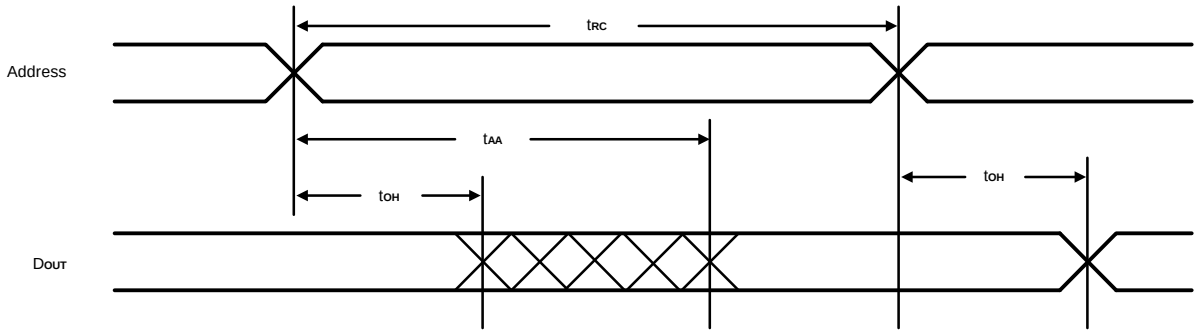
AC Characteristics (T_A = 0°C to +70°C, -10: 3.3V+10%, -5%; -12, -15: 3.3V±10%)

Symbol	Parameter	A61L6316-10		A61L6316-12		A61L6316-15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t_{RC}	Read Cycle Time	10	-	12	-	15	-	ns
t_{AA}	Address Access Time	-	10	-	12	-	15	ns
t_{ACE}	Chip Enable Access Time	-	10	-	12	-	15	ns
t_{BE}	Byte Enable Access Time	-	5	-	6	-	8	ns
t_{OE}	Output Enable to Output Valid	-	5	-	6	-	8	ns
t_{CLZ}	Chip Enable to Output in Low Z	3	-	3	-	3	-	ns
t_{OLZ}	Output Enable to Output in Low Z	0	-	0	-	0	-	ns
t_{BLZ}	Byte Enable to Output in Low Z	0	-	0	-	0	-	ns
t_{CHZ}	Chip Disable Output in High Z	0	5	0	6	-	8	ns
t_{BHZ}	Byte Disable to Output in High Z	0	5	0	6	0	8	ns
t_{OHZ}	Output Disable to Output in High Z	0	5	0	6	0	8	ns
t_{OH}	Output Hold from Address Change	3	-	3	-	3	-	ns
Write Cycle								
t_{WC}	Write Cycle Time	10	-	12	-	15	-	ns
t_{CW}	Chip Enable to End of Write	8	-	10	-	12	-	ns
t_{BW}	Byte Enable to End of Write	8	-	10	-	12	-	ns
t_{AS}	Address Setup Time of Write	0	-	0	-	0	-	ns
t_{AW}	Address Valid to End of Write	8	-	10	-	12	-	ns
t_{WP}	Write Pulse Width	8	-	10	-	12	-	ns
t_{WR}	Write Recovery Time	0	-	0	-	0	-	ns
t_{WHZ}	Write to Output in High Z	0	5	0	6	0	8	ns
t_{DW}	Data to Write Time Overlap	5	-	6	-	7	-	ns
t_{DH}	Data Hold from Write Time	0	-	0	-	0	-	ns
t_{OW}	Output Active from End of Write	3	-	3	-	3	-	ns

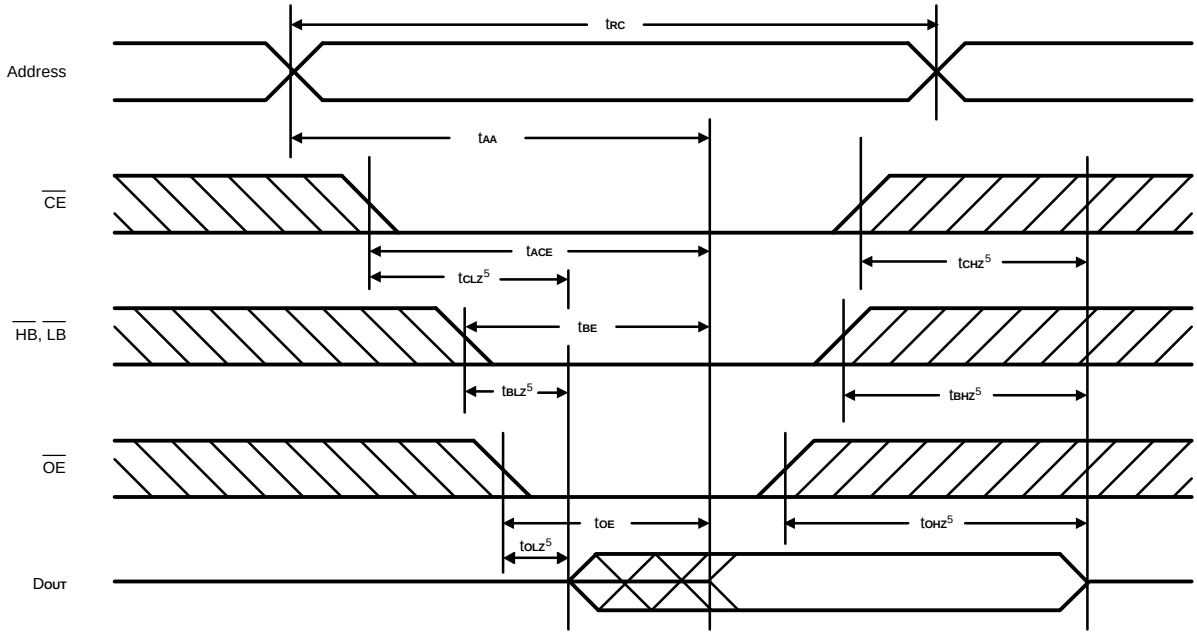
Notes: t_{CHZ}, t_{BHZ}, t_{OHZ} and t_{WHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.

Timing Waveforms

Read Cycle 1[1, 2, 4]



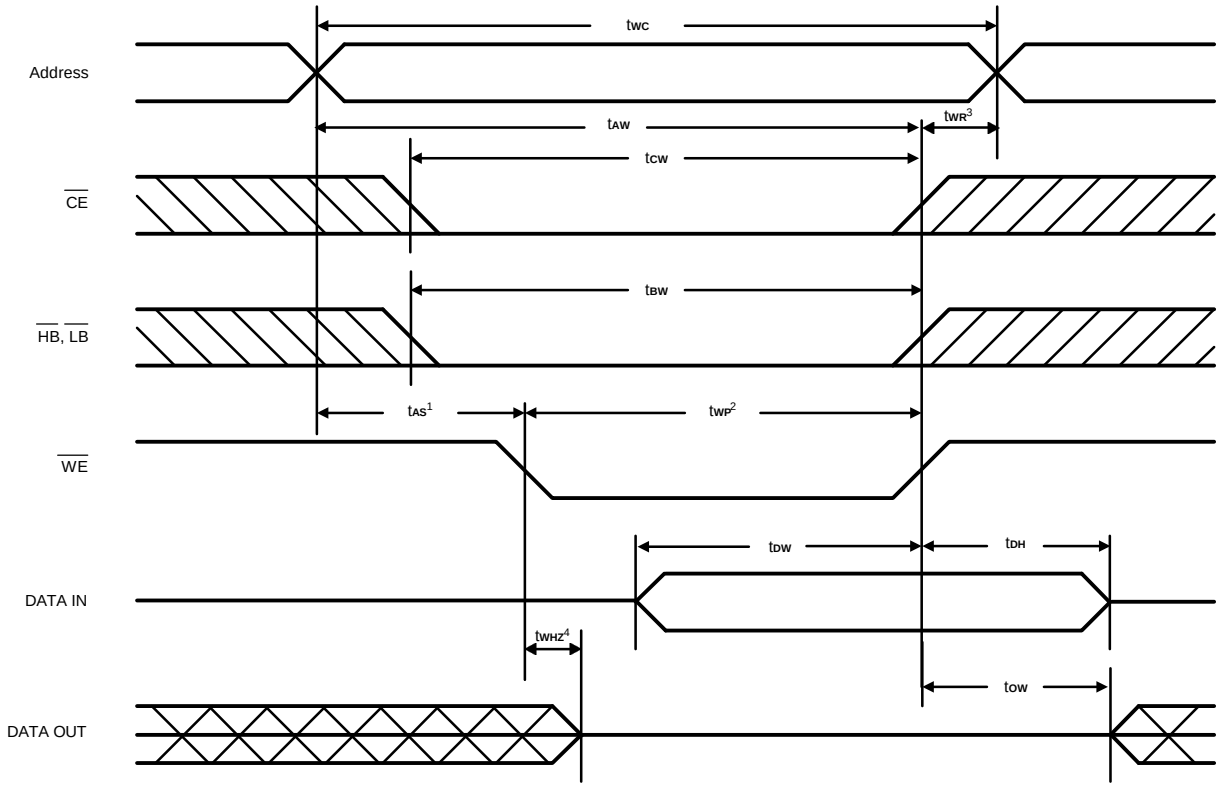
Read Cycle 2[1, 2, 3]



Notes: 1. $\overline{WE}$ is high for Read Cycle.
2. Device is continuously enabled $\overline{CE}$ = V_{IL}, $\overline{HB}$ = V_{IH} and, or $\overline{LB}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CE}$ and ($\overline{HB}$ and, or $\overline{LB}$) transition low.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±200mV from steady state. This parameter is sampled and not 100% tested.

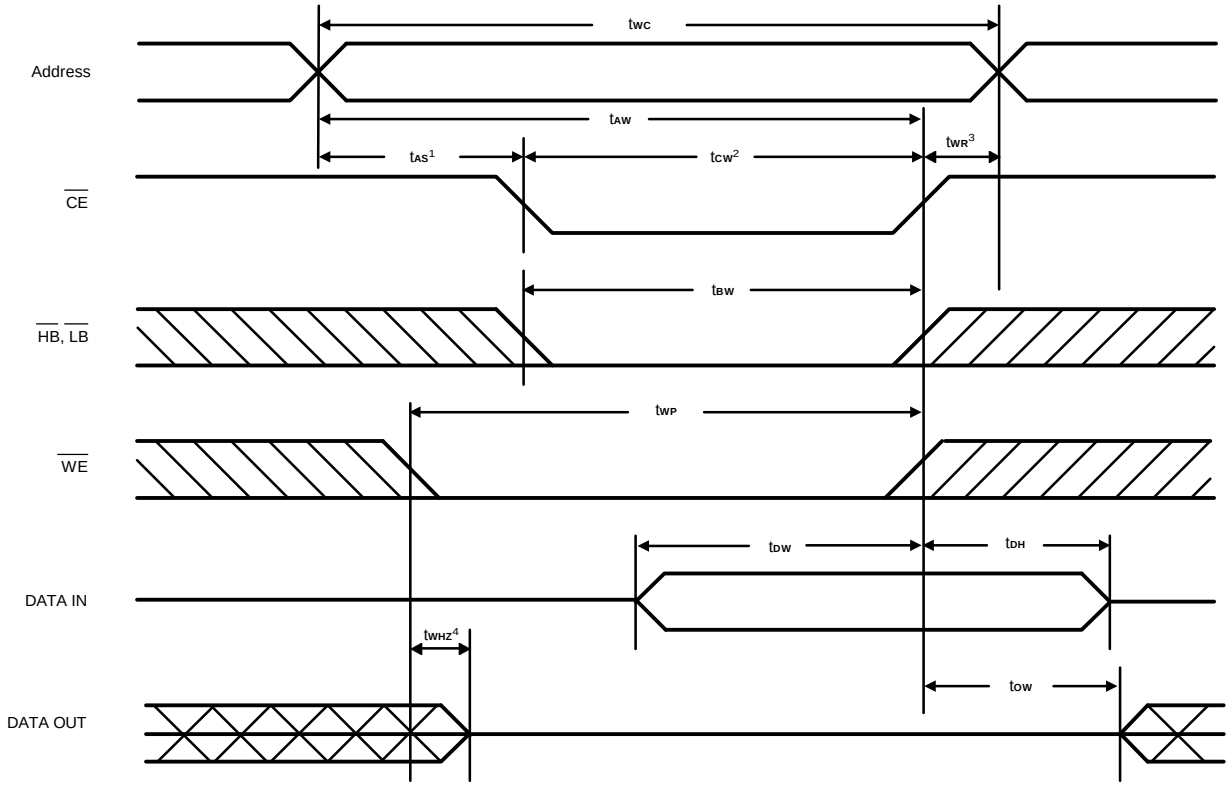
Timing Waveforms (continued)

Write Cycle 1
(Write Enable Controlled)



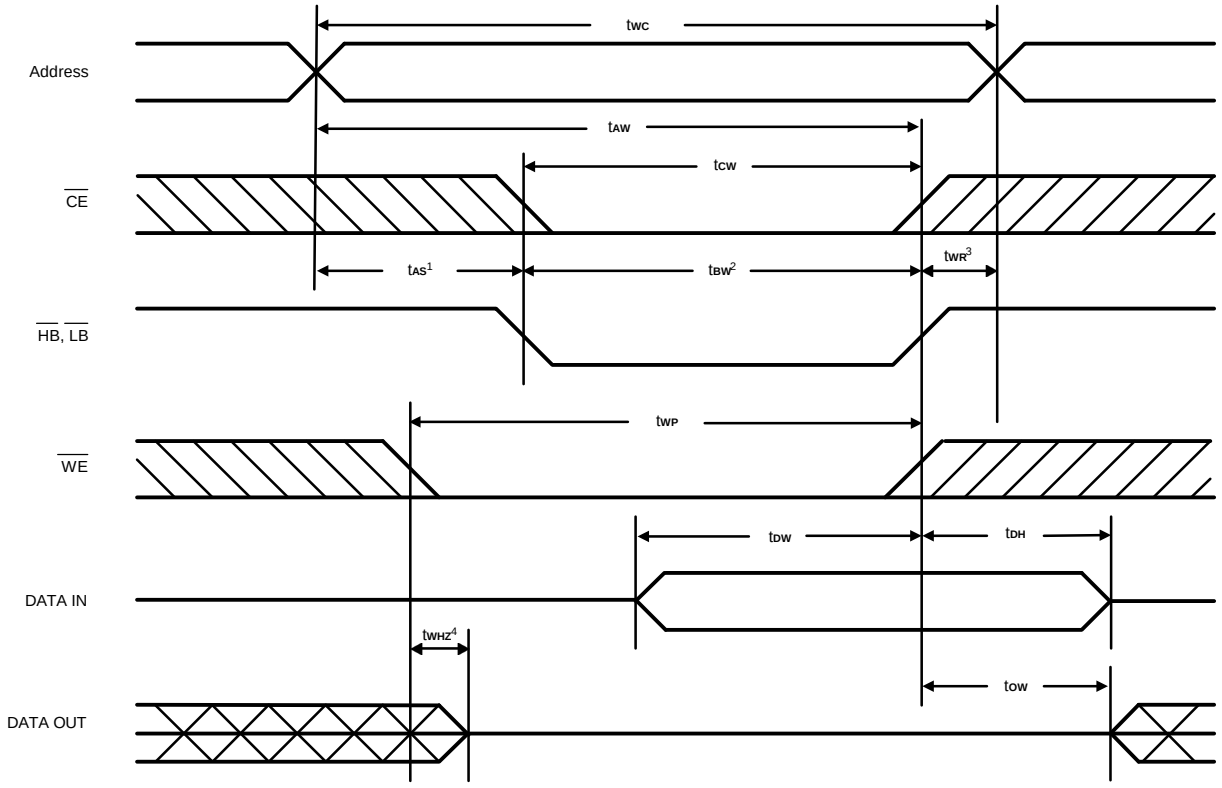
Timing Waveforms (continued)

Write Cycle 2
(Chip Enable Controlled)



Timing Waveforms (continued)

Write Cycle 3
(Byte Enable Controlled)



Notes: 1. t_{AS} is measured from the address valid to the beginning of Write.
2. A Write occurs during the overlap (t_{WP}, t_{BW}) of a low $\overline{CE}$, $\overline{WE}$ and ($\overline{HB}$ and, or $\overline{LB}$).
3. t_{WR} is measured from the earliest of $\overline{CE}$ or $\overline{WE}$ or ($\overline{HB}$ and, or $\overline{LB}$) going high to the end of the Write cycle.
4. $\overline{OE}$ level is high or low.
5. Transition is measured ±200mV from steady state. This parameter is sampled and not 100% tested.

AC Test Conditions

Input Pulse Levels	0V to 3.0V
Input Rise And Fall Time	3 ns
Input and Output Timing Reference Levels	1.5 V
Output Load	See Figures 1 and 2

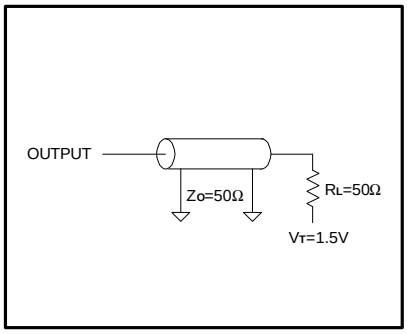


Figure 1. Output Load

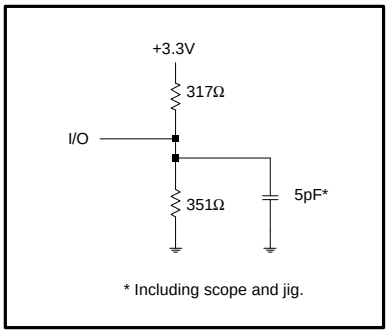


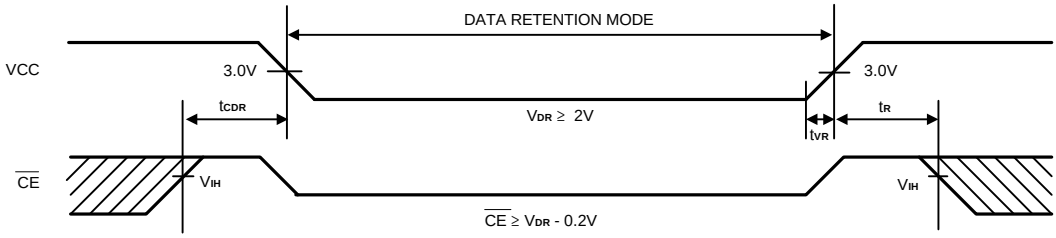
Figure 2. Output Load for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WHZ}, and t_{OW}

Data Retention Characteristics (T_A = 0°C to 70°C)

Symbol	Parameter	Min.	Max.	Unit	Conditions
V_{DR}	VCC for Data Retention	2	3.6	V	$\overline{CE}$ ≥ VCC - 0.2V
I_{CCDR}	Data Retention Current	-	5	mA	VCC = 2.0V $\overline{CE}$ ≥ VCC - 0.2V V_{IN} ≥ VCC - 0.2V or V_{IN} ≤ 0.2V
t_{CDR}	Chip Disable to Data Retention Time	0	-	ns	See Retention Waveform
t_R	Operation Recovery Time	T_{RC}*	-	ms	

t_{RC} = Read Cycle Time

Low VCC Data Retention Waveform



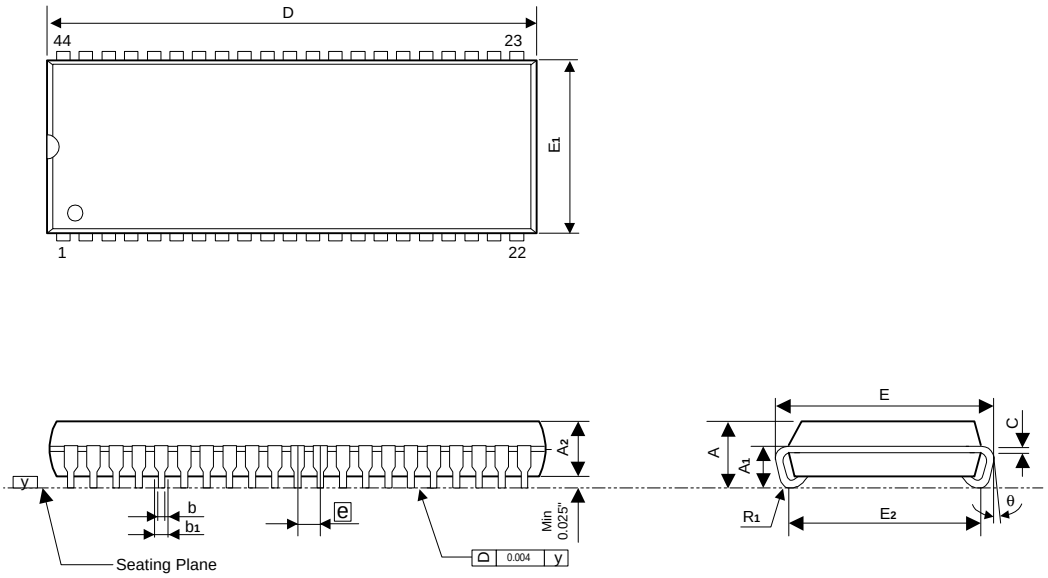
Ordering Information

Part No.	Access Time (ns)	Operating Current Max. (mA)	Standby Current Max. (mA)	Package
A61L6316S-10	10	230	12	44L SOJ
A61L6316V-10				44L TSOP(II)
A61L6316S-12	12	220	12	44L SOJ
A61L6316V-12				44L TSOP(II)
A61L6316S-15	15	210	12	44L SOJ
A61L6316V-15				44L TSOP(II)

Package Information

SOJ 44L Outline Dimensions

unit: inches/mm



Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	0.128	0.138	0.148	3.25	3.51	3.76
A_1	0.082	-	-	2.08	-	-
A_2	0.105	0.110	0.115	2.67	2.79	2.92
b	0.015	-	0.020	0.38	-	0.51
b_1	0.026	0.028	0.032	0.66	0.71	0.81
C	0.007	-	0.013	0.18	-	0.21
D	1.120	1.125	1.130	28.45	28.58	28.70
E	0.435	0.440	0.445	11.05	11.18	11.30
E_1	0.394	0.400	0.405	10.01	10.16	10.29
E_2	0.370 BSC			9.40 BSC		
e	0.050 BSC			1.27 BSC		
R_1	0.030	0.035	0.040	0.76	0.89	1.02
θ	0°	-	10°	0°	-	10°

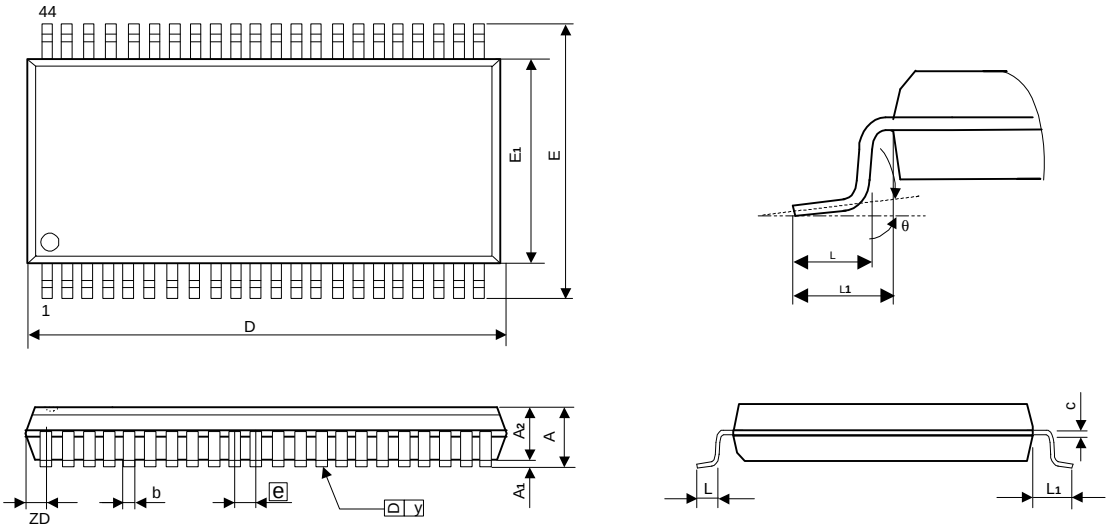
Notes:

1. The maximum value of dimension D includes end flash.
2. Dimension E does not include resin fins.
3. Dimension E_1 is for PC Board surface mount pad pitch design reference only.

Package Information

TSOP 44L (Type II) Outline Dimensions

unit: inches/mm



Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.047	-	-	1.20
A_1	0.002	-	0.006	0.05	-	0.15
A_2	0.037	0.039	0.041	0.95	1.00	1.05
b	0.012	-	0.018	0.30	-	0.45
c	0.005	-	0.008	0.12	-	0.21
D	0.720	0.725	0.730	18.28	18.41	18.54
ZD	0.032 REF			0.805 REF		
E	0.455	0.463	0.471	11.56	11.76	11.96
E_1	0.395	0.400	0.405	10.03	10.16	10.29
L	0.019	0.023	0.027	0.49	0.59	0.69
L_1	0.031 REF			0.80 REF		
e	0.031 BSC			0.80 BSC		
y	-	-	0.004	-	-	0.10
θ	0°	-	5°	0°	-	5°

Notes:
1. The maximum value of dimension D includes end flash.
2. Dimension E_1 does not include resin fins.
3. Dimension ZD includes end flash.