Document Title

2M and 256K MaskRAM

Revision History

Rev. No.	History	Issue Date	Remark
2.0	Final spec release	October 12, 1998	Final
2.1	Change t_{OE} speed from 150ns to 200ns	November 20, 1998	

A26E001A

2M and 256K MaskRAM

Features

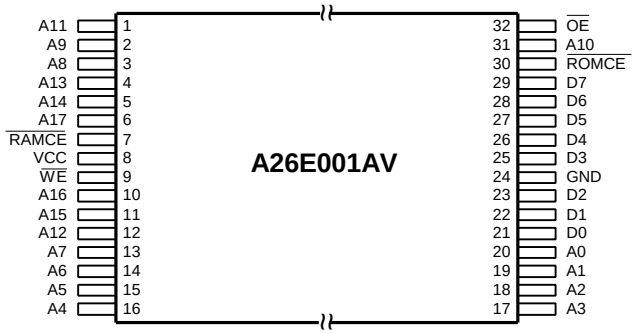
- Power supply range: 1.8V to 3.3V
- Access time: 450 ns (max.)
- Current:
  Low power version: Operating: 4mA (max.)
  Standby: 10µA (max.)
- Extended operating temperature range: -25°C to 85°C
- Full static operation, no clock or refreshing required
- All inputs and outputs are CMOS compatible
- Common I/O using three-state output
- Data retention voltage: 1.6V (min.)
- Available in 32-pin TSOP and sTSOP packages

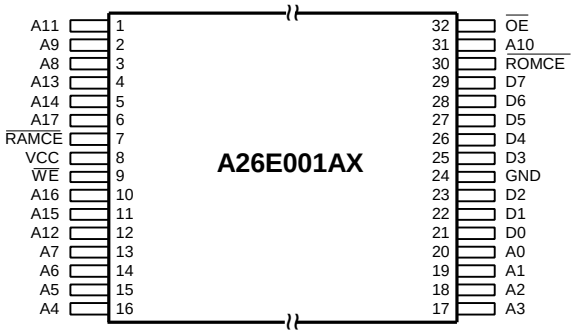
General Description

The A26E001A is a low operating current 262,144 x 8 bit CMOS MASK ROM and 32,768 x 8 bit CMOS SRAM integrated into one chip. It operates on a low power supply voltage from 1.8V to 3.3V, with two chip selects to enable the MASK ROM or SRAM independently.
Inputs and three-state outputs are CMOS compatible and allow for direct interfacing with common system bus structures.

Minimum standby power is drawn by this device when $\overline{\text{ROMCE}}$ and $\overline{\text{RAMCE}}$ are at a high level, independent of the other input levels.
Data retention is guaranteed at a power supply voltage as low as 1.6V.

Pin Configuration

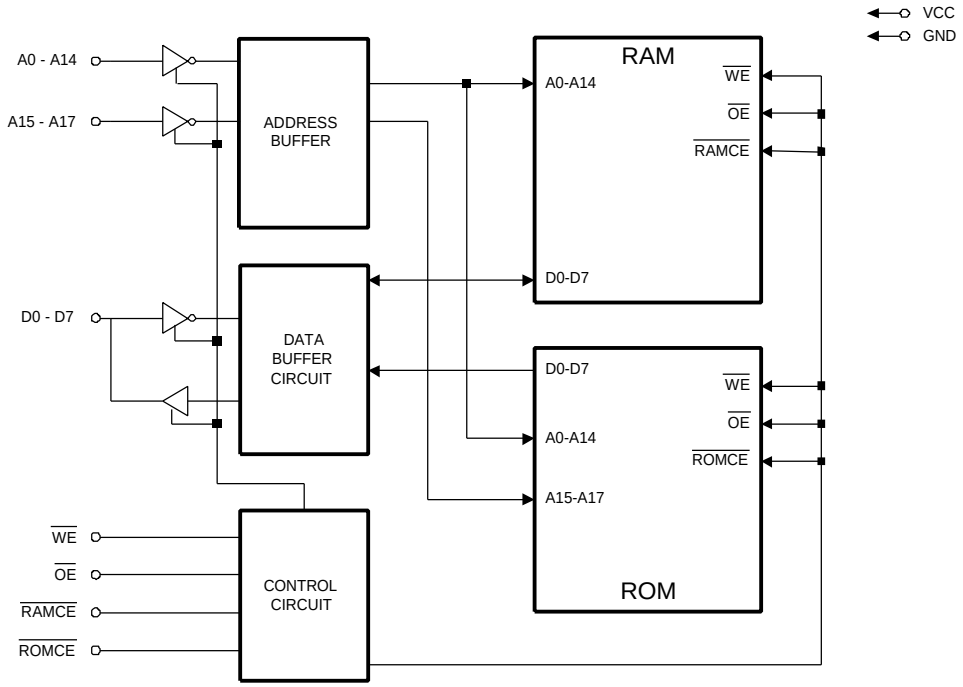




Pin Description

Pin No.	Symbol	Description
1 - 6, 10 - 20, 31	A0 - A17	Address Inputs
7	$\overline{\text{RAMCE}}$	SRAM Enable
9	$\overline{\text{WE}}$	Write Enable
21 - 23, 25 - 29	D0 - D7	Data Input/Outputs
30	$\overline{\text{ROMCE}}$	ROM Enable
32	$\overline{\text{OE}}$	Output Enable
8	VCC	Power Supply
24	GND	Ground

Block Diagram



Truth Table

Mode	$\overline{ROMCE}$	$\overline{RAMCE}$	$\overline{OE}$	$\overline{WE}$	D0 - D7	Supply Current
Standby	H	H	X	X	High Z	I_{SB}, I_{SB1}
Output Disable	L	H	H	X	High Z	I_{CCR}
ROM Read	L	H	L	X	D_{OUT}	I_{CCR}
Output Disable	H	L	H	H	High Z	I_{CCS}
SRAM Read	H	L	L	H	D_{OUT}	I_{CCS}
SRAM Write	H	L	X	L	D_{IN}	I_{CCS}

Notes:
1. X = H or L
2. A15 - A17 are only valid for ROM.
3. In case that $\overline{ROMCE}$ and $\overline{RAMCE}$ are "L" at the same time, both ROM and SRAM will be disabled.

Recommended DC Operating Conditions

(T_A = -25°C to + 85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	1.8	3.0	3.3	V
GND	Ground	0	0	0	V
V_{IH}	Input High Voltage	VCC x 0.7	-	VCC + 0.3	V
V_{IL}	Input Low Voltage	-0.3	-	VCC x 0.3	V

Absolute Maximum Ratings*

VCC to GND . . . . . -0.5V to +4.6V
IN, IN/OUT Volt to GND . . . . . -0.5V to VCC + 0.5V
Operating Temperature, Topr . . . . . -25°C to +85°C
Storage Temperature, Tstg . . . . . -55°C to +125°C
Power Dissipation, P_T 0.7W
Soldering Temp. & Time . . . . . 260°C, 10 sec

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

(T_A = -25°C to + 85°C, VCC = 1.8V to 3.3V)

Symbol	Parameter	Min.	Max.	Unit	Conditions
$\lvert I_{LI} \rvert$	Input Leakage Current	-	1	µA	V_{IN} = GND to VCC
$\lvert I_{LO} \rvert$	Output Leakage Current	-	1	µA	$V_{I/O}$ = GND to VCC
I_{CCR}	ROM Operating Current	-	4	mA	Min. Cycle, Duty = 100% $\overline{ROMCE}$ = V_{IL} and $\overline{RAMCE}$ = V_{IH}, $I_{I/O}$ = 0mA, V_{IN} = VCC or GND
I_{CCS}	SRAM Operating Current	-	4	mA	Min. Cycle, Duty = 100% $\overline{ROMCE}$ = V_{IH} and $\overline{RAMCE}$ = V_{IL}, $I_{I/O}$ = 0mA, V_{IN} = VCC or GND
I_{SB}	Standby Supply Current	-	50	µA	$\overline{ROMCE}$ = V_{IH} and $\overline{RAMCE}$ = V_{IH}
I_{SB1}		-	10	µA	$\overline{ROMCE}$ ≥ VCC - 0.2V and $\overline{RAMCE}$ ≥ VCC - o.2V
V_{OL}	Output Low Voltage	-	0.4	V	I_{OL} = 200µA
V_{OH}	Output High Voltage	VCC - 0.4	-	V	I_{OH} = -200µA

Capacitance

(T_A = 25°C, f = 1.0MHz)

Symbol	Parameter	Min.	Max.	Unit	Conditions
C_I*	Input Capacitance		6	pF	T_A = 25°C f = 1.0MHz
Co*	Input/Output Capacitance		8	pF	

* These parameters are sampled and not 100% tested.

AC Characteristics (ROM/SRAM Selection)

(T_A = -25°C to +85°C, VCC = 1.8V to 3.3V)

Symbol	Parameter	Min.	Max.	Unit
t_{RTS}	$\overline{\text{ROMCE}}$ Disable to $\overline{\text{RAMCE}}$ Enable Time	10	-	ns
t_{STR}	$\overline{\text{RAMCE}}$ Disable to $\overline{\text{ROMCE}}$ Enable Time	10	-	ns

AC Characteristics (ROM Selected)

(T_A = -25°C to +85°C, VCC = 1.8V to 3.3V)

Symbol	Parameter	Min.	Max.	Unit
t_{RC}	Read Cycle Time	500	-	ns
t_{AA}	Address Access Time	-	450	ns
t_{ACE}	$\overline{\text{ROMCE}}$ Chip Enable Access Time	-	450	ns
t_{OE}	Output Enable to Output Valid	-	200	ns
t_{CLZ}	$\overline{\text{ROMCE}}$ Chip Enable to Output in Low Z	10	-	ns
t_{OLZ}	Output Enable to Output in Low Z	10	-	ns
t_{CHZ}	$\overline{\text{ROMCE}}$ Chip Disable to Output in High Z	-	100	ns
t_{OHZ}	Output Disable to Output in High Z	-	100	ns
t_{OH}	Output Hold from Address Change	10	-	ns

Notes: t_{CHZ}, and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.

AC Characteristics (SRAM Selected) (T_A = -25°C to +85°C, VCC = 1.8V to 3.3V)

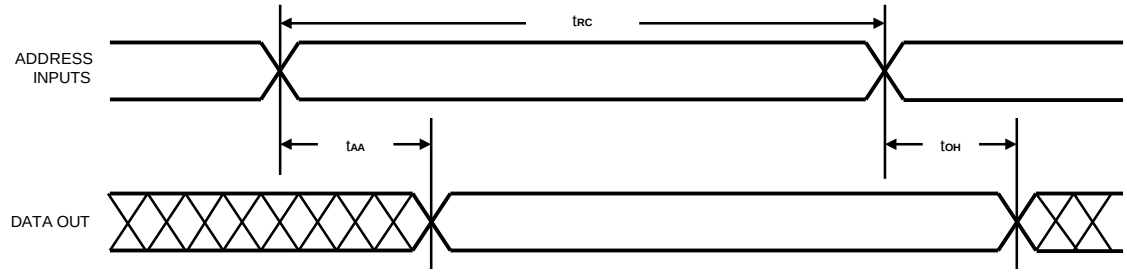
Symbol	Parameter	Min.	Max.	Unit
Read Cycle				
t_{RC}	Read Cycle Time	500	-	ns
t_{AA}	Address Access Time	-	450	ns
t_{ACE}	$\overline{\text{RAMCE}}$ Chip Enable Access Time	-	450	ns
t_{OE}	Output Enable to Output Valid	-	200	ns
t_{CLZ}	$\overline{\text{RAMCE}}$ Chip Enable to Output in Low Z	10	-	ns
t_{OLZ}	Output Enable to Output in Low Z	10	-	ns
t_{CHZ}	$\overline{\text{RAMCE}}$ Chip Disable to Output in High Z	-	100	ns
t_{OHZ}	Output Disable to Output in High Z	-	100	ns
t_{OH}	Output Hold from Address Change	10	-	ns
Write Cycle				
t_{WC}	Write Cycle Time	500	-	ns
t_{CW}	$\overline{\text{RAMCE}}$ Chip Enable to End of Write	220	-	ns
t_{AS}	Address Setup Time	0	-	ns
t_{AW}	Address Valid to End of Write	220	-	ns
t_{WP}	Write Pulse Width	200	-	ns
t_{WR}	Write Recovery Time	0	-	ns
t_{WHZ}	Write to Output in High Z	-	100	ns
t_{DW}	Data to Write Time Overlap	100	-	ns
t_{DH}	Data Hold from Write Time	0	-	ns
t_{OW}	Output Active from End of Write	10	-	ns

Notes: t_{CHZ}, t_{OHZ} and t_{WHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.

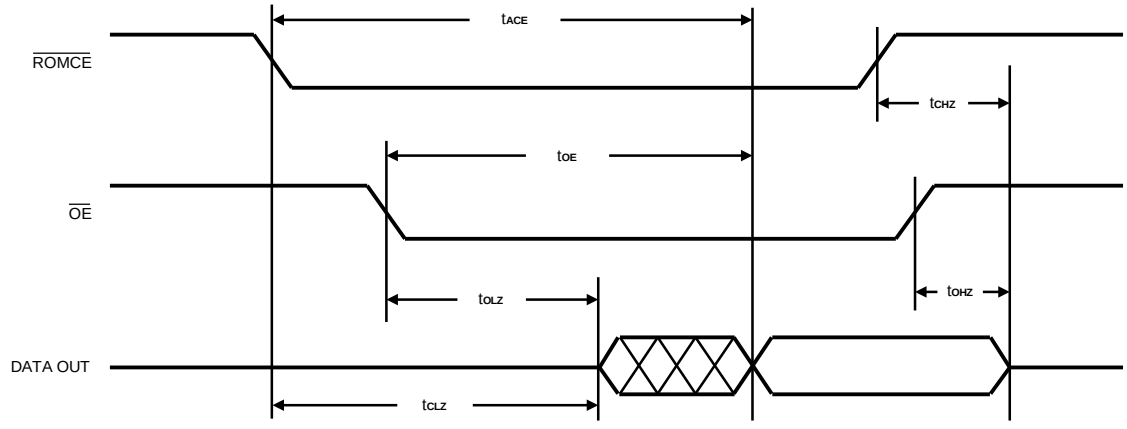
Timing Waveforms (ROM/SRAM Selection)

Timing Waveforms (ROM Selected)

Read from Address ($\overline{ROMCE}$ = Active, $\overline{OE}$ = Active)

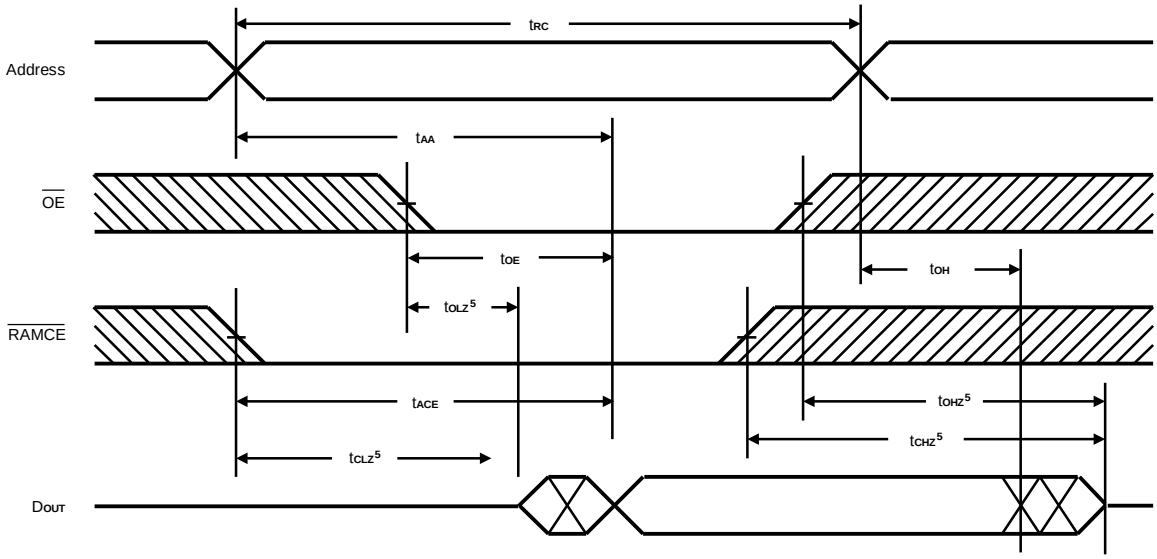


Read from $\overline{ROMCE}$ Chip Enable or Output Enable (Address Valid)

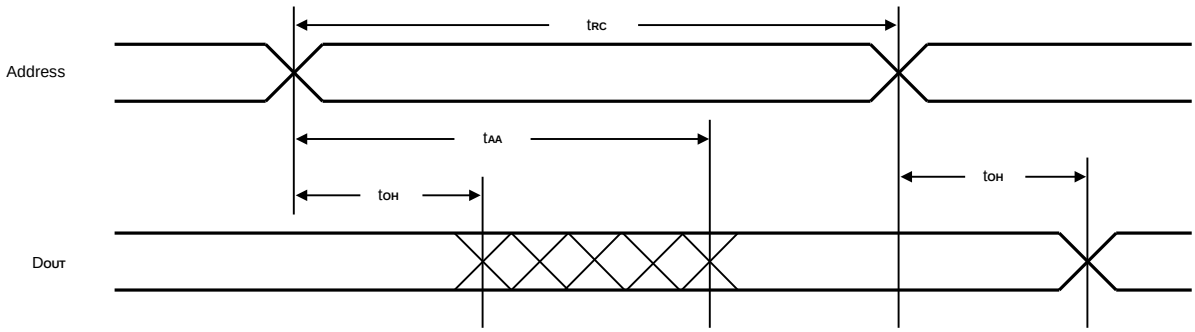


Timing Waveforms (SRAM Selected)

Read Cycle 1 (1)

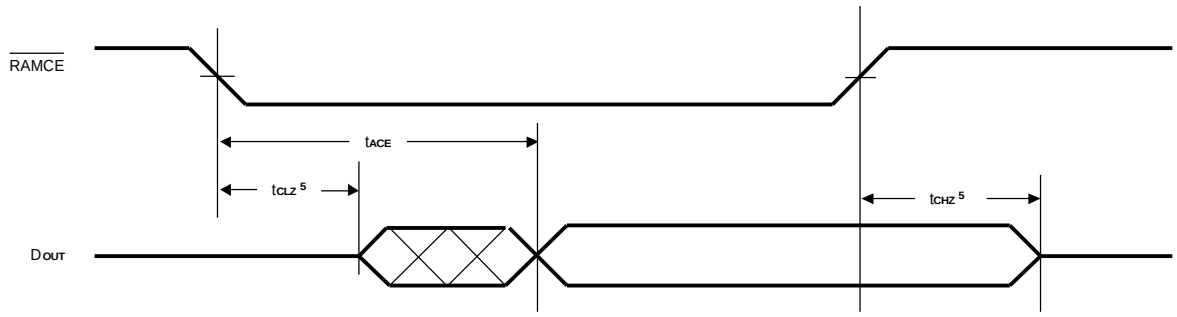


Read Cycle 2 (1, 2, 4)



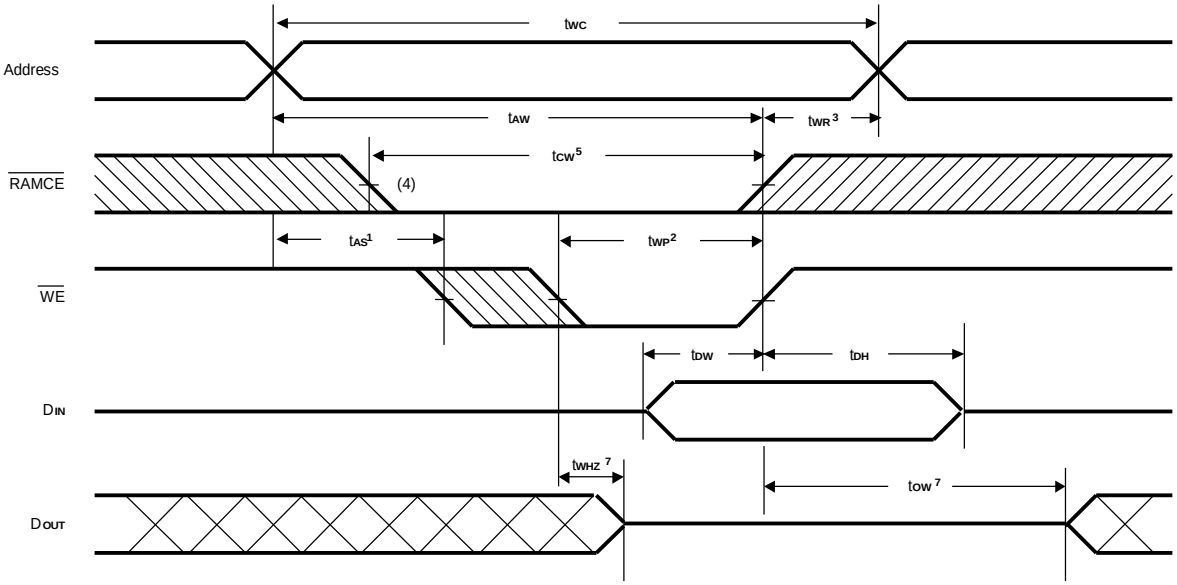
Timing Waveforms (SRAM Selected continued)

Read Cycle 3 (1, 3, 4)



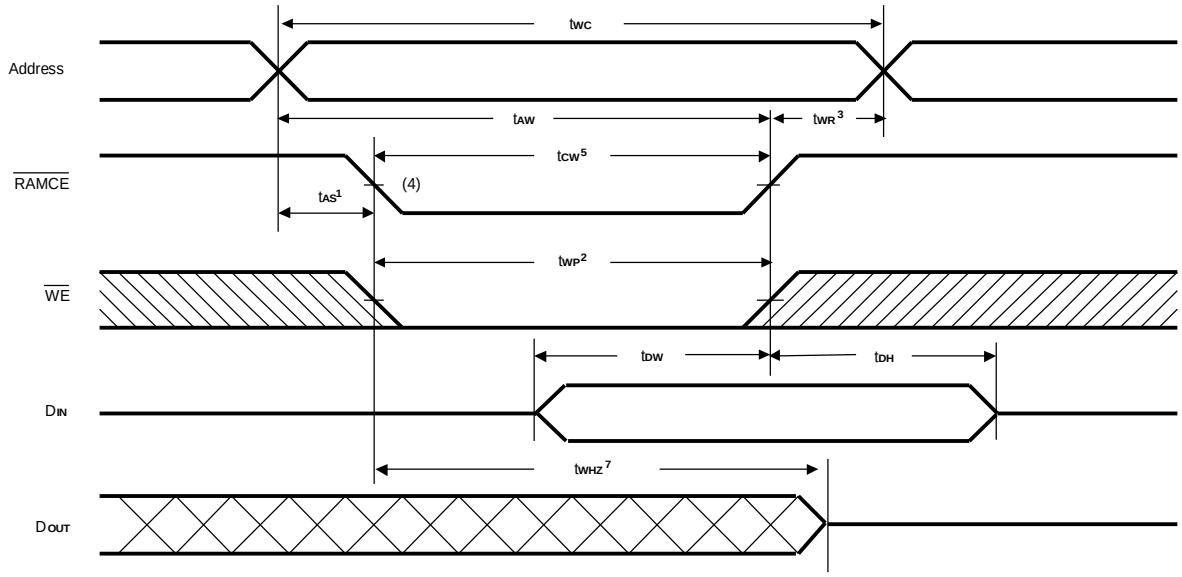
Notes: 1. $\overline{WE}$ is high for Read Cycle.
2. Device is continuously enabled, $\overline{RAMCE}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{RAMCE}$ transition low.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.

Write Cycle 1(6)
(Write Enable Controlled)



Timing Waveforms (SRAM Selected continued)

Write Cycle 2 [6]
(Chip Enable Controlled)



Notes: 1. t_{AS} is measured from the address valid to the beginning of Write.
2. A Write occurs during the overlap (t_{WP}) of a low $\overline{RAMCE}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earliest of $\overline{RAMCE}$ or $\overline{WE}$ going high to the end of the Write cycle.
4. If the $\overline{RAMCE}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
5. t_{CW} is measured from the later of $\overline{RAMCE}$ going low to the end of Write.
6. $\overline{OE}$ level is high or low.
7. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.

AC Test Conditions

Input Pulse Levels	0V, VCC
Input Rise And Fall Time	3 ns
Input and Output Timing Reference Levels	VCC/2
Output Load	See Figure 1

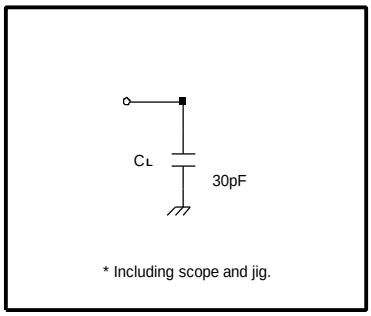
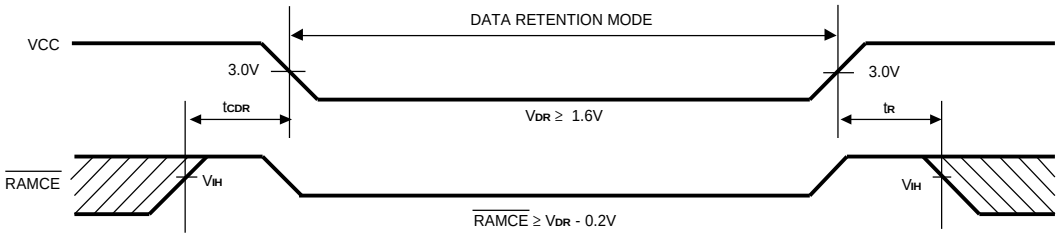


Figure 1. Output Load

Data Retention Characteristics (T_A = -25°C to 85°C)

Symbol	Parameter	Min.	Max.	Unit	Conditions
V_{DR}	VCC for Data Retention	1.6	3.6	V	$\overline{RAMCE}$ ≥ VCC - 0.2V
I_{CCDR}	Data Retention Current	-	3	µA	VCC = 1.6V, $\overline{RAMCE}$ ≥ VCC - 0.2V V_{IN} ≥ 0V
t_{CDR}	Chip Disable to Data Retention Time	0	-	ns	See Retention Waveform
t_R	Operation Recovery Time	t_{RC}	-	ns	

Low VCC Data Retention Waveform



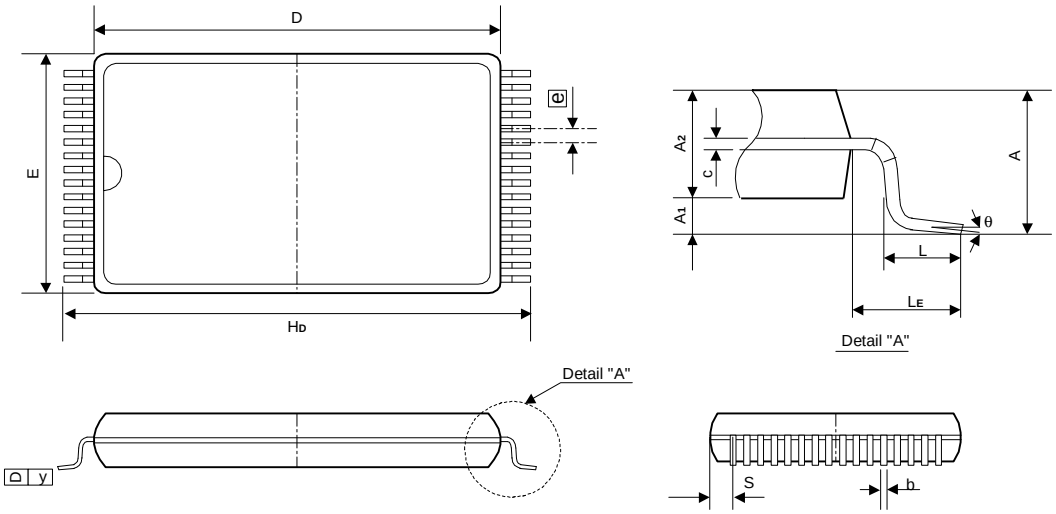
Ordering Information

Part No.	Access Time (ns)	Operation Current Max. (mA)	Standby Current Max. (mA)	Package
A26E001AV	450	4	10	32L TSOP
A26E001AX	450	4	10	32L sTSOP

Package Information

TSOP 32L TYPE I (8 X 20mm) Outline Dimensions

unit: inches/mm



Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.047	-	-	1.20
A_1	0.002	-	0.006	0.05	-	0.15
A_2	0.037	0.039	0.041	0.95	1.00	1.05
b	0.007	0.009	0.011	0.18	0.22	0.27
c	0.004	-	0.008	0.11	-	0.20
D	0.720	0.724	0.728	18.30	18.40	18.50
E	-	0.315	0.319	-	8.00	8.10
e	0.020 BSC			0.50 BSC		
H_D	0.779	0.787	0.795	19.80	20.00	20.20
L	0.016	0.020	0.024	0.40	0.50	0.60
L_E	-	0.032	-	-	0.80	-
S	-	-	0.020	-	-	0.50
y	-	-	0.003	-	-	0.08
θ	0°	-	5°	0°	-	5°

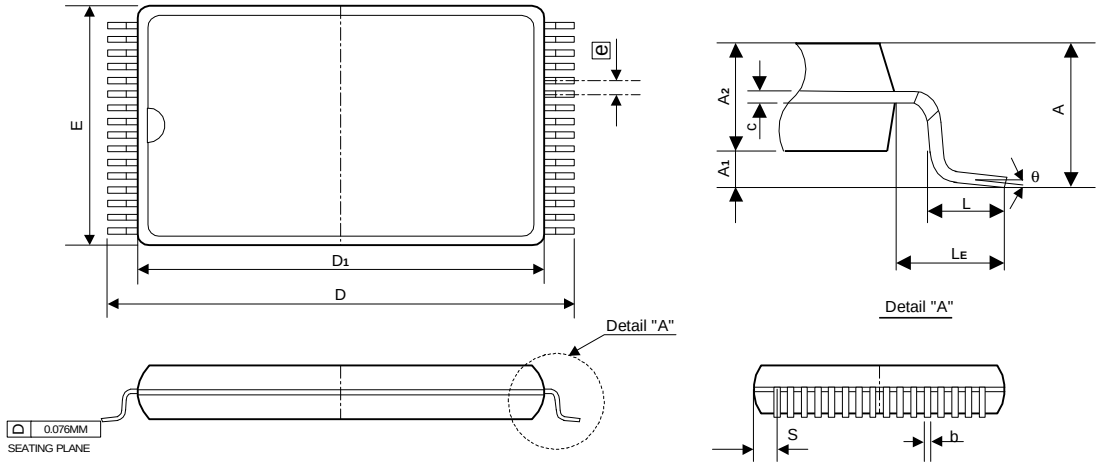
Notes:

1. The maximum value of dimension D includes end flash.
2. Dimension E does not include resin fins.
3. Dimension S includes end flash.

Package Information

sTSOP 32L TYPE I (8 X 13.4mm) Outline Dimensions

unit: inches/mm



Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.049	-	-	1.25
A_1	0.002	-	-	0.05	-	-
A_2	0.037	0.039	0.041	0.95	1.00	1.05
b	0.007	0.008	0.009	0.17	0.20	0.23
c	0.0056	0.0059	0.0062	0.142	0.150	0.158
E	0.311	0.315	0.319	7.90	8.00	8.10
e	0.020 TYP			0.50 TYP		
D	0.520	0.528	0.535	13.20	13.40	13.60
D_1	0.461	0.465	0.469	11.70	11.80	11.90
L	0.012	0.020	0.028	0.30	0.50	0.70
L_E	0.0275	0.0315	0.0355	0.700	0.800	0.900
S	0.0109 TYP			0.278 TYP		
θ	0°	3°	5°	0°	3°	5°

Notes:
1. The maximum value of dimension D_1 includes end flash.
2. Dimension E does not include resin fins.
3. Dimension S includes end flash.