Document Title

LCD Controller-Driver

Revision History

Rev. No.	History	Issue Date	Remark
0.0	Initial issue	April 20, 2000	Preliminary
0.1	Error correction: C3- → C3+ C1+ → C1- C1- → C1+ C2- → C2+ C2+ → C2- Add pad coordinates Change power supply range: 2.0V to 5.5V → 2.4V to 5.5V	February 19, 2001	

A31W65132 Series

Preliminary

LCD Controller-Driver

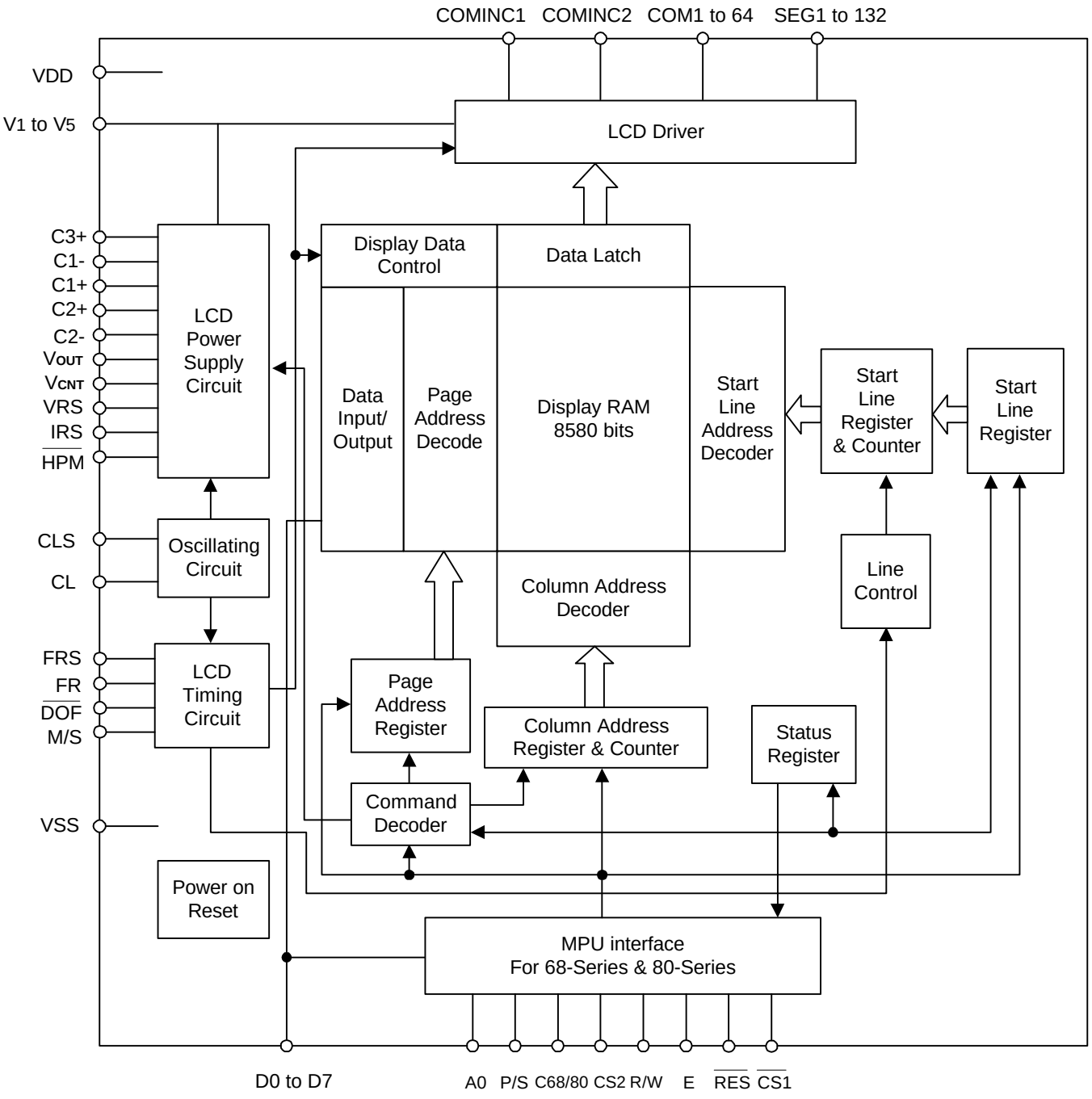
Features

- Power supply range : 2.4V to 5.5V
  6.0V to 16.5V (LCD drive)
- Internal LCD drivers :
  132 segment signal drivers
  65 commons signal drivers
- Power save current (<1uA)
- On chip 132 x 65 Display Data RAM
- 8 BIT 80/68-Series Parallel interface ,Serial interface
- Build-in RC oscillator or external clock input
- 1:7 / 1:9 Bias Ratio
- 64 level internal contrast control
- 8 level internal resistor ratio set (V5 voltage)
- Build-in temperature compensation circuit
- Internal bias divider circuit
- On chip internal DC/DC converter / External Power supply
- Dual/ Triple/ Quad booster
- Internal icon common Output system for indicators
- TCP package, Gold bumps

The A31W65132 series is a CMOS LCD driver, which has 132 segment, and 65 common graphic display. It has 80/68-series 8 bit parallel and serial interface capability for operating with general CPU. The internal 65 x 132 display data RAM makes the display of both graphics and characters possible. Besides the general LCD driver features, it has on chip LCD bias divider circuit such that minimize external component required in system application.

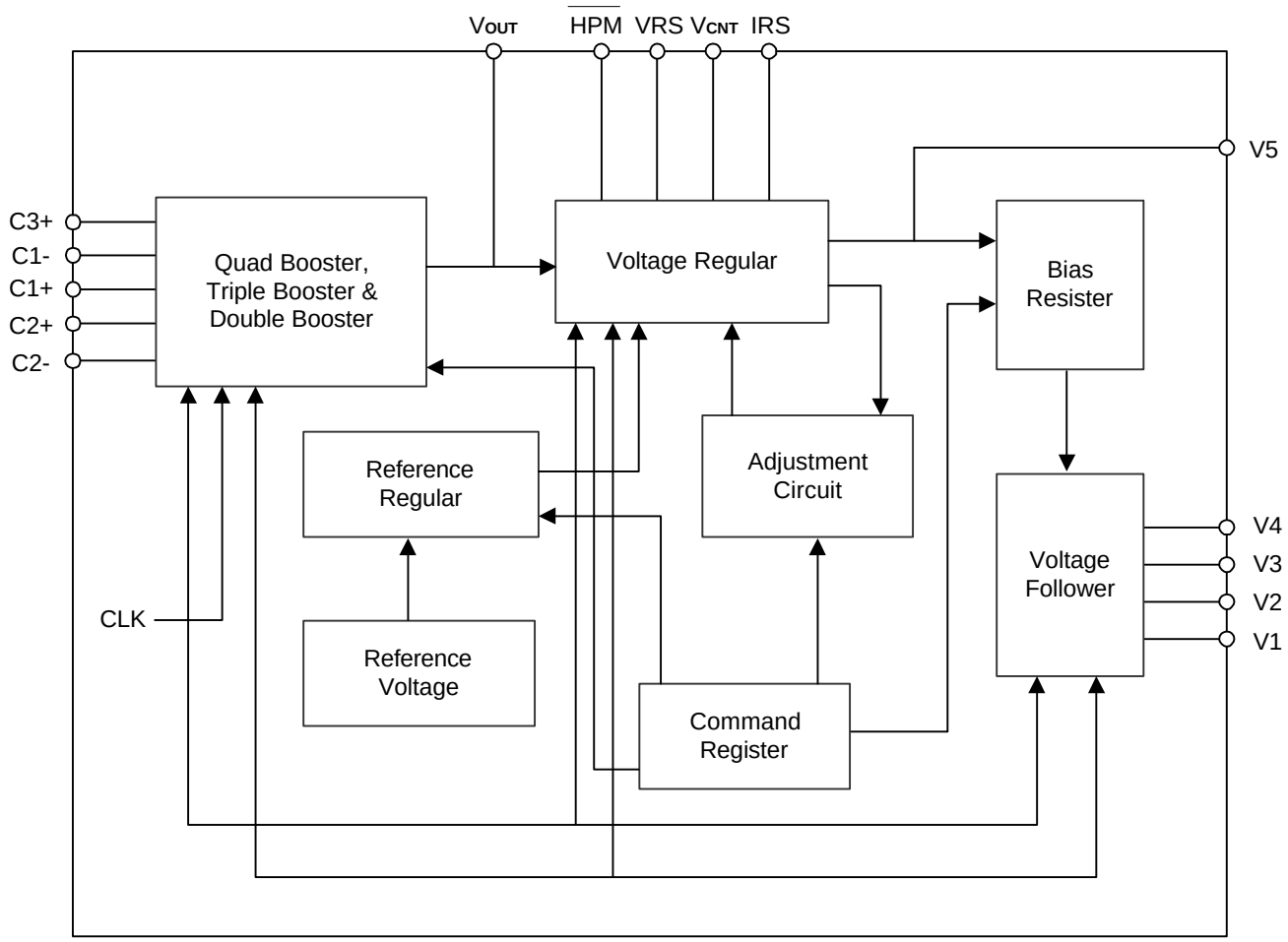
Block Diagram

1. Block Overview

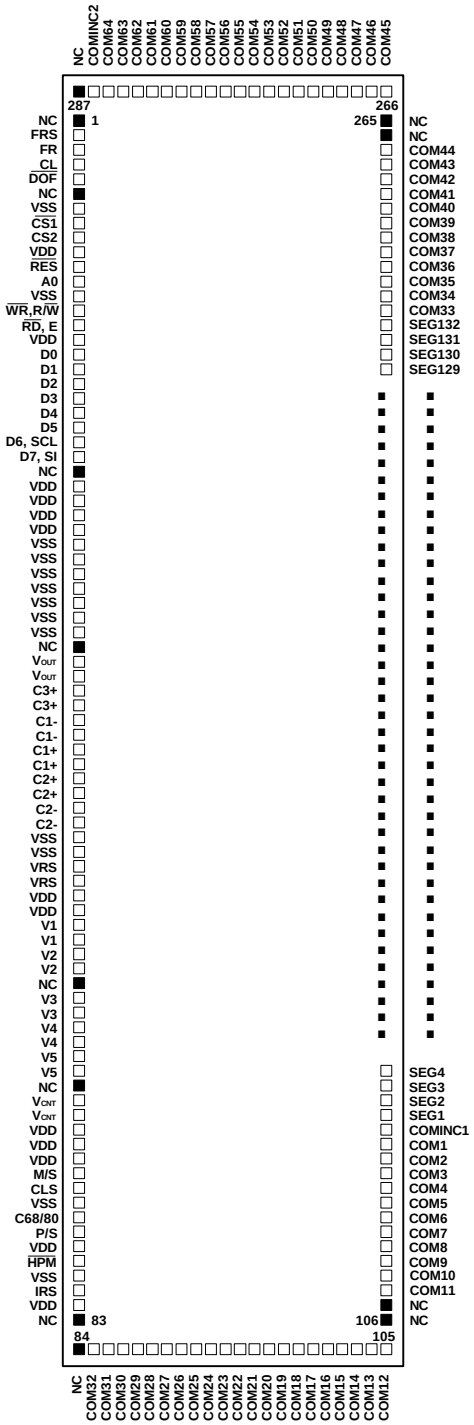


Block Diagram

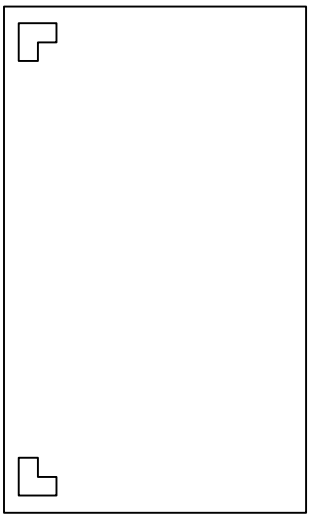
2. LCD Power Supply Circuit Block Diagram



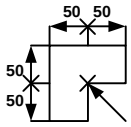
Pad Assignment



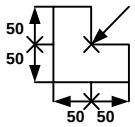
Chip Identification Marks



(The identification marks are larger than the actual scaling)



Unit : um



(The identification marks are made of Al patterns)

. Pad pitch
  - Segment driver 65um
  - Comon driver 65um
  - Control pad 100um

. Gold bump size
  - Drive 43x85um
  - Input pin 73x85um

. Gold bump height 18um (Typ.)

Pad Coordinates

Unit: μm (The origin is the center of the chip)

No.	Pin Name	X	Y	No.	Pin Name	X	Y
1	NC	-5152.5	-910	49	C2-	1684.4	-910
2	FRS	-4971.2	-910	50	VSS	1784.4	-910
3	FR	-4706	-910	51	VSS	1884.4	-910
4	CL	-4445.8	-910	52	VRS	1984.4	-910
5	$\overline{DOF}$	-4180.6	-910	53	VRS	2084.4	-910
6	NC	-3999.3	-910	54	VDD	2184.4	-910
7	VSS	-3899.3	-910	55	VDD	2284.4	-910
8	$\overline{CS1}$	-3785.7	-910	56	V1	2384.4	-910
9	CS2	-3685.7	-910	57	V1	2484.4	-910
10	VDD	-3572.7	-910	58	V2	2584.4	-910
11	$\overline{RES}$	-3459.7	-910	59	V2	2684.4	-910
12	A0	-3359.7	-910	60	NC	2784.4	-910
13	VSS	-3246.7	-910	61	V3	2884.4	-910
14	$\overline{W/R}$, R/$\overline{W}$	-3133.7	-910	62	V3	2984.4	-910
15	$\overline{RD}$, E	-3033.7	-910	63	V4	3084.4	-910
16	VDD	-2920.7	-910	64	V4	3184.4	-910
17	D0	-2739.1	-910	65	V5	3284.4	-910
18	D1	-2473.9	-910	66	V5	3384.4	-910
19	D2	-2213.7	-910	67	NC	3484.4	-910
20	D3	-1948.1	-910	68	V_{CNT}	3584.4	-910
21	D4	-1687.9	-910	69	V_{CNT}	3684.4	-910
22	D5	-1422.7	-910	70	VDD	3784.4	-910
23	D6, SCL	-1162.5	-910	71	VDD	3884.4	-910
24	D7, SI	-896.9	-910	72	VDD	3984.4	-910
25	NC	-715.6	-910	73	M/S	4097.4	-910
26	VDD	-615.6	-910	74	CLS	4197.4	-910
27	VDD	-515.6	-910	75	VSS	4310.4	-910
28	VDD	-415.6	-910	76	C68/80	4423.4	-910
29	VDD	-315.6	-910	77	P/S	4523.4	-910
30	VSS	-215.6	-910	78	VDD	4636.4	-910
31	VSS	-115.6	-910	79	$\overline{HPM}$	4736.4	-910
32	VSS	-15.6	-910	80	VSS	4836.4	-910
33	VSS	84.4	-910	81	IRS	4936.4	-910
34	VSS	184.4	-910	82	VDD	5036.4	-910
35	VSS	284.4	-910	83	NC	5136.4	-910
36	VSS	384.4	-910	84	NC	5146.5	-726.3
37	NC	484.4	-910	85	COM32	5146.5	-661.3
38	V_{OUT}	584.4	-910	86	COM31	5146.5	-596.3
39	V_{OUT}	684.4	-910	87	COM30	5146.5	-531.3
40	C3+	784.4	-910	88	COM29	5146.5	-466.3
41	C3+	884.4	-910	89	COM28	5146.5	401.3
42	C1-	984.4	-910	90	COM27	5146.5	-336.3
43	C1-	1084.4	-910	91	COM26	5146.5	-271.3
44	C1+	1184.4	-910	92	COM25	5146.5	-206.3
45	C1+	1284.4	-910	93	COM24	5146.5	-141.3
46	C2+	1384.4	-910	94	COM23	5146.5	-76.3
47	C2+	1484.4	-910	95	COM22	5146.5	-11.3
48	C2-	1584.4	-910	96	COM21	5146.5	53.7

Pad Coordinates (continued)

Unit: µm (The origin is the center of the chip)

No.	Pin Name	X	Y	No.	Pin Name	X	Y
97	COM20	5146.5	118.7	145	SEG26	2632.5	910
98	COM19	5146.5	183.7	146	SEG27	2567.5	910
99	COM18	5146.5	248.7	147	SEG28	2502.5	910
100	COM17	5146.5	313.7	148	SEG29	2437.5	910
101	COM16	5146.5	378.7	149	SEG30	2372.5	910
102	COM15	5146.5	443.7	150	SEG31	2307.5	910
103	COM14	5146.5	508.7	151	SEG32	2242.5	910
104	COM13	5146.5	573.7	152	SEG33	2177.5	910
105	COM12	5146.5	638.7	153	SEG34	2112.5	910
106	NC	5167.5	910	154	SEG35	2047.5	910
107	NC	5102.5	910	155	SEG36	1982.5	910
108	COM11	5037.5	910	156	SEG37	1917.5	910
109	COM10	4972.5	910	157	SEG38	1852.5	910
110	COM9	4907.5	910	158	SEG39	1787.5	910
111	COM8	4842.5	910	159	SEG40	1722.5	910
112	COM7	4777.5	910	160	SEG41	1657.5	910
113	COM6	4712.5	910	161	SEG42	1592.5	910
114	COM5	4647.5	910	162	SEG43	1527.5	910
115	COM4	4582.5	910	163	SEG44	1462.5	910
116	COM3	4517.5	910	164	SEG45	1397.5	910
117	COM2	4452.5	910	165	SEG46	1332.5	910
118	COM1	4387.5	910	166	SEG47	1267.5	910
119	COMINC1	4322.5	910	167	SEG48	1202.5	910
120	SEG1	4257.5	910	168	SEG49	1137.5	910
121	SEG2	4192.5	910	169	SEG50	1072.5	910
122	SEG3	4127.5	910	170	SEG51	1007.5	910
123	SEG4	4062.5	910	171	SEG52	942.5	910
124	SEG5	3997.5	910	172	SEG53	877.5	910
125	SEG6	3932.5	910	173	SEG54	812.5	910
126	SEG7	3867.5	910	174	SEG55	747.5	910
127	SEG8	3802.5	910	175	SEG56	682.5	910
128	SEG9	3737.5	910	176	SEG57	617.5	910
129	SEG10	3672.5	910	177	SEG58	552.5	910
130	SEG11	3607.5	910	178	SEG59	487.5	910
131	SEG12	3542.5	910	179	SEG60	422.5	910
132	SEG13	3477.5	910	180	SEG61	357.5	910
133	SEG14	3412.5	910	181	SEG62	292.5	910
134	SEG15	3347.5	910	182	SEG63	227.5	910
135	SEG16	3282.5	910	183	SEG64	162.5	910
136	SEG17	3217.5	910	184	SEG65	97.5	910
137	SEG18	3152.5	910	185	SEG66	32.5	910
138	SEG19	3087.5	910	186	SEG67	-32.5	910
139	SEG20	3022.5	910	187	SEG68	-97.5	910
140	SEG21	2957.5	910	188	SEG69	-162.5	910
141	SEG22	2892.5	910	189	SEG70	-227.5	910
142	SEG23	2827.5	910	190	SEG71	-292.5	910
143	SEG24	2762.5	910	191	SEG72	-357.5	910
144	SEG25	2697.5	910	192	SEG73	-422.5	910

Pad Coordinates (continued)

Unit: µm (The origin is the center of the chip)

No.	Pin Name	X	Y
193	SEG74	-487.5	910
194	SEG75	-552.5	910
195	SEG76	-617.5	910
196	SEG77	-682.5	910
197	SEG78	-747.5	910
198	SEG79	-812.5	910
199	SEG80	-877.5	910
200	SEG81	-942.5	910
201	SEG82	-1007.5	910
202	SEG83	-1072.5	910
203	SEG84	-1137.5	910
204	SEG85	-1202.5	910
205	SEG86	-1267.5	910
206	SEG87	-1332.5	910
207	SEG88	-1397.5	910
208	SEG89	-1462.5	910
209	SEG90	-1527.5	910
210	SEG91	-1592.5	910
211	SEG92	-1657.5	910
212	SEG93	-1722.5	910
213	SEG94	-1787.5	910
214	SEG95	-1852.5	910
215	SEG96	-1917.5	910
216	SEG97	-1982.5	910
217	SEG98	-2047.5	910
218	SEG99	-2112.5	910
219	SEG100	-2177.5	910
220	SEG101	-2242.5	910
221	SEG102	-2307.5	910
222	SEG103	-2372.5	910
223	SEG104	-2437.5	910
224	SEG105	-2502.5	910
225	SEG106	-2567.5	910
226	SEG107	-2632.5	910
227	SEG108	-2697.5	910
228	SEG109	-2762.5	910
229	SEG110	-2827.5	910
230	SEG111	-2892.5	910
231	SEG112	-2957.5	910
232	SEG113	-3022.5	910
233	SEG114	-3087.5	910
234	SEG115	-3152.5	910
235	SEG116	-3217.5	910
236	SEG117	-3282.5	910
237	SEG118	-3347.5	910
238	SEG119	-3412.5	910
239	SEG120	-3477.5	910
240	SEG121	-3542.5	910

No.	Pin Name	X	Y
241	SEG122	-3607.5	910
242	SEG123	-3672.5	910
243	SEG124	-3737.5	910
244	SEG125	-3802.5	910
245	SEG126	-3867.5	910
246	SEG127	-3932.5	910
247	SEG128	-3997.5	910
248	SEG129	-4062.5	910
249	SEG130	-4127.5	910
250	SEG131	-4192.5	910
251	SEG132	-4257.5	910
252	COM33	-4322.5	910
253	COM34	-4387.5	910
254	COM35	-4452.5	910
255	COM36	-4517.5	910
256	COM37	-4582.5	910
257	COM38	-4647.5	910
258	COM39	-4712.5	910
259	COM40	-4777.5	910
260	COM41	-4842.5	910
261	COM42	-4907.5	910
262	COM43	-4972.5	910
263	COM44	-5037.5	910
264	NC	-5102.5	910
265	NC	-5167.5	910
266	COM45	-5146.5	638.7
267	COM46	-5146.5	573.7
268	COM47	-5146.5	508.7
269	COM48	-5146.5	443.7
270	COM49	-5146.5	378.7
271	COM50	-5146.5	313.7
272	COM51	-5146.5	248.7
273	COM52	-5146.5	183.7
274	COM53	-5146.5	118.7
275	COM54	-5146.5	53.7
276	COM55	-5146.5	-11.3
277	COM56	-5146.5	-76.3
278	COM57	-5146.5	-141.3
279	COM58	-5146.5	-206.3
280	COM59	-5146.5	-271.3
281	COM60	-5146.5	-336.3
282	COM61	-5146.5	-401.3
283	COM62	-5146.5	-466.3
284	COM63	-5146.5	-531.3
285	COM64	-5146.5	-596.3
286	COMINC2	-5146.5	-661.3
287	NC	-5146.5	-726.3

Input/Output Pin Function

<table>
<tr><th>Pin No.</th><th>Symbol</th><th>Type</th><th>Description</th></tr>
<tr><td>7, 13,
30-36,
50-51,
75, 80</td><td>VSS</td><td>Supply</td><td>GROUND</td></tr>
<tr><td>10, 16,
26-29,
54-55,
70-72,
78, 82</td><td>VDD</td><td>Supply</td><td>Power supply pin</td></tr>
<tr><td>52-53</td><td>VRS</td><td>Supply</td><td>External VREG voltage supply for LCD voltage regulator.</td></tr>
<tr><td>74</td><td>CLS</td><td>Input</td><td>CLS = High : Internal oscillator is enabled
CLS = Low : Internal oscillator is disabled</td></tr>
<tr><td>4</td><td>CL</td><td>In/out</td><td>Display clock input
<table>
<tr><th>M/S</th><th>CLS</th><th>CL</th></tr>
<tr><td>H</td><td>H</td><td>Output</td></tr>
<tr><td>H</td><td>L</td><td>Input</td></tr>
<tr><td>L</td><td>H</td><td>Input</td></tr>
<tr><td>L</td><td>L</td><td>Input</td></tr>
</table>
The CL pins must be connected in Master/Slave mode.</td></tr>
<tr><td>73</td><td>M/S</td><td>Input</td><td>M/S = High : Master mode
M/S = Low : Slave mode
<table>
<tr><th>M/S</th><th>CLS</th><th>Power Supply Circuit</th><th>Oscillator Circuit</th><th>CL</th><th>FR</th><th>$\overline{DOF}$</th><th>FRS</th></tr>
<tr><td>H</td><td>H</td><td>Enable</td><td>Enable</td><td>Output</td><td>Output</td><td>Output</td><td>Output</td></tr>
<tr><td>H</td><td>L</td><td>Enable</td><td>Disable</td><td>Input</td><td>Output</td><td>Output</td><td>Output</td></tr>
<tr><td>L</td><td>H</td><td>Disable</td><td>Disable</td><td>Input</td><td>Input</td><td>Input</td><td>Output</td></tr>
<tr><td>L</td><td>L</td><td>Disable</td><td>Disable</td><td>Input</td><td>Input</td><td>Input</td><td>Output</td></tr>
</table>
The signals FR, $\overline{DOF}$, CL of slave chips must be supplied from the master chip.</td></tr>
<tr><td>3</td><td>FR</td><td>In/out</td><td>LC alternating current signal pin
M/S = High : Output
M/S = Low : Input
The FR pins must be connected in Master/Slave mode.</td></tr>
<tr><td>5</td><td>$\overline{DOF}$</td><td>In/out</td><td>LCD blanking control pin
M/S = High : Output
M/S = Low : Input
The $\overline{DOF}$ pins must be connected in Master/Slave mode</td></tr>
<tr><td>2</td><td>FRS</td><td>Output</td><td>The FRS output for the static icon drive and is used in conjunction with the FR pin, one of the static icon electrodes is connected to the FR pin, and the other is connected to FRS pin.</td></tr>
</table>

Input/Output Pin Function (continued)

Pin No.	Symbol	Type	Description
81	IRS	Input	The IRS is used in V5 voltage adjustment IRS = High : used the internal resistors IRS = Low : used the external resistors This pin is used in master mode. When in slave mode, it can fixed to either High or Low level
79	$\overline{HPM}$	Input	$\overline{HPM}$ = High : Normal mode power supply $\overline{HPM}$ = Low : High power mode power supply This pin is used in master mode. When in slave mode, it can fixed to either High or Low level
8, 9	$\overline{CS1}$ CS2	Input	Chip select input. When $\overline{CS1}$ = Low, CS2 = High, enable the chip select
11	$\overline{RES}$	Input	Reset pin, Low enable
12	A0	Input	A0=Low: Command input. A0=High: Display data input and outputs
14	R/$\overline{W}$ ($\overline{WR}$)	Input	68-Series R/$\overline{W}$=High: Read, R/$\overline{W}$=Low : Write 80-Series : Write enable, Active Low
15	E ($\overline{RD}$)	Input	68-Series : Enable clock signal input, Active High 80-Series : Read enable, Active Low
77	P/S	Input	Parallel/serial interface select input High : 8-bit parallel interface Low : Serial interface , display data RAM reading is not supported
76	C68/80	Input	Microprocessor interface select input High : 68-Series interface is selected Low : 80-Series interface is selected
17-24	D0-7 (SI, SCL)	Input/ Output	8bit bi-directional data bus to be connected to microprocessor's data bus P/S = High : 8-bit configuration data bus connection P/S = Low : Serial interface connection D6 Serial data input SCL D7 Serial clock input SI
120-251	SEG1- SEG132	Output	Provide the LCD segment driving signal
85-105, 108-118, 252-263, 266-285	COM1- COM64	Output	Provide the LCD common driving signal
119, 286	COMINC1 COMINC2	Output	Provide the icon common driving signal, the same signal is output in master/slave mode
38-39	V_{OUT}	Output	Boosting voltage output
40-41	C3+	Input	3rd- step boosting capacitor negative connection

Input/Output Pin Function (continued)

<table>
<tr><th>Pin No.</th><th>Symbol</th><th>Type</th><th>Description</th></tr>
<tr><td>46-47</td><td>C2+</td><td>Input</td><td>2nd-step boosting capacitor negative connection</td></tr>
<tr><td>48-49</td><td>C2-</td><td>Input</td><td>2nd-step boosting capacitor positive connection</td></tr>
<tr><td>44-45</td><td>C1+</td><td>Input</td><td>1 st-step boosting capacitor negative connection</td></tr>
<tr><td>42-43</td><td>C1-</td><td>Input</td><td>1 st-step boosting capacitor positive connection</td></tr>
<tr><td>68-69</td><td>VCNT</td><td>Input</td><td>External LCD power regulator voltage control through a resistive voltage divider.
IRS = Low: These can be used, because the internal resistors are disabled.
IRS = High: These can not be used.</td></tr>
<tr><td>56-57</td><td>V1</td><td>Input</td><td rowspan="5">LCD driver bias voltage. They can be supplied externally or generated by the internal bias divider.
<table><tr><th></th><th>1: 7 bias</th><th>1: 9 bias</th></tr><tr><td>V1</td><td>1/7 x V5</td><td>1/9 x V5</td></tr><tr><td>V2</td><td>2/7 x V5</td><td>2/9 x V5</td></tr><tr><td>V3</td><td>5/7 x V5</td><td>7/9 x V5</td></tr><tr><td>V4</td><td>6/7 x V5</td><td>8/9 x V5</td></tr></table>• Inputs LCD drive bias voltage when using an external LCD power supply circuit.
V5 ≥ V4, V3, V2, V1 > VSS</td></tr>
<tr><td>58-59</td><td>V2</td><td>Input</td></tr>
<tr><td>61-62</td><td>V3</td><td>Input</td></tr>
<tr><td>63-64</td><td>V4</td><td>Input</td></tr>
<tr><td>65-66</td><td>V5</td><td>Input</td></tr>
<tr><td>1, 6, 25, 37, 60, 67, 83-84 , 106-107, 264-265, 287</td><td>NC</td><td>Open</td><td>No Connection</td></tr>
</table>

Commands Table

Command	Bit pattern											Comment
	A0	E	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0	
Set Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0 1	D0:0 Display OFF: Display goes out, regardless of the content of the display data RAM D0:1 Display ON: Normal Display
Set Display Start Line	0	1	0	0	1	Display start line address (0-63)						Sets the line address of the display data RAM output to COM1
Page Address Set	0	1	0	1	0	1	1	Page Address (0-8)				Sets the page address of the display data RAM. Page 8 is assigned to the icon display
Upper 4 bits of Column Address Set	0	1	0	0	0	0	1	Upper 4 bits of Column Address				Sets upper 4 bits of the display data RAM Column Address
Lower 4 bits of the Column Address Set	0	1	0	0	0	0	0	Lower 4 bits of the Column Address				Lower 4 bits of display data RAM column Address
Status Read	0	0	1	Status								Status Read
Display Data Write	1	1	0	Write Data in Display Data RAM								Writes data of D0 to D7 in the display data RAM
Display Data Read	1	0	1	Read Data from Display Data RAM								Reads data from D0 to D7 from the display data RAM
ADC Select	0	1	0	1	0	1	0	0	0	0	0 1	Reverses upper or lower display data RAM column address D0:0 Normal: Column addresses 00 to 83H correspond to segment outputs 1 to 132 D0:1 Reverse: Column addresses 00 to 83H correspond to segment outputs 132 to 1
Display Normal/ Reverse	0	1	0	1	0	1	0	0	1	1	0 1	D0:0 Normal : "1" makes the display be lit D0:1 Reverse : "0" makes the display be lit The icon display is not reversed
Display All-Lit ON/OFF	0	1	0	1	0	1	0	0	1	0	0 1	D0:0 Normal Display D0:1 Display All-Lit ON
Common Output Sequence Select	0	1	0	1	1	0	0	0 1	*	*	*	D3:0 In a normal order COM1 to COM64 D3:1 In a reverse order COM64 to COM1
Read Modify Write	0	1	0	1	1	1	0	0	0	0	0	Increments display data RAM column address only during writing
End	0	1	0	1	1	1	0	1	1	1	0	Read Modify Write Release.
Icon Only Display	0	1	0	1	1	0	1	1	0 1	Boosting Control Data		D2:0 Normal Display (default) D2:1 Icon Only Display Boosting control data: D1 D0: 00 Fosc 01 fosc/2 10 fosc/4 (default) 11 fosc/8

Commands Table (continued)

Command	Bit pattern											Comment
	A0	E	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0	
Reset	0	1	0	1	1	1	0	0	0	1	0	It does not affect the contents of the display data RAM. After resetting, display starts according to the reset value: 1.Resets the display start line register to the 1st line. 2.Resets the column address counter to address 0. 3.Resets the page address counter to page 0. 4.Turns OFF the Read Modify Write. 5.Static icon off, static icon display register off. D1, D0 = 0, 0 6.Common output sequence in normal order 7.V5 voltage regulator internal resistor ratio set mode clear. D2~D0 = 1, 0, 0 8.LCD voltage command fine adjustment data D5~D0 = 1, 0, 0, 0, 0, 0
Bias Selection	0	1	0	1	0	1	0	0	0	1	0 1	D0 = 0 : 1/9 Bias Selection (default) D0 = 1 : 1/7 Bias Selection
Power Supply Circuit Operation Control	0	1	0	0	0	1	0	1	Control mode			LCD power supply circuit operation mode select
LCD Voltage Command	0	1	0	1	0	0	0	0	0	0	1	The LCD Voltage Command Fine Adjustment Data must set after the LCD Voltage Command set
LCD Voltage Command Fine Adjustment Data				*	*	0 . 1	0 . 1	0 . 1	0 . 1	0 . 1	0 . 1	Minimum value Maximum value (Total 64 level)
V5 Voltage Regulator Internal Resistor Ratio	0	1	0	0	0	1	0	0	0 . 1	0 . 1	0 . 1	Small Large Voltage regulator internal resistor (Ra/Rb) ratio, total 8 level
Static Icon Display Command Set	0	1	0	1	0	1	0	1	1	0	0 1	Static icon display command set : D0 = 0 Static icon display OFF D0 = 1 Static icon display ON (The static icon display register set command must set after the static icon display ON command set)
Static Icon Display Register Set (Double Byte Command)				*	*	*	*	*	*	Mode		Static icon display register set : D1 D0 = 0 0 :OFF 0 1 : Blinking , one second intervals 1 0 : Blinking , 0.5 second intervals 1 1 : ON
Reference Voltage Temperature Coefficient Select	0	1	0	1	1	1	0	0	1	0 1	0 1	D0 : 0 0.05%/°C (default) D0 : 1 0.2%/°C D1 : 0 Internal VREG (default) D1 : 1 External VREG
Power Save												Set Display OFF then set Display all-lit ON command
NOP	0	1	0	1	1	1	0	0	0	1	1	Non operation command

Operation of LCD Display Driver

1. Powering ON setting sequence

Recommended Command Setting Sequence:

(1) Set Display OFF : In order to prevent unnecessary characters from being displayed during powering ON of the power .
When the master is turned on, the oscillator circuit is operable immediately. After the powering on, it will be in All-OFF state.

(2) Set Display All-Lit OFF: Normal display operation.

(3) Set LCD Power Supply operation control

(4) Set Bias Select: 1. Bias selection setting
2. V5 voltage regulator internal resistor ratio setting
3. LCD voltage command and LCD voltage command fine adjustment data setting

(5) Set Reference Voltage Temperature Compensation Coefficient

(6) End Command Input

(7) ADC Select setting

(8) Set Display Normal/Reverse:

D0 : 0 Normal Display data "1" makes the display be lit.

D0 : 1 Reverse Display data "0" makes the display be lit.

(9) Set Display Start Line address: Changing the display start line allows for page change on the display screen as well as vertical smooth scroll.

(10) Set Common Output Sequence

(11) Icon Only Display

(12) Static Icon Display select

(13) Display Data Write: After writing the display data, the column address is automatically incremented. To write the display data in succession after setting the 1st column address to be written by the COLUMN ADDRESS SETTING command, the column address is not needed to be set each time. The icon display data is valid for only D0.
Write “L” or data to be displayed in all display data RAM before turning the display ON.

(14) Display ON

2. Set Powering OFF, Power Save Mode

Set Powering OFF sequence:

(1) Set Display OFF

(2) Set Display All-Lit ON

(3) Set LCD Power Supply Circuit OFF

Power Save Mode:

The power save mode has two modes, one is sleep mode and the other is standby mode.
The MPU is still able to access the display data RAM when in power save mode.

	Combination of Commands		State
	Display ON	Display All-Lit OFF	Normal display operation
	Display ON	Display All-Lit ON	All-lit display
	Display OFF	Display All-Lit OFF	AII-OFF
Static Icon Display ON	Display OFF	Display All-Lit ON	Standby mode (Power save)
Static Icon Display OFF	Display OFF	Display All-Lit ON	Sleep mode (Power save)

When in sleep mode, the command sleeps the system:
- Internal oscillating circuit and LCD power supply circuit are stopped.
- All LC drive circuit are stopped, the Segment and Common outputs are fixed at VSS level.

When in standby mode:
- Internal oscillating circuit continues to operate and LCD power supply circuits are stopped.
- The duty drive system LC circuits are stopped, the Segment and Common outputs are fixed at VSS level.
- The static icon drive system continues to operate.

When a reset command is set in the standby mode, the LCD system will enter the sleep mode.
When using an external power supply circuit, stop the external power supply circuit and float the LCD power supply when the power save mode is started. When using an external bias resistor in order to reduce the current of power save mode, attach a switching transistor which cuts the current flowing through the bias resistor. The LCD blinking control pin $\overline{DOF}$ will output Low signal when the power save mode is start. We can use the $\overline{DOF}$ to stop the external power supply.

3. MPU Interface Select

The parallel 68-series, 80-series interface or serial interface can be selected by P/S, C68/80 pin setup:

P/S Pin	C68/80 Pin	MPU Interface
H	L	80-series Interface selected
	H	68-series Interface selected
L	don't care	Serial Interface selected

3.1 MPU Parallel 68-Series and 80-Series Interface

The parallel interface consists of 8 bi-directional data pins (D0-D7), R/$\overline{W}$ ($\overline{WR}$), A0, E($\overline{RD}$), $\overline{CS}$ In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read.

A31W65132 Pin Name	A0	E	R/$\overline{W}$	$\overline{CS1}$	CS2	D0 - D7
68-Series MPU Signal	A0	E	R/$\overline{W}$	$\overline{CS1}$	CS2	D0 - D7
80-Series MPU Signal	A0	$\overline{RD}$	$\overline{WR}$	$\overline{CS1}$	CS2	D0 - D7

3.2 MPU Serial Interface

The serial interface consists of serial clock input SCL, serial data input SI and chip select $\overline{CS1}$, CS2, A0. When the serial interface is selected by setting P/S to “L”, the instruction code is the same as for the parallel interface .By setting $\overline{CS1}$ to “L”, CS2 to “H”. the serial interface circuit enters an operating state. And by setting $\overline{CS1}$ to “H’, or setting CS2 to “L”, it will reset the serial interface circuit and initialized the counter.
Data is input in the order of D7, D6, D5,....D0. The displayed data and commands are written at the rising edge of the SCL. The A0 is detected every 8 rising edge of SCLK serial clock after the chip select pins is enabled.

D7 (SI) : Serial Data Input
D6 (SCL) : Serial Clock Input
D5 to D0 : Open
A0 : Select the command data or display data

A0	Operation
L	Command write
H	Display data write

4. Command Execution

When the input at D0-D7 is interpreted as a command and it will be decoded and written to the corresponding command register. The user can input the commands continuously without confirming the busy flag of status command register because the command is completely executed within the cycle time (t_{CYC}) according to the timing characteristics of the command input. But that re-inputting the command within the executed cycle time is inhibited. The busy flag is outputted to D7 pin with the read instruction, "H" indicates the chip is in busy state.

5. Data Bus Select

When $\overline{CS1}$ is held at "H" level or CS2 is held at "L" level, the D0-D7 is in high impedance state.

68/80-Series shared	68-Series	80-Series		Description
A0	R/$\overline{W}$	E	R/$\overline{W}$	
1	1	0	1	Reads from Display Data RAM
1	0	1	0	Writes to Display Data RAM
0	1	0	1	Reads Status
0	0	1	0	Command Write to internal register

6. Display Data RAM

The Display Data RAM is made of dual port RAM. The size of the RAM is 64 x 132 + 132 = 8580 bits.
Write "L" or data to be displayed in all display data RAM before turning the display ON.

7. Accessing the Display Data RAM From MPU

In order to match the operating frequency of Display Data RAM with that of the MPU, a dummy read is required before the first actual display data read. When the MPU reads the Display Data RAM, the first dummy read cycle stores the first read data in the bus holder, and then at the next read cycle the MPU read the first read data from the bus holder.
It does not need a dummy cycle when MPU writes data to the Display Data RAM. When the MPU write data to Display Data RAM, once the data is stored in the bus holder, then it is written to Display Data RAM before the next data write cycle.

8. Set Column Address (higher, lower nibble)

This command specifies the column address (higher and lower nibble) of the Display Data RAM. The column address will be incremented automatically by each data access after it is pre-set by the MPU. The incrementation of column addresses stops with 83H.

9. Set Page Address (0-8)

This command positions the page address to 0 of 8 possible positions in Display Data RAM. Page 0-7 are the graphic display area, and the page 8 are the icon display area. The icon display data is valid for only D0.

10. Set display start line (0-63)

The command is used to change the display page or smooth scroll.
With the display start line value equals to 0, D0 of page 0 is mapped to COM1. The display start line values of 0 to 63 are assigned to page 0 to 7.

11. Status Read

This command shows the status of A31W65132

BUSY	: D7	=0 :	The A31W65132 is not busy
		1 :	The A31W65132 is in internal operation or reset state.
ADC	: D6	=0 :	ADC Reverse : Column addresses 00 to 7FH correspond to segment outputs 132 to 1.
		1 :	ADC Normal : Column addresses 00 to 7FH correspond to segment outputs 1 to 132.
ON/OFF	: D5	=0 :	Display ON
		1 :	Display OFF
RESET	: D4	=0 :	In normal operation state
		1 :	Internal reset operation state
PSAVE	: D3	=0 :	In normal operation state
		1 :	In Power Save state
ICON	: D2	=0 :	In normal operation state
		1 :	In icon only display state
DREV	: D1	=0 :	Display Normal
		1 :	Display Reverse
ALON	: D0	=0 :	Normal display
		1 :	Display All-Lit ON

12. Common Output sequence select

Output sequence	Common driving signal output in normal mode	Common driving signal Output in reverse mode
1	COM1	COM64
2	COM2	COM63
3	COM3	COM62
:	:	:
16	COM16	COM49
17	COM17	COM48
:	:	:
63	COM63	COM2
64	COM64	COM1

13. Icon Only Display

D2 = 0 Normal Display
D2 = 1 Icon Only Display

D1	D0	Boosting frequency
0	0	fosc
0	1	fosc/2
1	0	fosc/4
1	1	fosc/8

When D2=High, regardless of the content of the display data RAM, display icon only and LCD panel compelled to be off. When reducing the boosting frequency, the gray scale of icon display differs depending on the panel size or the value of the boosting capacitor.

14. Read Modify Write , END

Read Modify Write

This command puts the chip in read modify write mode. In this mode the column address is saved before entering the mode, and is incremented by display data write but not by display data read. During the Read Modify Write mode, all commands are usable except the Column address set command.

End

This command relieves the A31W65132 from read modify write mode. The column address that is saved before entering read modify write mode will be restored.

15. RC Oscillator Circuit

The built-in RC oscillator generates the clock for the boosting frequency, and is also used in the display timing. When using the external clock (CLS = Low or M/S = Low), the external clock is input to CL pin.

16. Reference Voltage Temperature Compensation Coefficient Select

This command is to set one out of 2 different temperature coefficients in order to match various liquid crystal temperature grades.

$$\Delta V_{REF} = \frac{|V_{REF}(T_2) - V_{REF}(T_1)|}{T_2 - T_1}$$

$T_2 > T_1$

17. The Reset Circuit

After reset by the $\overline{RES}$ pin (Low enable), the A31W65132 return to the default status as follows:

1. Display off
2. Display normal
3. ADC select normal
4. Power supply circuit operation control D2, D1, D0 = 0, 0, 0
5. Serial interface internal counter and register clear
6. LCD power supply bias rate selection = 1/9
7. All indicator lamps-on OFF (D0 = Low)
8. Power saving clear
9. V5 voltage regulator internal resistors Ra, Rb separation
10. Turn off the Read Modify Write
11. Resets the display start line register to 1st line
12. Resets the column address counter to address 0
13. Resets the page address counter to page0
14. The SEG and COM output conditions: SEG = V2/V3, COM = V1/V4. While $\overline{RES}$ = Low, the CL, FR, FRS and $\overline{DOF}$ are fixed to High, and the oscillator and display timing generator stop. The VSS level is output from SEG and COM outputs.
15. Static icon off, and static icon display register = off (D1, D0 = 0, 0)
16. Common output sequence in normal order
17. V5 voltage regulator internal resistor ratio set mode clear D2~D0 = 1, 0, 0
18. LCD voltage command fine adjustment data D5~D0 = 1, 0, 0, 0, 0, 0
19. Reference voltage temperature coefficient select 0.05%/°C
20. Icon Only Display command: Normal display, Boosting control D1, D0 = 1, 0

18. LCD Power Supply Circuit

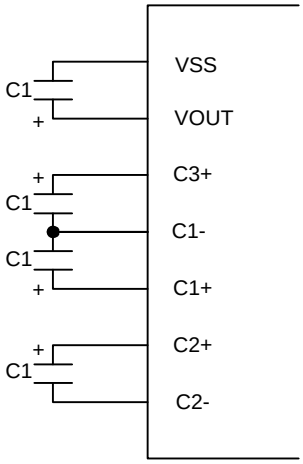
The LCD power supply circuit generates the LCD voltage needed for display output, which is controlled by power supply operation control command. It consists of:

1. Double / triple / quad DC-DC voltage converter
2. Internal resistors and voltage command fine adjustment circuit (64 level) for the V5 voltage regulator
3. LCD bias resistor and voltage follower

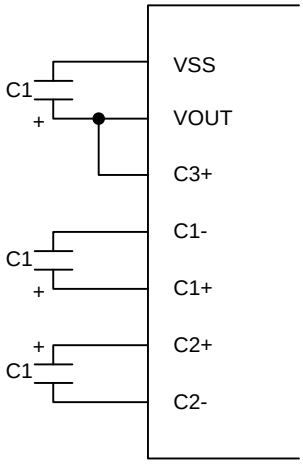
D2	D1	D0	Double/Triple/ Quad Circuit	Voltage Regulator Circuit	LCD Bias Resistor/ Voltage Follower Circuit
H	H	H	ON	ON	ON
L	L	L	OFF	OFF	OFF
L	H	H	OFF	ON	ON
L	L	H	OFF	OFF	ON

18.1 Double / Tripler / Quad

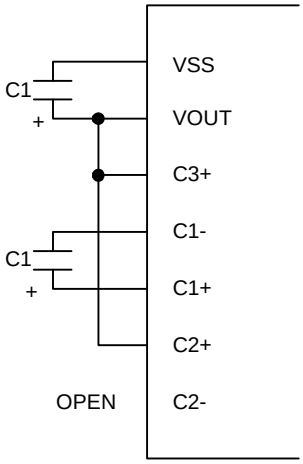
It is the 2X, 3X , 4X DC-DC voltage converter. Please refer to application notes.



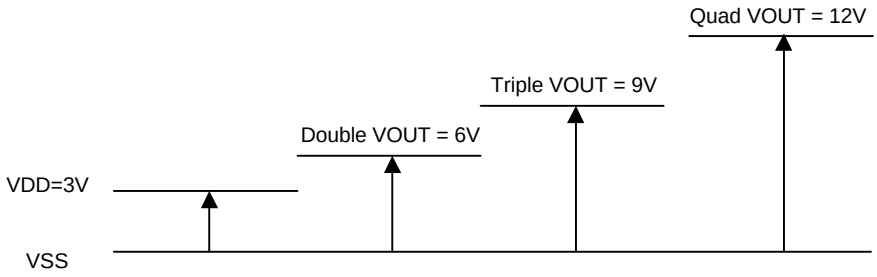
4 x step-up voltage circuit



3 x step-up voltage circuit



2 x step-up voltage circuit



Example of Booster Output

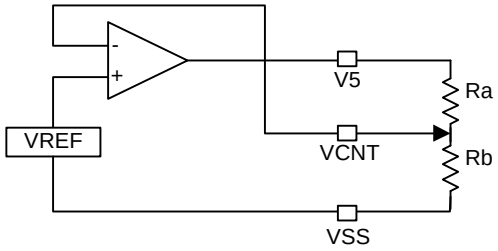
18.2 LCD Voltage Adjustment

There are two methods of adjusting the LCD voltage as follows:

18.2.1 Voltage Regulator

Voltage regulator output V5 is adjusted by internal Ra/Rb resistors ratio or externally attached Ra and Rb.
VREF(V) = (1-α /162) x VREG

$$V5 = \frac{Ra + Rb}{Ra} \times VREF\ (V)$$



Temperature Coefficient	VREG	Ta = 25°C
0.05%/°C	2.1Voltage	
0.2%/°C	4.9 Voltage	
External VREG input	VRS	

V5 Voltage regulator Internal Resistor Ratio Register Value and (Ra+Rb)/Ra Ratio (for reference)

Internal Resistance Ratio Register			Internal (Ra+Rb)/Ra Ratio		
D2	D1	D0	0.05	0.2	VREG External Input
0	0	0	3.0	1.3	1.5
0	0	1	3.5	1.5	2.0
0	1	0	4.0	1.8	2.5
0	1	1	4.5	2.0	3.0
1	0	0	5.0	2.3	3.5
1	0	1	5.5	2.5	4.0
1	1	0	6.0	2.8	4.5
1	1	1	6.4	3.0	5.0

18.2.2 LCD Voltage Command Fine Adjustment control

Software control of 64 voltage levels (α) adjustment of V5 voltage by set 6 bits of the data bus. It can adjust the LCD contrast.
LCD voltage command is a two-byte command used as a pair with the LCD voltage command and LCD voltage command fine adjustment control, and both command must be issued on after the other.

18.3 Static Icon Display

This controls the static drive system display. This is used when one of the static indicator LCD electrodes is connected to the FR terminal, and the other is connected to the FRS terminal.
The Static Icon Display command set ON is a two-byte command used as a pair with the Static Icon Display command set and Static Icon Display register set.
The Static Icon Display command set OFF is a single byte command.

18.4 LCD Bias voltage

When use built-in LCD bias resistor, Software can control the 1/9, 1/7 bias ratio to match the characteristic of LCD panel.

18.5 Voltage Follower

The voltage follower buffers the LCD bias voltage created by the built-in bias resistor, and supplies it to the LCD drive circuit.

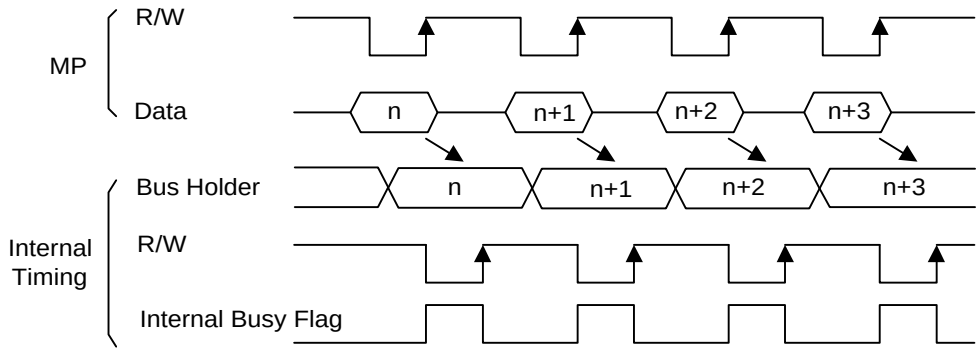
18.6 High power mode

When the LCD with large loads, the high power mode power supply (set $\overline{HPM}$ = Low) can improve the quality of the LCD display.

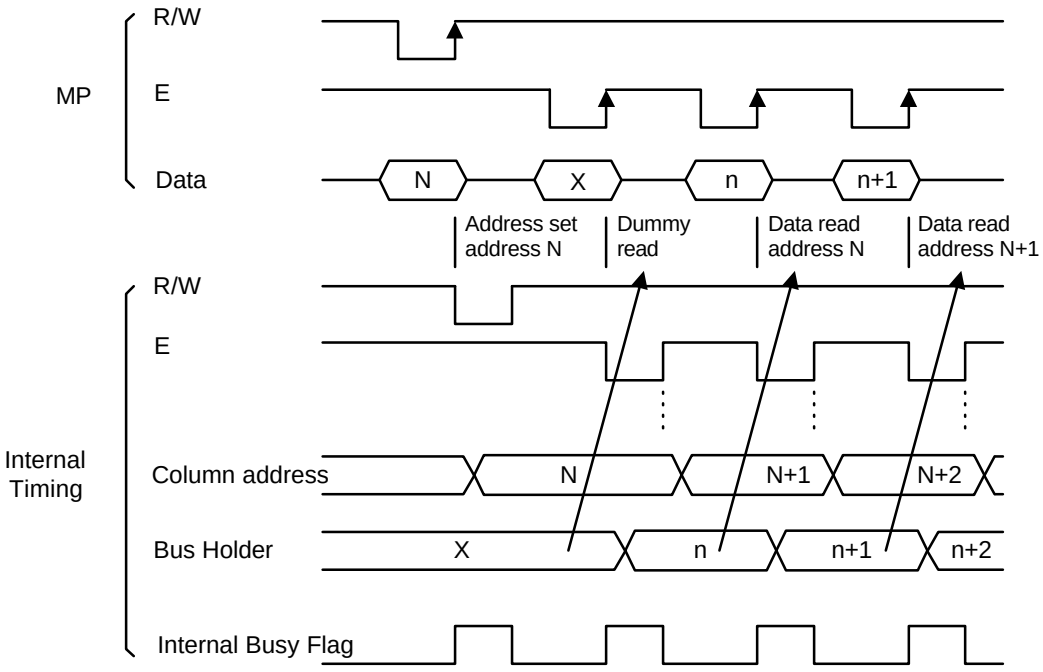
Interface

1. Parallel Interface

1.1 Display Data Write (the 80-Series interface)

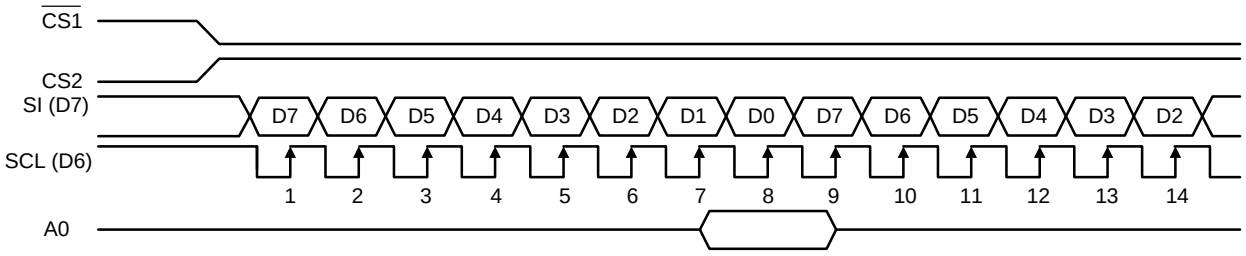


1.2 Display Data Read (the 80-Series interface)



2 Serial Interface

Serial Interface Display Data Write Timing



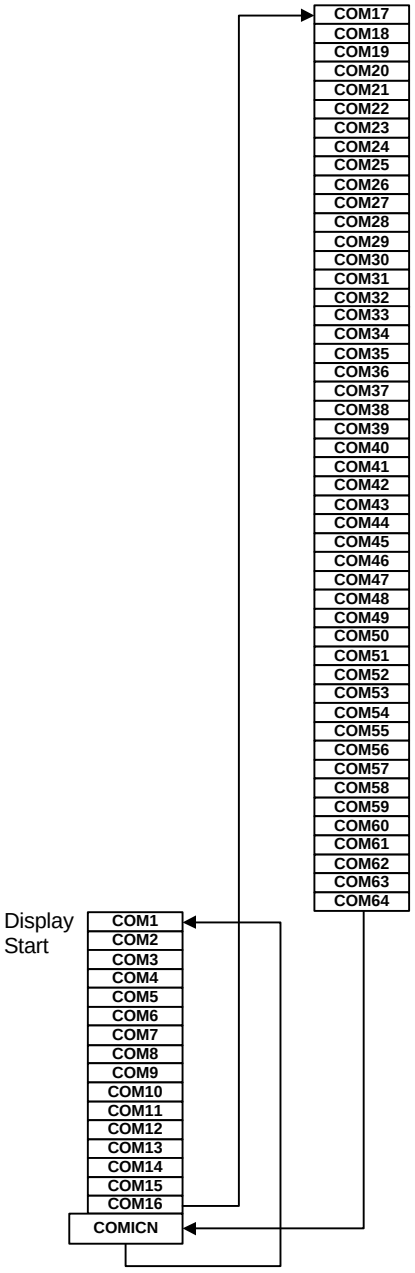
Notes:

1. The user can not reading from A31W65132 when in serial interface mode.
2. A0=High, the data is display data, A0=Low, the data is command data.
   The A0 signal is sampled every 8th rising edge of SCL clock, when the chip becomes active in serial interface mode.
3. The counter and the shift register are reset to the default value when the chip is not active.

Display Data RAM vs Address

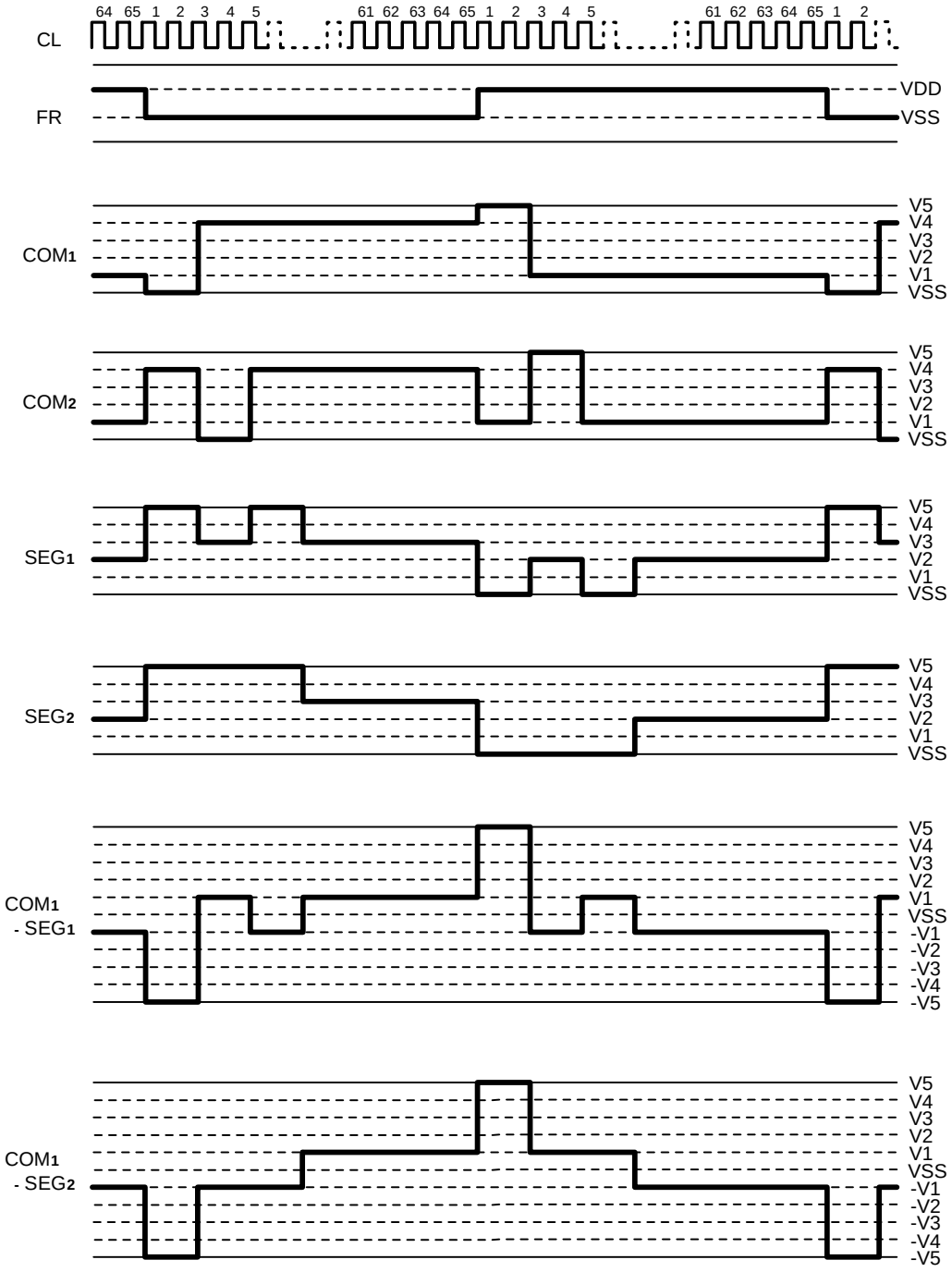
Page Address			Line Address
0, 0, 0, 0	D0 D1 D2 D3 D4 D5 D6 D7	**Page0**	00H 01H 02H 03H 04H 05H 06H 07H
0, 0, 0, 1	D0 D1 D2 D3 D4 D5 D6 D7	**Page1**	08H 09H 0AH 0BH 0CH 0DH 0EH 0FH
0, 0, 1, 0	D0 D1 D2 D3 D4 D5 D6 D7	**Page2**	10H 11H 12H 13H 14H 15H 16H 17H
0, 0, 1, 1	D0 D1 D2 D3 D4 D5 D6 D7	**Page3**	18H 19H 1AH 1BH 1CH 1DH 1EH 1FH
0, 1, 0, 0	D0 D1 D2 D3 D4 D5 D6 D7	**Page4**	20H 21H 22H 23H 24H 25H 26H 27H
0, 1, 0, 1	D0 D1 D2 D3 D4 D5 D6 D7	**Page5**	28H 29H 2AH 2BH 2CH 2DH 2EH 2FH
0, 1, 1, 0	D0 D1 D2 D3 D4 D5 D6 D7	**Page6**	30H 31H 32H 33H 34H 35H 36H 37H
0, 1, 1, 1	D0 D1 D2 D3 D4 D5 D6 D7	**Page7**	38H 39H 3AH 3BH 3CH 3DH 3EH 3FH
1, 0, 0, 0	D0	**Page8**	40H
Column Address	00 01 02 03 04 05 06 07 ..... 3F 40 ..... 82 83		ADC D0= "0"
	83 82 81 80 7F 7E 7D 7C 01 00		ADC D0= "1"
SEG Pin	1 2 3 4 5 6 7 8 .... 131 132		

An example of common output executing display start from the line address 30H.



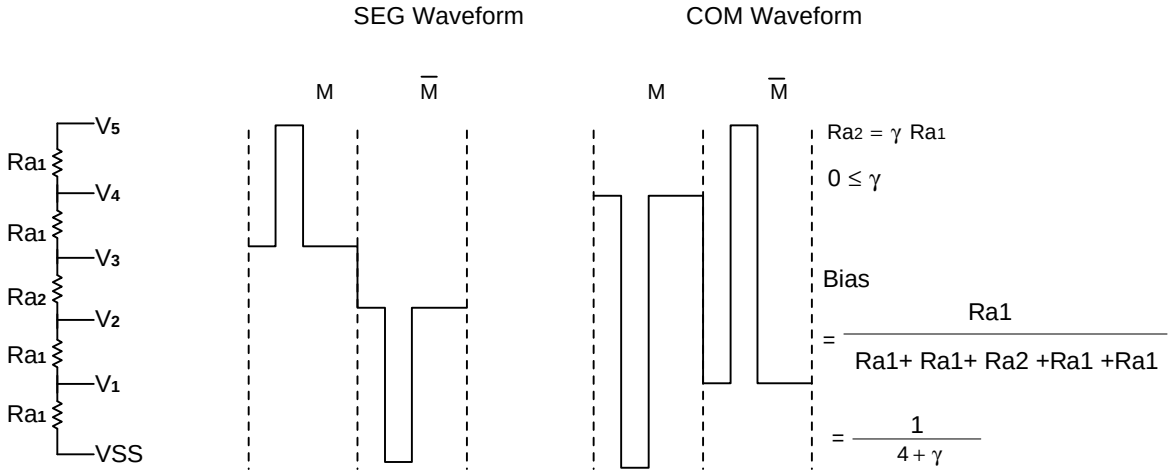
LCD Drive Output Waveform (Waveform B)

The following is an example of how the common and segment drivers may be connected to a LCD panel.



Examples of External Bias Resistor Connection vs LCD Drive Waveform

1/7 or 1/9 Bias



Absolute Maximum Ratings

VSS = 0.0V

Parameter		Symbol	Ratings	Unit
Supply voltage		VDD	-0.4 to +7.0	V
LCD drive voltage 1		V5, VOUT	-0.4 to +18	V
LCD drive voltage 2		V1, V2, V3, V4	-0.4 to V5	V
Input voltage		VIN	-0.4 to VDD+0.4	V
Output voltage		VOUT	-0.4 to VDD+0.4	V
Operating temperature range		Topr	-40 to +85	°C
Storage temperature range	Chip	Tstg	-55 to +125	°C
	TAB		-55 to +100	

Note 1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Note 2 Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 3 When connecting a bias resistor externally, set the LCD power supply voltage so that the state is changed to V5 ≥VDD.

DC Characteristics

Unless otherwise specified, VSS = 0 V, VDD = 3.0 V ± 10%, Ta = -40 to 85°C

Item		Symbol	Condition		Rating Min.	Rating Typ.	Rating Max.	Units	Applicable Pin
Operating Voltage (1)	Recommended Voltage	VDD			2.4	-	5.5	V	VDD*[1]
	Possible Operating Voltage				-	-	-	V	VDD*[1]
Operating Voltage (2)	Possible Operating Voltage	V5	(Relative to VSS)		4.5	-	16	V	V5
	Possible Operating Voltage	V1, V2	(Relative to VSS)		0	-	0.4 × V5	V	V1, V2
	Possible Operating Voltage	V3, V4	(Relative to VSS)		0.6 × V5	-	V5	V	V3, V4
High-level Input Voltage		V_{IHC}			0.8 × VDD	-	VDD	V	*3
Low-level Input Voltage		V_{ILC}			VSS	-	0.2 × VDD	V	*3
High-level Output Voltage		V_{OHC}	I_{OH} = -0.5 mA		0.8 × VDD	-	VDD	V	*4
Low-level Output Voltage		V_{OLC}	I_{OL} = 0.5 mA		VSS	-	0.2 × VDD	V	*4
Input leakage Current		I_{LI}	V_{IN} = VDD or VSS		-1.0	-	1.0	µA	*5
Output leakage Current		I_{LO}			-3.0	-	3.0	µA	*5
Liquid Crystal Driver ON Resistance		R_{ON}	Ta = 25°C (Relative To VSS)	V5 = 14.0 V V5 = 8.0 V	- -	2.0 3.2	3.5 5.4	KΩ KΩ	SEGn COMn*7
Static Consumption Current		I_{SSQ}	V5 = 18.0 V		-	0.01	5	µA	VSS
Output Leakage Current		I_{5Q}	(Relative To VSS)		-	0.01	15	µA	V5
Input Terminal Capacitance		C_{IN}	Ta = 25°C f = 1 MHz		-	5.0	8.0	pF	
Oscillator Frequency	Internal Oscillator	fosc	Ta = 25°C		18	22	26	KHz	*8
	External Input	f_{CL}			18	22	26	KHz	CL
Internal Power	Supply Step-up Output Voltage Circuit	V_{OUT}	(Absolute value referenced to VSS)		-	-	16.5	V	V_{OUT}
	Voltage Regulator Circuit Operating Voltage	V_{OUT}	(Absolute value referenced to VSS)		6	-	16.5	V	V_{OUT}
	Voltage Follower Circuit Operating Voltage	V5	(Absolute value referenced to VSS)		4.5	-	16	V	V5*9
	Base Voltage	V_{REG0} V_{REG1}	Ta = 25°C (Relative to VSS)	0.05%/°C 0.2%/°C	2.04 4.65	2.10 4.9	2.16 5.15	V V	*10 *10

DC Characteristics (continued)

. Dynamic Consumption Current (1), During Display, with the Internal Power Supply OFF
  Current consumed by the total ICs when an external power supply is used
. Dynamic Consumption Current (2), During Display, with the Internal Power Supply ON

Ta = 25°C

Item	Symbol	Condition		Rating			Units	Notes
				Min.	Typ.	Max.		
A31W65132	I_{DD} (1)	VDD=5.0 V, V5=11.0 V		-	18	30	µA	*11
		VDD=3.0 V, V5=11.0 V		-	16	27		
		VDD=5.0 V, V5=11.0 V		-	23	38		
		VDD=3.0 V, V5=11.0 V		-	21	35		
	I_{DD} (2)	VDD=5.0V, Triple step-up voltage. V5 =11.0 V	Normal Mode	-	67	112	µA	*12
			High-Power Mode	-	114	190		
		VDD=3.0V, Quad step-up voltage. V5 =11.0 V	Normal Mode	-	81	135		
			High-Power Mode	-	138	230		
		VDD=5.0V, Triple step-up voltage. V5 =11.0 V	Normal Mode	-	81	135	µA	*12
			High-Power Mode	-	127	212		
		VDD=3.0V, Quad step-up voltage. V5 =11.0 V	Normal Mode	-	96	160		
			High-Power Mode	-	153	255		
Sleep mode	I_{DDS1}	-		-	0.01	5	µA	*13
Standby mode	I_{DDS2}	-		-	4	8		

(Consumption Current at Time of Power Saver Mode, VSS=0V, VDD=3.0V±10%)

. The Relationship between Oscillator Frequency f_{OSC}, Display Clock Frequency f_{CL} and the Liquid Crystal Frame Rate Frequency f_{FR}

Item		f_{CL}	f_{FR}
A31W65132	When the internal oscillator circuit is used	$\frac{f_{OSC}}{4}$	$\frac{f_{OSC}}{4 \times 65}$
	When the internal oscillator circuit is not used	External input	

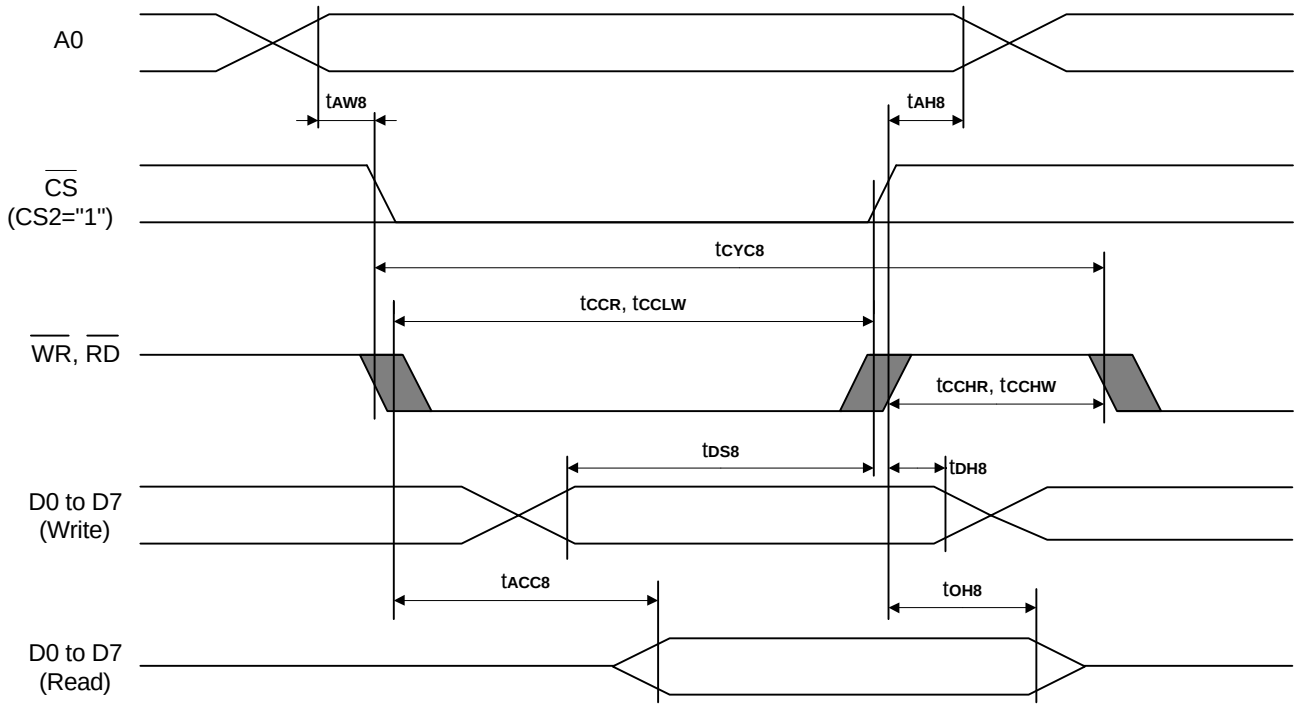
(f_{FR} is the liquid crystal alternating current period, and not the FR signal period.)

Notes:

1. While a broad range of operating voltages is guaranteed, performance cannot be guaranteed if there are sudden fluctuations to the voltage while the MPU is being accessed.
2. This applies when the external power supply is being used.
3. The A0, D0 to D5, D6 (SCL), D7 (SI), $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$), $\overline{CS1}$, CS2, CLS, CL, FR, M/S, C68/80, P/S, $\overline{DOF}$, $\overline{RES}$, IRS, and $\overline{HPM}$ terminals.
4. The D0 to D7, FR, FRS, $\overline{DOF}$, and CL terminals.
5. The A0, $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$), $\overline{CS1}$, CS2, CLS, M/S, C68/80, P/S, $\overline{RES}$, IRS, and $\overline{HPM}$ terminals.
6. Applies when the D0 to D5, D6 (SCL), D7 (SI), CL, FR, and $\overline{DOF}$ terminals are in a high impedance state.
7. These are the resistance values for when a 0.1 V voltage is applied between the output terminal SEGn or COMn and the various power supply terminals (V1, V2, V3, and V4). These are specified for the operating voltage (3) range.
   R_{ON} = 0.1 V/D I (Where D I is the current that flows when 0.1 V is applied while the power supply is ON.)
8. See the relationship between the oscillator frequency and the frame rate frequency.
9. The V5 voltage regulator circuit regulates within the operating voltage range of the voltage follower.
10. This is the internal voltage reference supply for the V5 voltage regulator circuit. In the A31W65132, the temperature range can come in three types as VREG options: (1) approximately 0.05%/°C
    (2) 0.2%/°C
    (3) external input.
11., 12. It indicates the current consumed on ICs alone when the internal oscillator circuit and display are turned on.
    The A31W65132 is 1/9 biased.
    Does not include the current due to the LCD panel capacity and wiring capacity.
    Applicable only when there is no access from the MPU.
12. It is the value on a model having the VREG option temperature gradient is 0.05%/°C when the V5 voltage regulator internal resistor is used.
13. When consumption current in Power Saver Mode is measured, the A0, $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$), D0~D7 terminals must be fixed in H or L.

Timing Characteristics

System Bus Read/Write Characteristics 1 (for the 8080 Series MPU)



(VDD = 4.5V to 5.5V Ta=-40 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	t_{AH8}		0	-	ns
Address setup time		t_{AW8}		0	-	ns
System cycle time	A0	t_{CYC8}		166	-	ns
Control L pulse width ($\overline{WR}$)	$\overline{WR}$	t_{cclw}		30	-	ns
Control L pulse width ($\overline{RD}$)	$\overline{RD}$	t_{CCLR}		70	-	ns
Control H pulse width ($\overline{WR}$)	$\overline{WR}$	t_{CCHW}		30	-	ns
Control H pulse width ($\overline{RD}$)	$\overline{RD}$	t_{CCHR}		30	-	ns
Data setup time	D0 to D7	t_{DS8}		30	-	ns
Address hold time		t_{DH8}		10	-	ns
$\overline{RD}$ access time		t_{ACC8}	CL = 100pF	-	70	ns
Output disable time		t_{OH8}		5	50	ns

(VDD = 2.7V to 4.5V Ta=-40 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	t_{AH8}		0	-	ns
Address setup time		t_{AW8}		0	-	ns
System cycle time	A0	t_{CYC8}		300	-	ns
Control L pulse width ($\overline{WR}$)	$\overline{WR}$	t_{CCLW}		60	-	ns
Control L pulse width ($\overline{RD}$)	$\overline{RD}$	t_{CCLR}		120	-	ns
Control H pulse width ($\overline{WR}$)	$\overline{WR}$	t_{CCHW}		60	-	ns
Control H pulse width ($\overline{RD}$)	$\overline{RD}$	t_{CCHR}		60	-	ns
Data setup time	D0 to D7	t_{DS8}		40	-	ns
Address hold time		t_{DH8}		15	-	ns
$\overline{RD}$ access time		t_{ACC8}	CL = 100pF	-	140	ns
Output disable time		t_{OH8}		10	100	ns

(VDD = 2.4V to 2.7V Ta=-40 to 85°C)

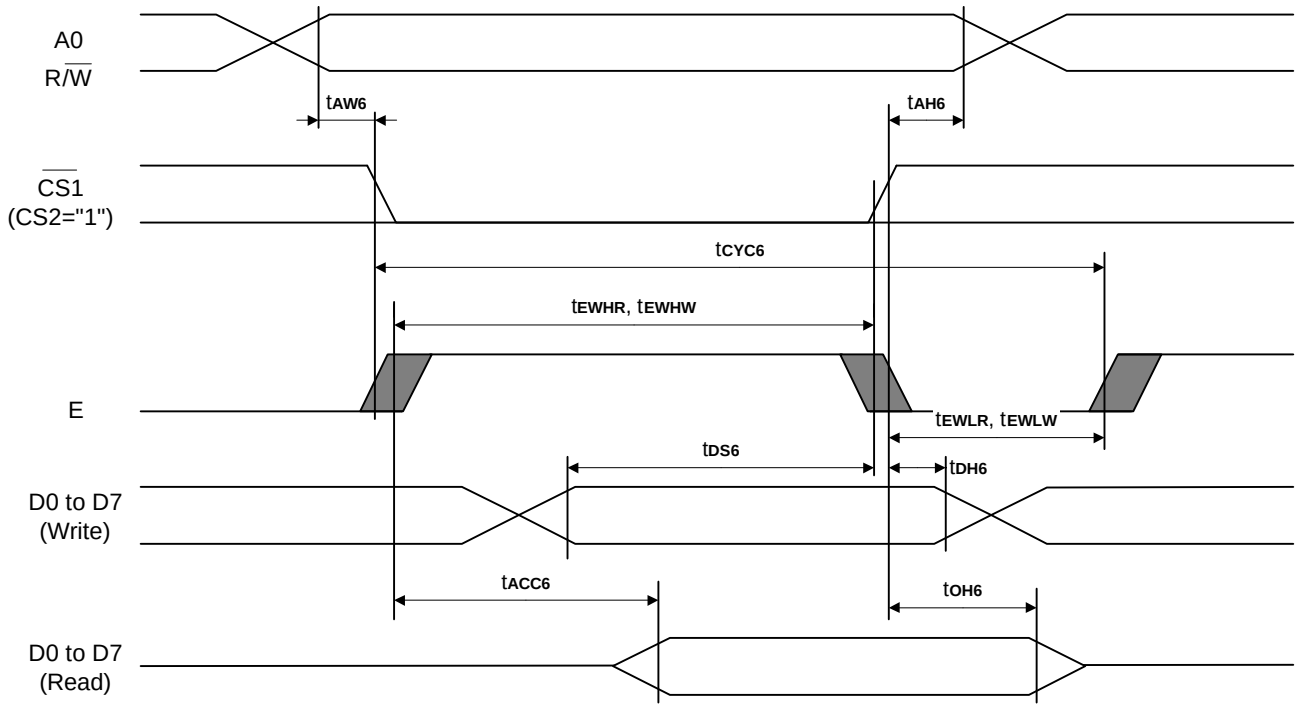
Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	t_{AH8}		0	-	ns
Address setup time		t_{AW8}		0	-	ns
System cycle time	A0	t_{CYC8}		1000	-	ns
Control L pulse width ($\overline{WR}$)	$\overline{WR}$	t_{CCLW}		120	-	ns
Control L pulse width ($\overline{RD}$)	$\overline{RD}$	t_{CCLR}		240	-	ns
Control H pulse width ($\overline{WR}$)	$\overline{WR}$	t_{CCHW}		120	-	ns
Control H pulse width ($\overline{RD}$)	$\overline{RD}$	t_{CCHR}		120	-	ns
Data setup time	D0 to D7	t_{DS8}		80	-	ns
Address hold time		t_{DH8}		30	-	ns
$\overline{RD}$ access time		t_{ACC8}	CL = 100pF	-	280	ns
Output disable time		t_{OH8}		10	200	ns

Notes:

1. The input signal rise time and fall time (t_r, t_f) is specified at 15 ns or less. When the system cycle time is extremely fast, ($t_r + t_f$) ≤ ($t_{CYC8} - t_{CCLW} - t_{CCHW}$) for ($t_r + t_f$) ≤ ($t_{CYC8} - t_{CCLR} - t_{CCHR}$) are specified.
2. All timing is specified using 20% and 80% of VDD as the reference.
3. t_{CCLW} and t_{CCLR} are specified as the overlap between $\overline{CS1}$ being "L" (CS2 = "H") and $\overline{WR}$ and $\overline{RD}$ being at the "L" level.

Timing Characteristics (continued)

System Bus Read/Write Characteristics 2 (for the 6800 Series MPU)



(VDD = 4.5V to 5.5V Ta=-40 to 85°C)

Item		Signal	Symbol	Condition	Rating		Units
					Min.	Max.	
Address hold time		A0	t_{AH6}		0	-	ns
Address setup time			t_{AW6}		0	-	ns
System cycle time		A0	t_{CYC6}		166	-	ns
Data setup time		D0 to D7	t_{DS6}		30	-	ns
Data hold time			t_{DH6}		10	-	ns
Access time			t_{ACC6}	CL = 100pF	-	70	ns
Output disable time			t_{OH6}		10	50	ns
Enable H pulse time	Read	E	t_{EWHR}		70	-	ns
	Write		t_{EWHW}		30	-	ns
Enable L pulse time	Read	E	t_{EWLR}		30	-	ns
	Write		t_{EWLW}		30	-	ns

(VDD = 2.7V to 4.5V Ta=-40 to 85°C)

Item		Signal	Symbol	Condition	Rating		Units
					Min.	Max.	
Address hold time		A0	t_{AH6}		0	-	ns
Address setup time			t_{AW6}		0	-	ns
System cycle time		A0	t_{CYC6}		300	-	ns
Data setup time		D0 to D7	t_{DS6}		40	-	ns
Data hold time			t_{DH6}		15	-	ns
Access time			t_{ACC6}	CL = 100pF	-	140	ns
Output disable time			t_{OH6}		10	100	ns
Enable H pulse time	Read	E	t_{EWHR}		120	-	ns
	Write		t_{EWHW}		60	-	ns
Enable L pulse time	Read	E	t_{EWLR}		60	-	ns
	Write		t_{EWLW}		60	-	ns

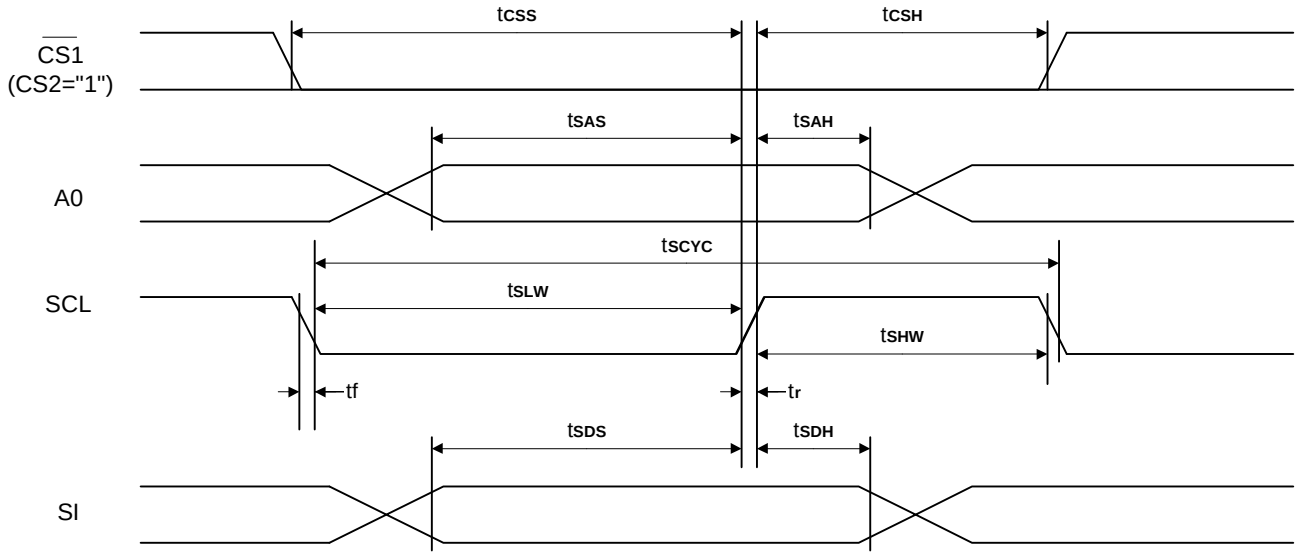
(VDD = 2.4V to 2.7V Ta=-40 to 85°C)

Item		Signal	Symbol	Condition	Rating		Units
					Min.	Max.	
Address hold time		A0	t_{AH6}		0	-	ns
Address setup time			t_{AW6}		0	-	ns
System cycle time		A0	t_{CYC6}		1000	-	ns
Data setup time		D0 to D7	t_{DS6}		80	-	ns
Data hold time			t_{DH6}		30	-	ns
Access time			t_{ACC6}	CL = 100pF	-	280	ns
Output disable time			t_{OH6}		10	280	ns
Enable H pulse time	Read	E	t_{EWHR}		240	-	ns
	Write		t_{EWHW}		120	-	ns
Enable L pulse time	Read	E	t_{EWLR}		120	-	ns
	Write		t_{EWLW}		120	-	ns

Notes:

1. The input signal rise time and fall time (t_r, t_f) is specified at 15 ns or less. When the system cycle time is extremely fast, ($t_r + t_f$) ≤ ($t_{CYC6} - t_{EWLW} - t_{EWHW}$) for ($t_r + t_f$) ≤ ($t_{CYC6} - t_{EWLR} - t_{EWHR}$) are specified.
2. All timing is specified using 20% and 80% of VDD as the reference.
3. t_{EWLW} and t_{EWLR} are specified as the overlap between $\overline{CS1}$ being "L" (CS2 = "H") and E.

The Serial Interface



(VDD = 4.5V to 5.5V Ta=-40 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	t_{SCYC}		200	-	ns
SCL "H" pulse width		t_{SHW}		75	-	ns
SCL "L" pulse width		t_{SLW}		75	-	ns
Access setup time	A0	t_{SAS}		50	-	ns
Address hold time		t_{SAH}		100	-	ns
Data setup time	SI	t_{SDS}		50	-	ns
Data hold time		t_{SDH}		50	-	ns
CS-SCL time	CS	t_{CSS}		100	-	ns
		t_{CSH}		100	-	ns

(VDD = 2.7V to 4.5V Ta=-40 to 85°C)

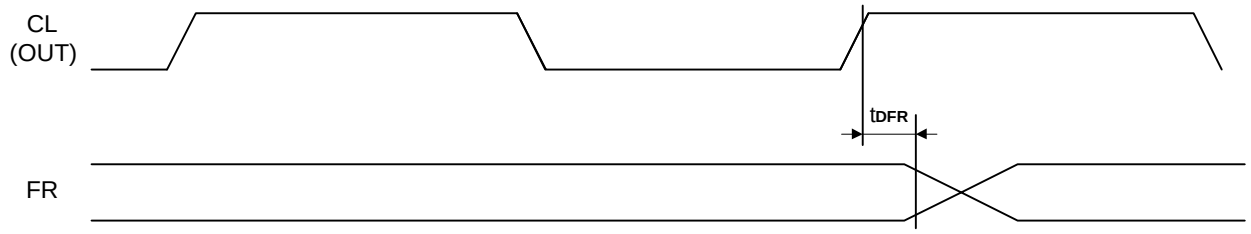
Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	t_{SCYC}		250	-	ns
SCL "H" pulse width		t_{SHW}		100	-	ns
SCL "L" pulse width		t_{SLW}		100	-	ns
Access setup time	A0	t_{SAS}		150	-	ns
Address hold time		t_{SAH}		150	-	ns
Data setup time	SI	t_{SDS}		100	-	ns
Data hold time		t_{SDH}		100	-	ns
CS-SCL time	CS	t_{CSS}		150	-	ns
		t_{CSH}		150	-	ns

(VDD = 2.4V to 2.7V Ta=-40 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	t_{SCYC}		400	-	ns
SCL "H" pulse width		t_{SHW}		150	-	ns
SCL "L" pulse width		t_{SLW}		150	-	ns
Access setup time	A0	t_{SAS}		250	-	ns
Address hold time		t_{SAH}		250	-	ns
Data setup time	SI	t_{SDS}		150	-	ns
Data hold time		t_{SDH}		150	-	ns
CS-SCL time	CS	t_{CSS}		250	-	ns
		t_{CSH}		250	-	ns

Notes:
1. The input signal rise and fall time (t_r, t_f) are specified at 15ns or less.
2. All timing is specified using 20% and 80% of VDD as the standard.

Display Control Output Timing



(VDD = 4.5V to 5.5V Ta=-40 to 85°C)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
FR delay time	FR	t_{DFR}	C_L = 50 pF	-	10	40	ns

(VDD = 2.7V to 4.5V Ta=-40 to 85°C)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
FR delay time	FR	t_{DFR}	C_L = 50 pF	-	20	80	ns

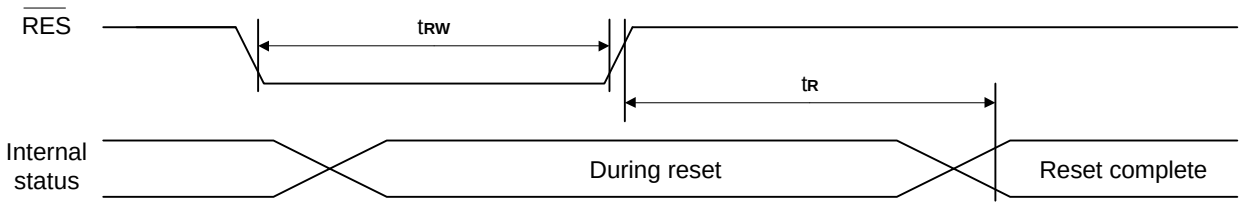
(VDD = 2.4V to 2.7V Ta=-40 to 85°C)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
FR delay time	FR	t_{DFR}	C_L = 50 pF	-	50	200	ns

Notes:

1. Valid only when the master mode is selected.
2. All timing is based on 20% and 80% of VDD.

Reset Timing



(VDD = 4.5V to 5.5V Ta=-40 to 85°C)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		t_R		-	-	0.5	µs
Reset "L" pulse width	$\overline{RES}$	t_{RW}		0.5	-	-	µs

(VDD = 2.7V to 4.5V Ta=-40 to 85°C)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		t_R		-	-	1	µs
Reset "L" pulse width	$\overline{RES}$	t_{RW}		1	-	-	µs

(VDD = 2.4V to 4.5V Ta=-40 to 85°C)

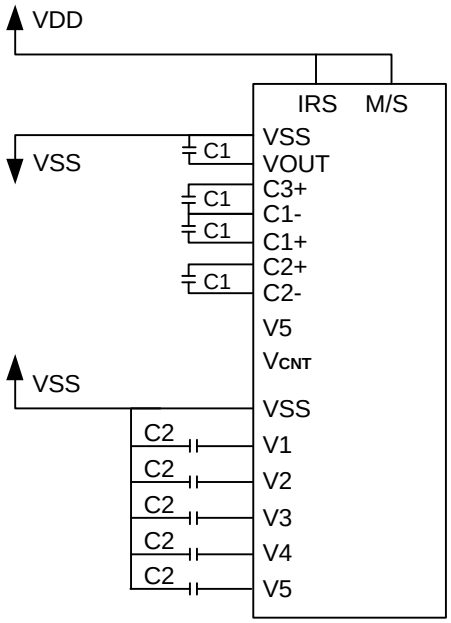
Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		t_R		-	-	1.5	µs
Reset "L" pulse width	$\overline{RES}$	t_{RW}		1.5	-	-	µs

Note: All timing is specified with 20% and 80% of VDD as the standard.

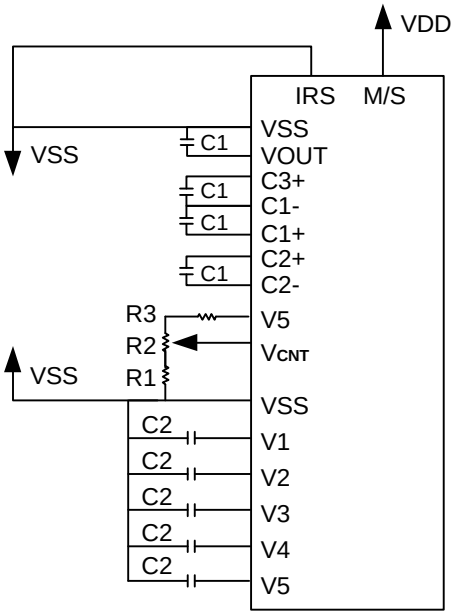
Examples of Applications of LCD Power Supply

1. When used all of the step-up circuit, voltage regulating circuit and V/F circuit

. When the voltage regulator internal resistor is used.
(Example 4x step-up)

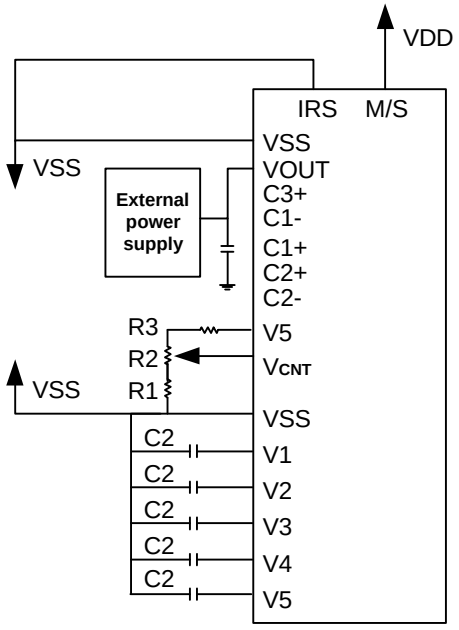


. When the voltage regulator internal resistor is not used.
(Example 4x step-up)

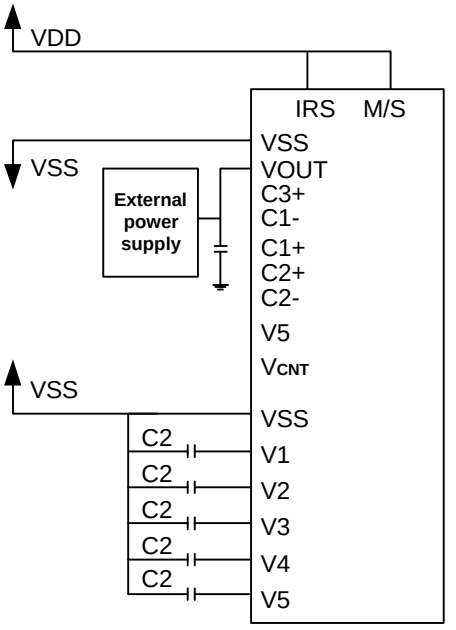


2. When the voltage regulator circuit and V/F circuit alone used

. When the V5 voltage regulator internal resistor is not used.

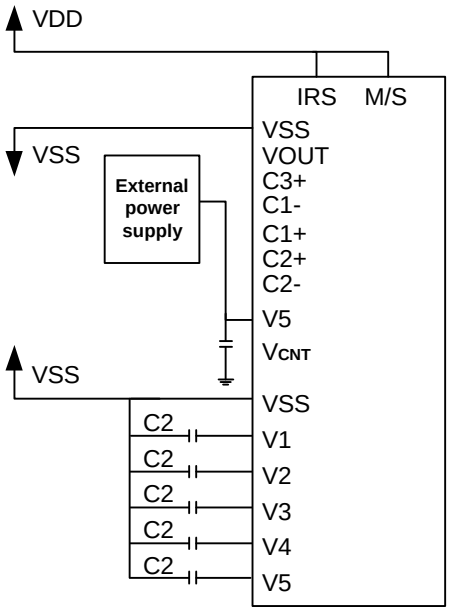


. When the V5 voltage regulator internal resistor is used.

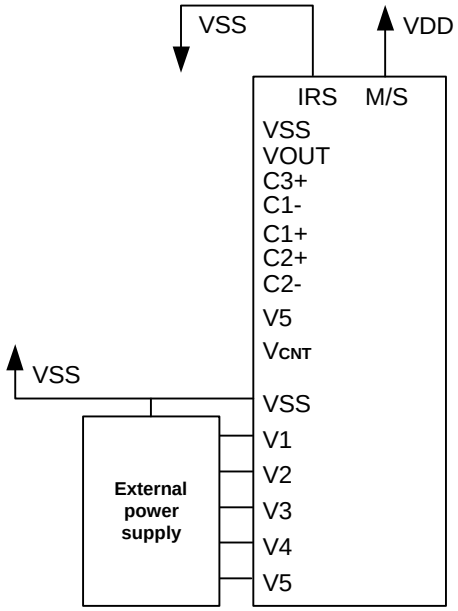


Examples of Applications of LCD Power Supply (continued)

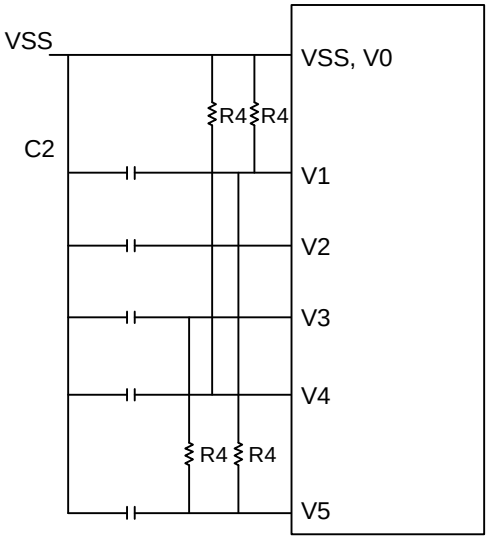
3. When the V/F circuit alone is used



4. When the built-in power is not used



5. When the built-in power circuit is used to drive a liquid crystal panel heavily loaded with AC or DC, it is recommended to connect an external resistor to stabilize potentials of V1, V2, V3 and V4 which are output from the built-in voltage follower.



Reference set value R4: 100KΩ ~ 1MΩ
It is recommended to set an optimum resistance value R4 taking the liquid crystal display and the drive waveform.

Example of shared reference settings When V5 can vary between 8 and 12V

Item	Set value	Units
C1	1.0 to 4.7	uF
C2	0.01 to 1.0	uF

Notes:

1. Because the V_R terminal input impedance is high, use short leads and shielded lines.
2. C1 and C2 are determined by the size of the LCD being driven. Select a value that will stabilize the liquid crystal drive voltage.

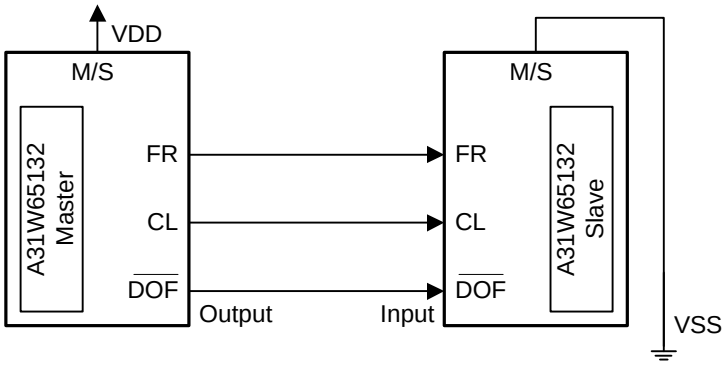
Example of the Process by which to Determine the Settings:

- Turn the voltage regulator circuit and voltage follower circuit ON and supply a voltage to V_{OUT} from the outside.
- Determine C2 by displaying a LCD pattern with a heavy load (such as horizontal stripes) and selecting a C2 that stabilizes the liquid crystal drive voltages (V1 to V5). Note that all C2 capacitors must have the same capacitance value.
- Next turn all the power supplies ON and determine C1.

Connections Between LCD Drivers (reference examples)

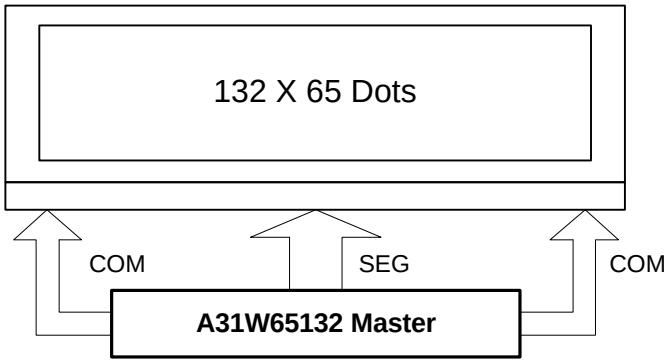
The liquid crystal display area can be enlarged with ease through the use of multiple A31W65132 series chips. Use a same equipment type.

1. A31W65132 (master) ↔ A31W65132 (slave)

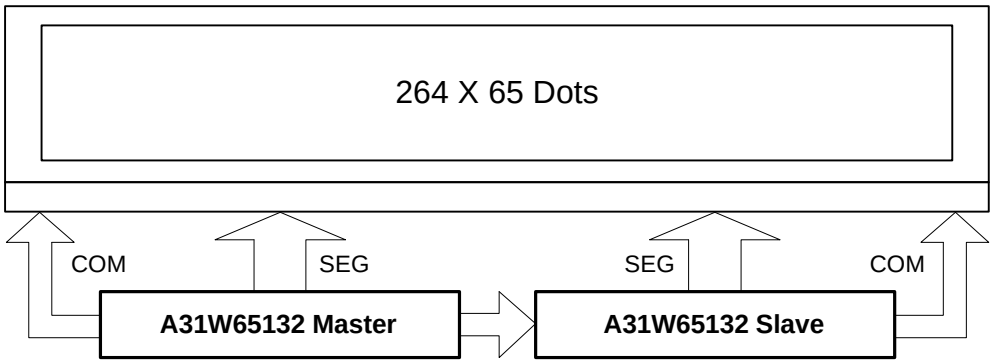


The liquid crystal display area can be enlarged with ease through the use of multiple A31W65132 series chips. Use a same equipment type, in the composition of these chips.

1. Single-chip Structure



2. Double-chip Structure, # 1



Ordering Information

Part No.	Package
A31W65132C	COG
A31W65132T	TCP