



# A6173081 Series

***Preliminary***

***128K X 8 BIT HIGH SPEED CMOS SRAM***

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**Document Title**

**128K X 8 BIT HIGH SPEED CMOS SRAM**

**Revision History**

| <b><u>Rev. No.</u></b> | <b><u>History</u></b> | <b><u>Issue Date</u></b> | <b><u>Remark</u></b> |
|------------------------|-----------------------|--------------------------|----------------------|
| 0.0                    | Initial issue         | July 14, 2000            | Preliminary          |



# A6173081 Series

**Preliminary**

## 128K X 8 BIT HIGH SPEED CMOS SRAM

### Features

- Center power pinout
- Supply voltage:  $5V \pm 10\%$
- Access times: 12/15 ns (max.)
- Current: Operating: -12: 170mA (max.)  
                  -15: 165mA (max.)  
                  Standby: TTL: 25mA (max.)  
                              CMOS: 8mA (max.)
- Full static operation, no clock or refreshing required
- All inputs and outputs are directly TTL compatible
- Common I/O using three-state output
- Data retention voltage: 3V (min.)
- Available in 32-pin 300mil / 400mil SOJ packages

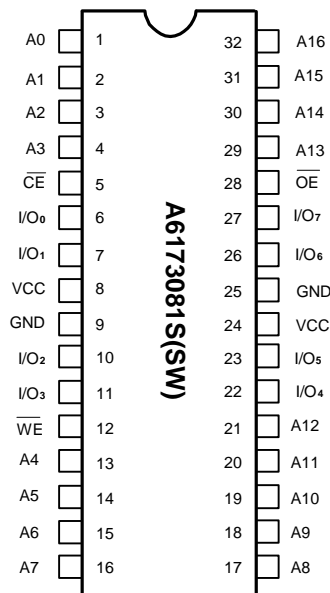
### General Description

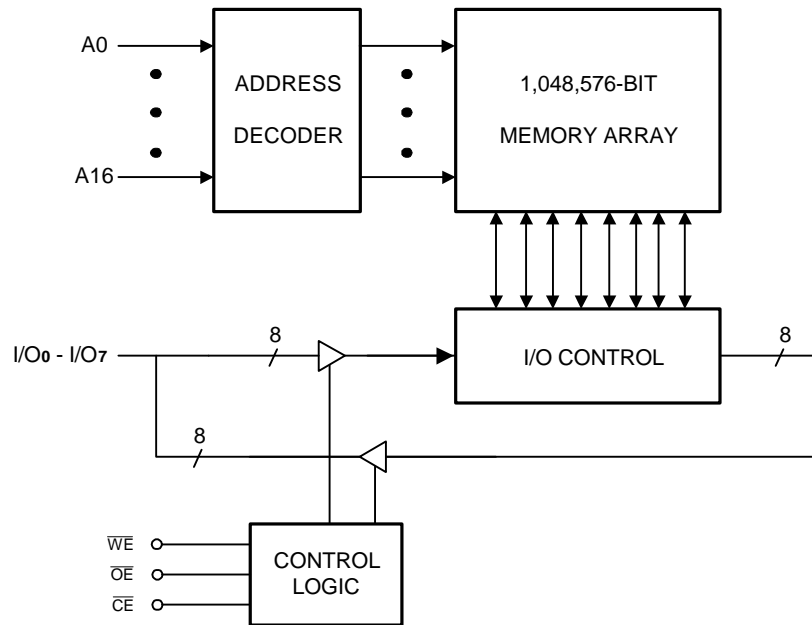
The A6173081 is a high-speed 1,048,576-bit static random access memory organized as 131,072 words by 8 bits and operates on a 5V power supply. It is built using high performance CMOS process. Inputs and three-state outputs are TTL compatible and allow for direct interfacing with common system bus structures.

Minimum standby power is drawn by this device when chip enable is disable, independent of the other input levels. Data retention is guaranteed at a power supply voltage as low as 3V.

### Pin Configurations

#### ■ SOJ



**Block Diagram**

**Pin Descriptions – SOJ**

| Pin No.                  | Symbol                              | Description         |
|--------------------------|-------------------------------------|---------------------|
| 1-4, 13-21, 29-32        | A0 - A16                            | Address Inputs      |
| 6-7, 10-11, 22-23, 26-27 | I/O <sub>0</sub> - I/O <sub>7</sub> | Data Inputs/Outputs |
| 5                        | $\overline{CE}$                     | Chip Enable         |
| 28                       | $\overline{OE}$                     | Output Enable       |
| 12                       | $\overline{WE}$                     | Write Enable        |
| 8, 24                    | VCC                                 | Power Supply        |
| 9, 25                    | GND                                 | Ground              |



**Recommended DC Operating Conditions**

(T<sub>A</sub> = 0°C to +70°C)

| Symbol          | Parameter             | Min. | Typ. | Max.      | Unit |
|-----------------|-----------------------|------|------|-----------|------|
| VCC             | Supply Voltage        | 4.5  | 5.0  | 5.5       | V    |
| GND             | Ground                | 0    | 0    | 0         | V    |
| V <sub>IH</sub> | Input High Voltage    | 2.2  | -    | VCC + 0.5 | V    |
| V <sub>IL</sub> | Input Low (1) Voltage | -0.5 | 0    | +0.8      | V    |
| C <sub>L</sub>  | Output Load           | -    | -    | 30        | pF   |

**Absolute Maximum Ratings\***

VCC to GND . . . . . -0.5V to +7V  
 IN, IN/OUT Volt to GND . . . . . -0.5V to VCC +0.5V  
 Operating Temperature, Topr . . . . . 0°C to +70°C  
 Storage Temperature, Tstg . . . . . -55°C to +125°C  
 Temperature Under Bias, Tbias . . . . . -10°C to +85°C  
 Power Dissipation, Pr . . . . . 1.0W

**\*Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

**DC Electrical Characteristics** (T<sub>A</sub> = 0°C to +70°C, VCC = 5V ± 10%, GND = 0V)

| Symbol               | Parameter                    | A6173081-12 |      | A6173081-15 |      | Unit | Conditions  |
|----------------------|------------------------------|-------------|------|-------------|------|------|---|
|                      |                              | Min.        | Max. | Min.        | Max. |      |   |
| I <sub>LI</sub>      | Input Leakage                | -           | 2    | -           | 2    | μA   | V <sub>IN</sub> = GND to VCC  |
| I <sub>LO</sub>      | Output Leakage               | -           | 2    | -           | 2    | μA   | $\overline{CE} = V_{IH}, \overline{OE} = V_{IH}$<br>V <sub>I/O</sub> = GND to VCC         |
| I <sub>CC1</sub> (2) | Dynamic Operating Current    | -           | 170  | -           | 165  | mA   | $\overline{CE} = V_{IL}, I_{I/O} = 0$ mA<br>Min. Cycle, Duty = 100%                       |
| I <sub>SB</sub>      | Standby Power Supply Current | -           | 25   | -           | 25   | mA   | $\overline{CE} = V_{IH}$  |
| I <sub>SB1</sub>     |                              | -           | 8    | -           | 8    | mA   | $\overline{CE} \geq VCC - 0.2V,$<br>V <sub>IN</sub> ≥ VCC -0.2V or V <sub>IN</sub> ≤ 0.2V |
| V <sub>OL</sub>      | Output Low Voltage           | -           | 0.4  | -           | 0.4  | V    | I <sub>OL</sub> = 8 mA  |
| V <sub>OH</sub>      | Output High Voltage          | 2.4         | -    | 2.4         | -    | V    | I <sub>OH</sub> = -4 mA   |

- Notes: 1. V<sub>IL</sub> = -3.0V for pulses less than 20 ns.  
 2. I<sub>CC1</sub> is dependent on output loading, cycle rates, and Read/Write patterns.



**Truth Table**

| Mode           | $\overline{CE}$ | $\overline{OE}$ | $\overline{WE}$ | I/O Operation | Supply Current    |
|----------------|-----------------|-----------------|-----------------|---------------|-------------------|
| Standby        | H               | X               | X               | High Z        | $I_{SB}, I_{SB1}$ |
| Output Disable | L               | H               | H               | High Z        | $I_{CC1}$         |
| Read           | L               | L               | H               | Dout          | $I_{CC1}$         |
| Write          | L               | X               | L               | Din           | $I_{CC1}$         |

Note: X = H or L

**Capacitance** ( $T_A = 25^\circ\text{C}$ ,  $f = 1.0\text{MHz}$ )

| Symbol     | Parameter                | Min. | Max. | Unit | Conditions    |
|------------|--------------------------|------|------|------|---------------|
| $C_{IN}^*$ | Input Capacitance        | -    | 8    | pF   | $V_{IN} = 0V$ |
| $C_{IO}^*$ | Input/Output Capacitance | -    | 8    | pF   | $V_{IO} = 0V$ |

\* These parameters are sampled and not 100% tested.

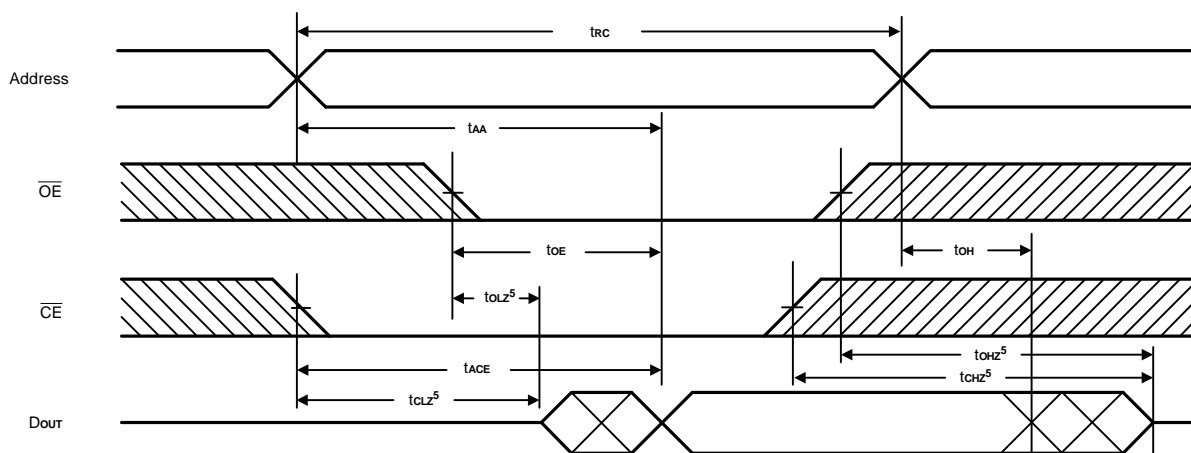
**AC Characteristics** ( $T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ ,  $V_{CC} = 5V \pm 10\%$ )

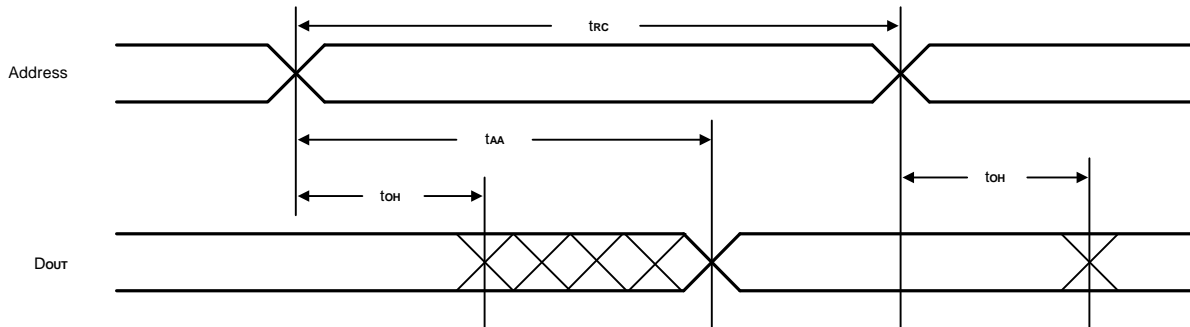
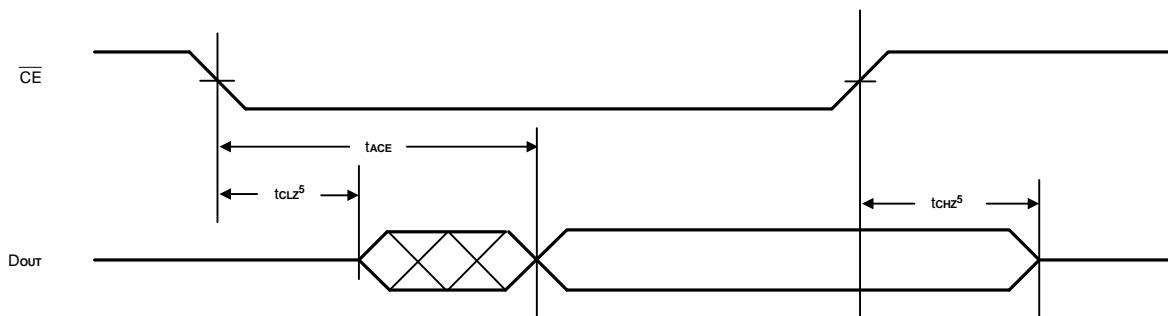
| Symbol     | Parameter                          | A6173081-12 |      | A6173081-15 |      | Unit |
|------------|------------------------------------|-------------|------|-------------|------|------|
|            |                                    | Min.        | Max. | Min.        | Max. |      |
| Read Cycle |                                    |             |      |             |      |      |
| $t_{RC}$   | Read Cycle Time                    | 12          | -    | 15          | -    | ns   |
| $t_{AA}$   | Address Access Time                | -           | 12   | -           | 15   | ns   |
| $t_{ACE}$  | Chip Enable Access Time            | -           | 12   | -           | 15   | ns   |
| $t_{OE}$   | Output Enable to Output Valid      | -           | 6    | -           | 8    | ns   |
| $t_{CLZ}$  | Chip Enable to Output in Low Z     | 3           | -    | 3           | -    | ns   |
| $t_{OLZ}$  | Output Enable to Output in Low Z   | 0           | -    | 0           | -    | ns   |
| $t_{CHZ}$  | Chip Disable Output in High Z      | 0           | 6    | -           | 8    | ns   |
| $t_{OHZ}$  | Output Disable to Output in High Z | 0           | 6    | 0           | 8    | ns   |
| $t_{OH}$   | Output Hold from Address Change    | 3           | -    | 3           | -    | ns   |

**AC Characteristics (continued)**

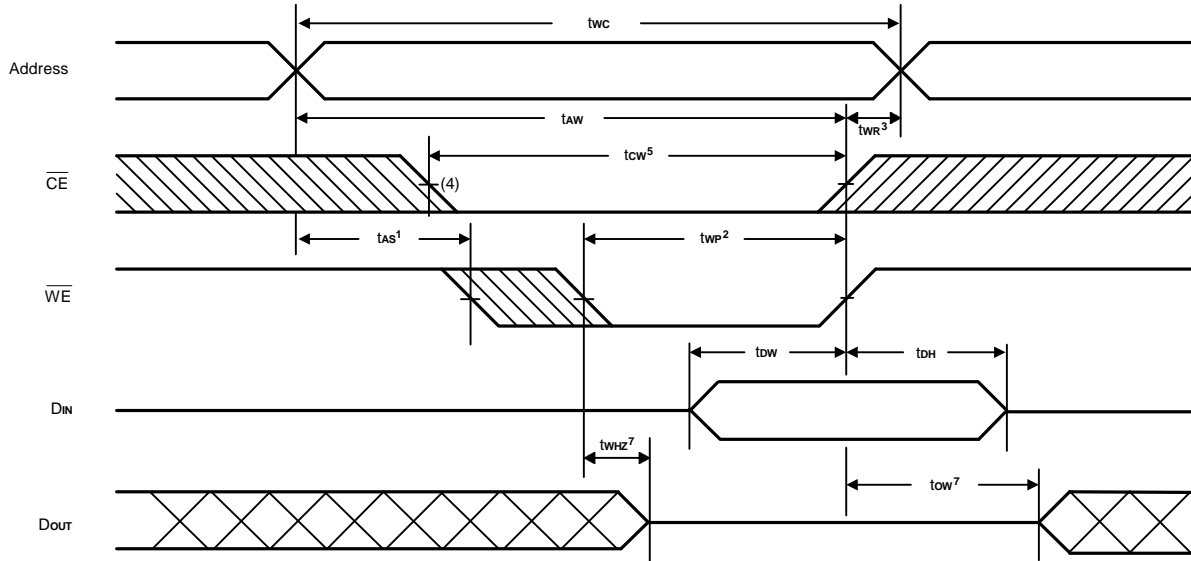
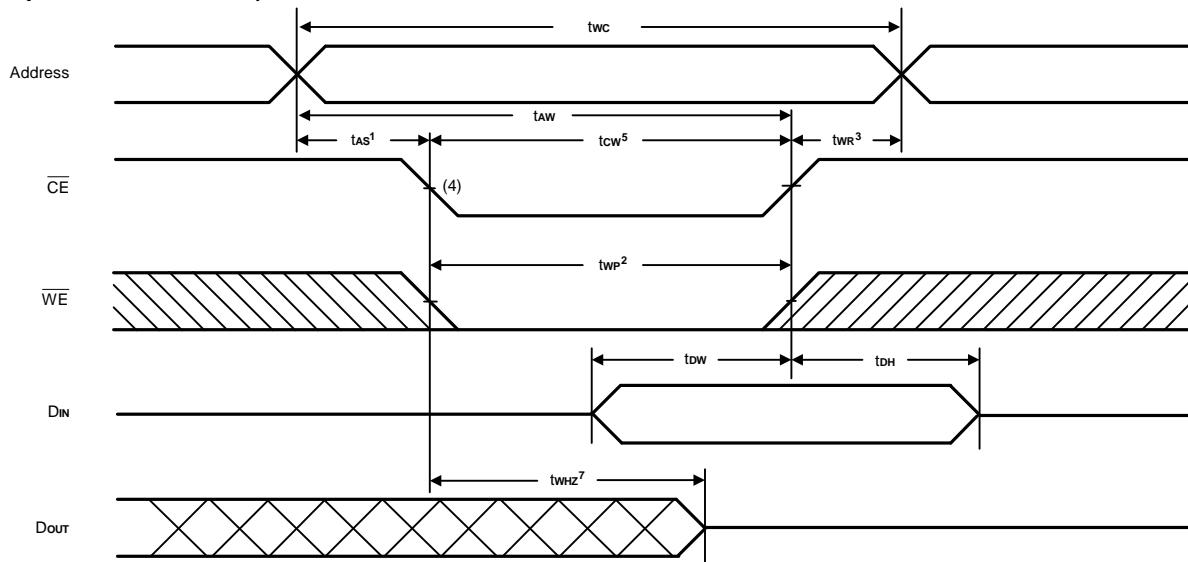
| Symbol           | Parameter                       | A6173081-12 |      | A6173081-15 |      | Unit |
|------------------|---------------------------------|-------------|------|-------------|------|------|
|                  |                                 | Min.        | Max. | Min.        | Max. |      |
| Write Cycle      |                                 |             |      |             |      |      |
| t <sub>wc</sub>  | Write Cycle Time                | 12          | -    | 15          | -    | ns   |
| t <sub>cw</sub>  | Chip Enable to End of Write     | 10          | -    | 12          | -    | ns   |
| t <sub>as</sub>  | Address Setup Time of Write     | 0           | -    | 0           | -    | ns   |
| t <sub>aw</sub>  | Address Valid to End of Write   | 10          | -    | 12          | -    | ns   |
| t <sub>wp</sub>  | Write Pulse Width               | 10          | -    | 12          | -    | ns   |
| t <sub>wr</sub>  | Write Recovery Time             | 0           | -    | 0           | -    | ns   |
| t <sub>whz</sub> | Write to Output in High Z       | 0           | 6    | 0           | 8    | ns   |
| t <sub>dw</sub>  | Data to Write Time Overlap      | 6           | -    | 7           | -    | ns   |
| t <sub>dh</sub>  | Data Hold from Write Time       | 0           | -    | 0           | -    | ns   |
| t <sub>ow</sub>  | Output Active from End of Write | 3           | -    | 3           | -    | ns   |

Notes: t<sub>chz</sub>, t<sub>ohz</sub> and t<sub>whz</sub> are defined as the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.

**Timing Waveforms**
**Read Cycle 1<sup>(1)</sup>**


**Timing Waveforms (continued)**
**Read Cycle 2<sup>(1, 2, 4)</sup>**

**Read Cycle 3<sup>(1, 3, 4)</sup>**


- Notes:
1.  $\overline{WE}$  is high for Read Cycle.
  2. Device is continuously enabled,  $\overline{CE} = V_{IL}$ .
  3. Address valid prior to or coincident with  $\overline{CE}$  transition low.
  4.  $\overline{OE} = V_{IL}$ .
  5. Transition is measured  $\pm 200\text{mV}$  from steady state. This parameter is sampled and not 100% tested.

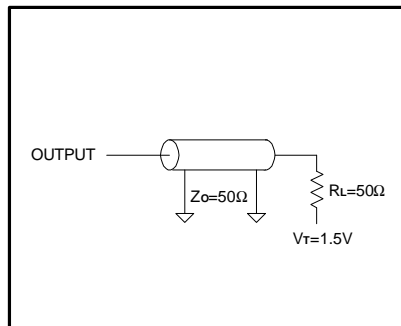
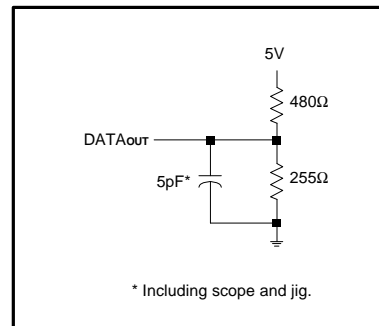
**Timing Waveforms (continued)**
**Write Cycle 1<sup>(6)</sup>  
(Write Enable Controlled)**

**Write Cycle 2  
(Chip Enable Controlled)**


- Notes:
1.  $t_{AS}$  is measured from the address valid to the beginning of Write.
  2. A Write occurs during the overlap ( $t_{WP}$ ) of a low  $\overline{CE}$  and a low  $\overline{WE}$ .
  3.  $t_{WR}$  is measured from the earliest of  $\overline{CE}$  or  $\overline{WE}$  going high to the end of the Write cycle
  4. If the  $\overline{CE}$  low transition occurs simultaneously with the  $\overline{WE}$  low transition or after the  $\overline{WE}$  transition, outputs remain in a high impedance state.
  5.  $t_{CW}$  is measured from the later of  $\overline{CE}$  going low to the end of Write.
  6.  $\overline{OE}$  is continuously low. ( $\overline{OE} = V_{IL}$ )
  7. Transition is measured  $\pm 200\text{mV}$  from steady state. This parameter is sampled and not 100% tested.



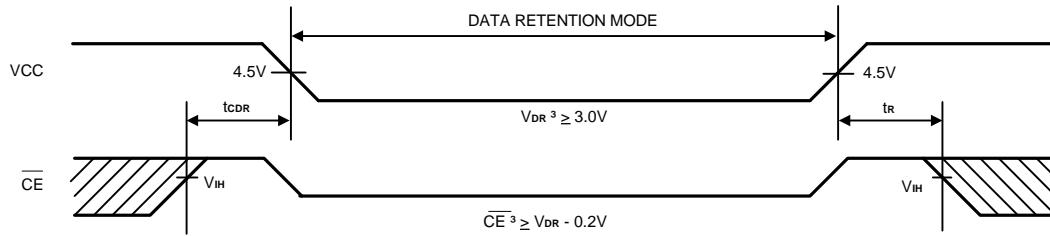
**AC Test Conditions**

|  |                     |
|--|---------------------|
| Input Pulse Levels                       | 0V to 3.0V          |
| Input Rise and Fall Time                 | 3 ns                |
| Input and Output Timing Reference Levels | 1.5V                |
| Output Load                              | See Figures 1 and 2 |


**Figure 1. Output Load**

**Figure 2. Output Load for  $t_{CLZ}$ ,  $t_{OLZ}$ ,  $t_{CHZ}$ ,  $t_{OHZ}$ ,  $t_{WHZ}$ , and  $t_{OW}$** 
**Data Retention Characteristics** ( $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ )

| Symbol     | Parameter                           | Min.       | Max. | Unit | Conditions   |
|------------|-------------------------------------|------------|------|------|--|
| $V_{DR}$   | VCC for Data Retention              | 3          | 5.5  | V    | $\overline{CE} \geq VCC - 0.2V$  |
| $I_{CCDR}$ | Data Retention Current              | -          | 1    | mA   | $VCC = 3.0V$<br>$\overline{CE} \geq VCC - 0.2V$<br>$V_{IN} \geq VCC - 0.2V$ or<br>$V_{IN} \leq 0.2V$ |
| $t_{CDR}$  | Chip Disable to Data Retention Time | 0          | -    | ns   | See Retention Waveform   |
| $t_R$      | Operation Recovery Time             | $T_{RC}^*$ | -    | ms   |  |

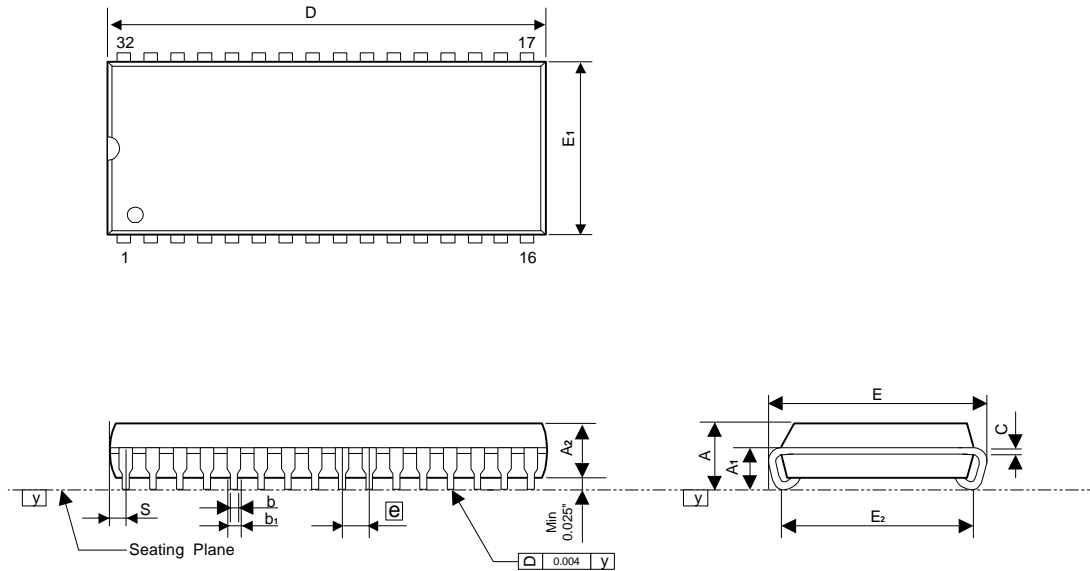
 $t_{RC}$  = Read Cycle Time

**Low VCC Data Retention Waveform**

**Ordering Information**

| Part No.      | Access Time (ns) | Operating Current Max. (mA) | CMOS Standby Max. (mA) | Package        |
|---------------|------------------|-----------------------------|------------------------|----------------|
| A6173081S-12  | 12               | 170                         | 8                      | 32L 300mil SOJ |
| A6173081SW-12 |                  |                             |                        | 32L 400mil SOJ |
| A6173081S-15  | 15               | 165                         | 8                      | 32L 300mil SOJ |
| A6173081SW-15 |                  |                             |                        | 32L 400mil SOJ |

**Package Information**
**SOJ 32L(300mil) Outline Dimensions**

unit: inches/mm



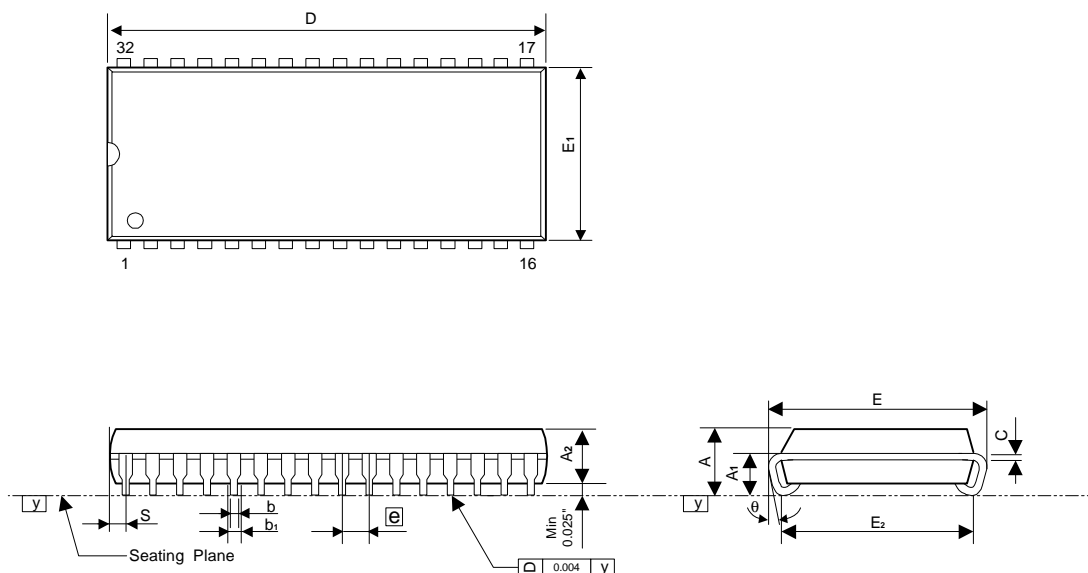
| Symbol | Dimensions in inches |       |       | Dimensions in mm |       |       |
|--------|----------------------|-------|-------|------------------|-------|-------|
|        | Min                  | Nom   | Max   | Min              | Nom   | Max   |
| A      | 0.128                | 0.132 | 0.140 | 3.25             | 3.35  | 3.56  |
| A1     | 0.052                | -     | -     | 2.08             | -     | -     |
| A2     | 0.095                | 0.100 | 0.105 | 2.41             | 2.54  | 2.67  |
| b      | 0.016                | 0.018 | 0.020 | 0.41             | 0.46  | 0.51  |
| b1     | 0.026                | 0.028 | 0.032 | 0.66             | 0.71  | 0.81  |
| C      | 0.006                | 0.008 | 0.012 | 0.15             | 0.20  | 0.30  |
| D      | 0.820                | 0.825 | 0.830 | 20.83            | 20.96 | 21.08 |
| E      | 0.330                | 0.335 | 0.340 | 8.39             | 8.51  | 8.63  |
| E1     | 0.295                | 0.300 | 0.305 | 7.49             | 7.62  | 7.75  |
| E2     | 0.260                | 0.267 | 0.274 | 6.61             | 6.78  | 6.96  |
| [e]    | -                    | 0.050 | -     | -                | 1.27  | -     |
| S      | -                    | -     | 0.048 | -                | -     | 1.22  |
| y      | -                    | -     | 0.004 | -                | -     | 0.10  |

**Notes:**

1. The maximum value of dimension D includes end flash.
2. Dimension E does not include resin fins.
3. Dimension E1 is for PC Board surface mount pad pitch design reference only.
4. Dimension S includes end flash.

**Package Information**
**SOJ 32L (400mil) Outline Dimensions**

unit: inches/mm



| Symbol | Dimensions in inches |       |       | Dimensions in mm |       |       |
|--------|----------------------|-------|-------|------------------|-------|-------|
|        | Min                  | Nom   | Max   | Min              | Nom   | Max   |
| A      | 0.131                | 0.138 | 0.145 | 3.33             | 3.51  | 3.68  |
| A1     | 0.082                | -     | -     | 2.08             | -     | -     |
| A2     | 0.105                | 0.110 | 0.115 | 2.67             | 2.79  | 2.91  |
| b      | 0.016                | 0.018 | 0.020 | 0.41             | 0.46  | 0.51  |
| b1     | 0.026                | 0.028 | 0.032 | 0.66             | 0.71  | 0.81  |
| C      | 0.006                | 0.008 | 0.011 | 0.15             | 0.20  | 0.28  |
| D      | 0.820                | 0.825 | 0.830 | 20.83            | 20.96 | 21.08 |
| E      | 0.435                | 0.440 | 0.445 | 11.05            | 11.18 | 11.31 |
| E1     | 0.395                | 0.400 | 0.405 | 10.03            | 10.16 | 10.29 |
| E2     | 0.360                | 0.370 | 0.380 | 9.15             | 9.40  | 9.65  |
| e      | -                    | 0.050 | -     | -                | 1.27  | -     |
| S      | -                    | -     | 0.045 | -                | -     | 1.14  |
| y      | -                    | -     | 0.004 | -                | -     | 0.10  |
| θ      | -5°                  | 2°    | 6°    | -5°              | 2°    | 6°    |

**Notes:**

1. The maximum value of dimension D includes end flash.
2. Dimension E does not include resin fins.
3. Dimension E1 is for PC Board surface mount pad pitch design reference only.
4. Dimension S includes end flash.