AMERICAN MICROSYSTEMS, INC.

FS6146

VCXO Clock Generator IC

April 2000

Preliminary

1.0 Features

- On-chip tunable voltage-controlled crystal oscillator circuitry (VCXO) allows precise system frequency tuning (pull range typically 300ppm)
- VCXO tuning range: 0-3V
- Uses inexpensive fundamental-mode crystals
- Integrated phase-locked loop (PLL) multiplies VCXO frequency to the higher system frequencies needed
- 5V core supply voltage (contact factory for 3.3V)
- 3.3V / 5V output supply voltage
- Small circuit board footprint (8-pin 0.150″ SOIC)
- Custom frequency selections available - contact your local AMI Sales Representative for more information

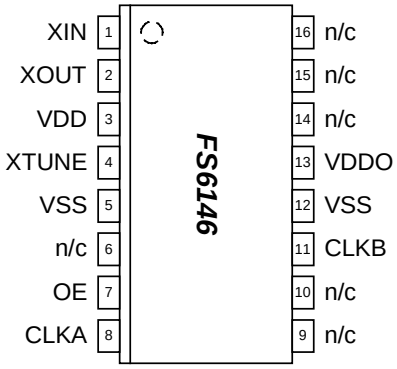
2.0 Description

The FS6146 is a monolithic CMOS clock generator IC designed to minimize cost and component count in digital video/audio systems.

At the core of the FS6146 is circuitry that implements a voltage-controlled crystal oscillator when an external resonator is attached. The VCXO allows device frequencies to be precisely adjusted for use in systems that have frequency matching requirements, such as digital satellite receivers.

A high-resolution phase-locked loop generates the output clock frequencies (CLKA and CLKB). These frequencies are phase-locked and frequency-locked to the VCXO frequency.

Figure 1: Pin Configuration



16-pin (0.150″) SOIC

Table 1: Crystal / Output Frequencies

DEVICE	f_{XIN} (MHz)	CLKA (MHz)	CLKB (MHz)
FS6146-01	10.000	40.000	80.000

NOTE: Contact AMI for custom PLL frequencies

Figure 2: Block Diagram

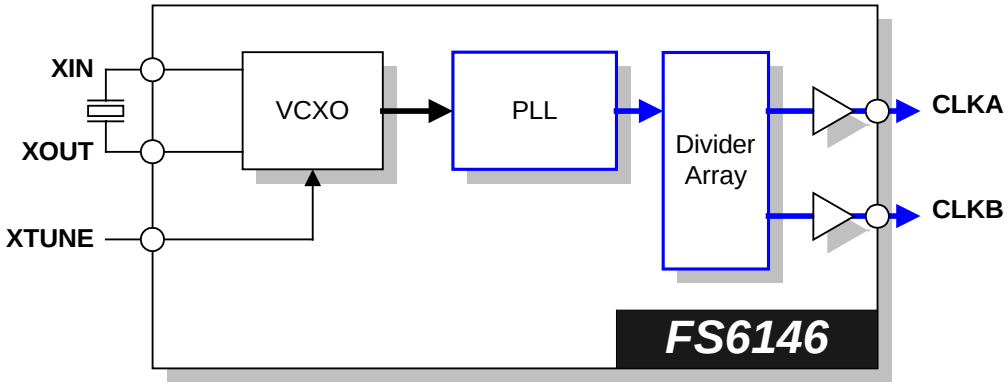


Table 2: Pin Descriptions

Key: AI = Analog Input; AO = Analog Output; DI = Digital Input; DI^U = Input with Internal Pull-Up; DI_D = Input with Internal Pull-Down; DIO = Digital Input/Output; DI-3 = Three-Level Digital Input, DO = Digital Output; P = Power/Ground; # = Active Low pin

PIN	TYPE	NAME	DESCRIPTION
1	AI	XIN	VCXO Crystal Feedback
2	AO	XOUT / FREF	VCXO Crystal Drive / External Reference Clock Input
3	P	VDD	Core Power Supply
4	AI	XTUNE	VCXO Tune Input
5	P	VSS	Ground
6	-	N/C	No Connection
7	DI^U	OE	Output Enable
8	DO	CLKA	Clock Output “A”
9	-	N/C	No Connection
10	-	N/C	No Connection
11	DO	CLKB	Clock Output “B”
12	P	VSS	Ground
13	P	VDDO	Output Power Supply (must be less than or equal to VDD)
14	-	N/C	No Connection
15	-	N/C	No Connection
16	-	N/C	No Connection

3.0 Functional Block Description

3.1 Phase-Locked Loop (PLL)

The on-chip PLL is a standard frequency- and phase-locked loop architecture. The PLL multiplies the reference oscillator to the desired frequency by a ratio of integers. The frequency multiplication is exact with a zero synthesis error.

3.2 Voltage-Controlled Crystal Oscillator (VCXO)

The VCXO provides a tunable, low-jitter frequency reference for the rest of the FS6146 system components. Loading capacitance for the crystal is internal to the FS6146. No external components (other than the crystal resonator itself) are required for operation of the VCXO.

Continuous fine-tuning of the VCXO frequency is accomplished by varying the voltage on the XTUNE pin.

The oscillator operates the crystal resonator in the parallel-resonant mode. Crystal warping, or the “pulling” of the crystal oscillation frequency, is accomplished by altering the effective load capacitance presented to the crystal by the oscillator circuit. The actual amount that changing the load capacitance alters the oscillator frequency will be dependent on the characteristics of the crystal as well as the oscillator circuit itself.

Specifically, the motional capacitance of the crystal (usually referred to by crystal manufacturers as C_1), the static capacitance of the crystal (C_0), and the load capacitance (C_L) of the oscillator determine the “warping” or “pulling” capability of the crystal in the oscillator circuit.

A simple formula to obtain the warping capability of a crystal oscillator is:

$$\Delta f\ (ppm) = \frac{C_1 \times (C_{L2} - C_{L1}) \times 10^6}{2 \times (C_0 + C_{L2}) \times (C_0 + C_{L1})}$$

where C_{L1} and C_{L2} are the two extremes of the applied load capacitance.

EXAMPLE: A crystal with the following parameters is used. With C_1 = 0.02pF, C_0 = 5pF, C_{L1} = 10pF, and C_{L2} = 22.66pF, the tuning range is

$$\Delta f = \frac{0.02 \times (22.66 - 10) \times 10^6}{2 \times (5 + 22.66) \times (5 + 10)} = 305\,ppm.$$

4.0 Electrical Specifications

Table 3: Absolute Maximum Ratings

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These conditions represent a stress rating only, and functional operation of the device at these or any other conditions above the operational limits noted in this specification is not implied. Exposure to maximum rating conditions for extended conditions may affect device performance, functionality, and reliability.

PARAMETER	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage (V_{SS} = ground)	V_{DD}	V_{SS}-0.5	7	V
Input Voltage, dc	V_I	V_{SS}-0.5	V_{DD}+0.5	V
Output Voltage, dc	V_O	V_{SS}-0.5	V_{DD}+0.5	V
Input Clamp Current, dc (V_I < 0 or V_I > V_{DD})	I_{IK}	-50	50	mA
Output Clamp Current, dc (V_I < 0 or V_I > V_{DD})	I_{OK}	-50	50	mA
Storage Temperature Range (non-condensing)	T_S	-65	150	°C
Ambient Temperature Range, Under Bias	T_A	-55	125	°C
Junction Temperature	T_J		125	°C
Lead Temperature (soldering, 10s)			260	°C
Input Static Discharge Voltage Protection (MIL-STD 883E, Method 3015.7)			2	kV

CAUTION: ELECTROSTATIC SENSITIVE DEVICE

Permanent damage resulting in a loss of functionality or performance may occur if this device is subjected to a high-energy electrostatic discharge.

Table 4: Operating Conditions

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	MIN.	TYP.	MAX.	UNITS
Supply Voltage	V_{DD}	5V ± 10%	4.75	5	5.25	V
Ambient Operating Temperature Range	T_A		0		70	°C
Crystal Resonator Frequency	f_{XTAL}	Fundamental Mode	5	13.5	18	MHz
Crystal Resonator Motional Capacitance	$C_{1(xtal)}$	AT cut		25		fF
Crystal Loading Capacitance	$C_{L(xtal)}$	AT cut		14		pF

Table 5: DC Electrical Specifications

Unless otherwise stated, V_{DD} = 5V ± 10%, no load on any output, and ambient temperature range T_A = 0°C to 70°C. Parameters denoted with an asterisk (*) represent nominal characterization data and are not production tested to any specific limits. Where given, MIN and MAX characterization data are ±3σ from typical. Negative currents indicate current flows out of the device.

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	MIN.	TYP.	MAX.	UNITS
Overall						
Supply Current, Dynamic, with Loaded Outputs	I_{DD}	f_{XTAL} = 13.5MHz; C_L = 10pF		20		mA
Voltage Controlled Crystal Oscillator - VDD=5.0V						
Crystal Loading Capacitance	$C_{L(xtal)}$	As seen by a crystal connected to XIN and XOUT (@ V_{XTUNE} = 1.65V)		14		pF
Crystal Resonator Motional Capacitance	$C_{1(xtal)}$	AT cut		25		fF
VCXO Tuning Range		f_{XTAL} = 13.5MHz; $C_{L(xtal)}$ = 14pF; $C_{1(xtal)}$ = 25fF		300		ppm
VCXO Tuning Characteristic		Note: positive ΔF for positive ΔV		100		ppm/V
Crystal Drive Level		R_{XTAL}=20Ω; $C_{L(xtal)}$ = 14pF		200		uW
Clock Outputs (CLKA, CLKB) - VDDO=3.3V						
High-Level Output Source Current *	I_{OH}	V_O = 2.0V		-40		mA
Low-Level Output Sink Current *	I_{OL}	V_O = 0.4V		17		mA
Output Impedance *	z_{OH}	V_O = 0.1V_{DD}; output driving high		25		Ω
	z_{OL}	V_O = 0.1V_{DD}; output driving low		25		
Short Circuit Source Current *	I_{OSH}	V_O = 0V; shorted for 30s, max.		-55		mA
Short Circuit Sink Current *	I_{OSL}	V_O = 5V; shorted for 30s, max.		55		mA

Table 6: AC Timing Specifications

Unless otherwise stated, V_{DD} = 5V ± 10%, no load on any output, and ambient temperature range T_A = 0°C to 70°C. Parameters denoted with an asterisk (*) represent nominal characterization data and are not production tested to any specific limits. Where given, MIN and MAX characterization data are ±3σ from typical.

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	CLOCK (MHz)	MIN.	TYP.	MAX.	UNITS
Overall							
VCXO Stabilization Time *	$t_{VCXOSTB}$	From power valid			10		ms
PLL Stabilization Time *	t_{PLLSTB}	From VCXO stable			500		us
Output Frequency Synthesis Error		(unless otherwise noted in Frequency Table)				0	ppm
Clock Output (CLK)							
Duty Cycle *		Ratio of high pulse width (as measured from rising edge to next falling edge at V_{DD}/2) to one clock period		45		55	%
Jitter, Period (peak-peak) *	$t_{j(\Delta P)}$	From rising edge to next rising edge at V_{DD}/2, C_L = 10pF			300		ps
Jitter, Long Term ($\sigma_y(\tau)$) *	$t_{j(LT)}$	From 0-500µs at V_{DD}/2, C_L = 10pF compared to ideal clock source			150		ps
Rise Time *	t_r	V_{DD} = 5V; V_O = 0.5V to 4.5V; C_L = 10pF					ns
Fall Time *	t_f	V_{DD} = 5V; V_O = 4.5V to 0.5V; C_L = 10pF					ns

5.0 Package Information

Table 7: 16-pin SOIC (0.150") Package Dimensions

	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.061	0.068	1.55	1.73
A1	0.004	0.0098	0.102	0.249
A2	0.055	0.061	1.40	1.55
B	0.013	0.019	0.33	0.49
C	0.0075	0.0098	0.191	0.249
D	0.386	0.393	9.80	9.98
E	0.150	0.157	3.81	3.99
e	0.050 BSC		1.27 BSC	
H	0.230	0.244	5.84	6.20
h	0.010	0.016	0.25	0.41
L	0.016	0.035	0.41	0.89
Θ	0°	8°	0°	8°

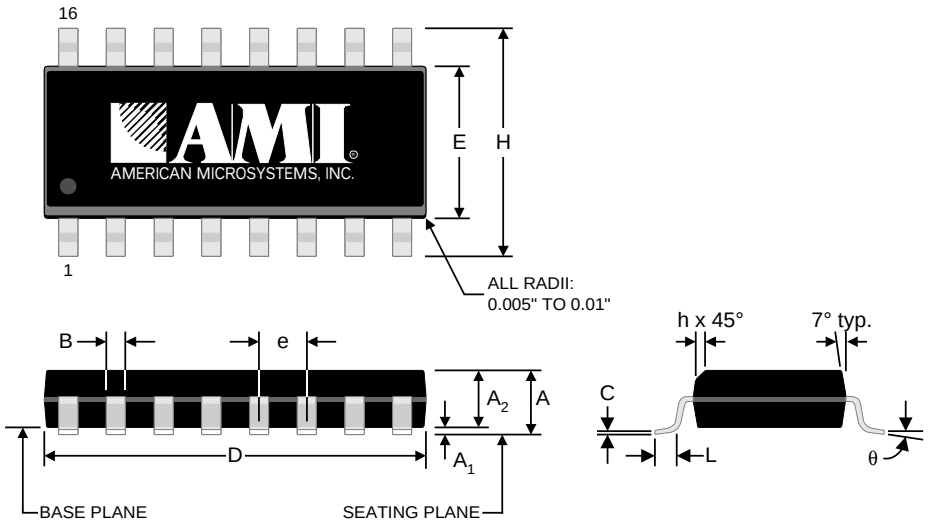


Table 8: 16-pin SOIC (0.150") Package Characteristics

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	TYP.	UNITS
Thermal Impedance, Junction to Free-Air 16-pin 0.150" SOIC	Θ_{JA}	Air flow = 0 m/s	109	°C/W
Lead Inductance, Self	L_{11}	Corner lead	4.0	nH
		Center lead	3.0	
Lead Inductance, Mutual	L_{12}	Any lead to any adjacent lead	0.4	nH
Lead Capacitance, Bulk	C_{11}	Any lead to V_{SS}	0.5	pF

6.0 Ordering Information

Table 9: Device Ordering Codes

ORDERING CODE	DEVICE NUMBER	PACKAGE TYPE	OPERATING TEMPERATURE RANGE	SHIPPING CONFIGURATION
11640-823	FS6146-01	8-pin (0.150") SOIC (Small Outline Package)	0° C to 70° C (Commercial)	Tape and Reel
11640-833	FS6146-01	8-pin (0.150") SOIC (Small Outline Package)	0° C to 70° C (Commercial)	Tubes

7.0 Revision Information

DATE	PAGE	DESCRIPTION
4/26/00	2	Fixed formatting errors

American Microsystems, Inc., 2300 Buckskin Rd., Pocatello, ID 83201, (208) 233-4690, FAX (208) 234-6796, WWW Address: http://www.amis.com E-mail: tgp@amis.com