AMERICAN MICROSYSTEMS, INC.

FS6158-01

Two-Way/Four Way Motherboard Clock Generator/Buffer IC

September 2000

1.0 Features

- Generates the Host and Memory clocks required for 2-way and 4-way multi-processor (MP) clock-partitioned platforms, including:
  - Six differential current-mode Host clock pairs
  - Two 3.3V Memory Reference clocks
  - 66.67MHz and 14.318MHz 3.3V Reference clocks for the FS6159 device
  - Three optional 33.3MHz 1.8V APIC clocks
- Control of current-mode Host clocks via IREF current programming pin and ISEL_0:1 current multiplier pins
- Optional APIC clocks enabled via APICON input (see Table 5 for Pins 21-23 configuration)
- Host clock frequency selection via the SEL_A, SEL_B, and SEL133/100# pins
- Active-low PWR_DWN# signal allows one complete clock cycle on each clock outputs and then shuts down the crystal oscillator, PLL, and disables outputs
- Spread-spectrum modulation (-0.5% at 31.5kHz) of Host, Memory, APIC, and 66MHz Reference clocks, enabled via SS_EN# input
- Supports test mode and tristate output control to facilitate board testing
- Available in a 48-pin SSOP and TSSOP

Figure 1: Block Diagram

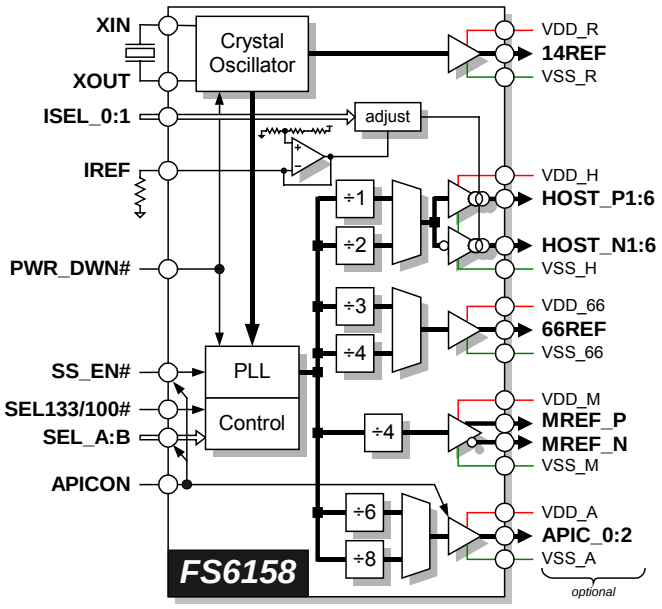

Figure 2: Pin Configuration

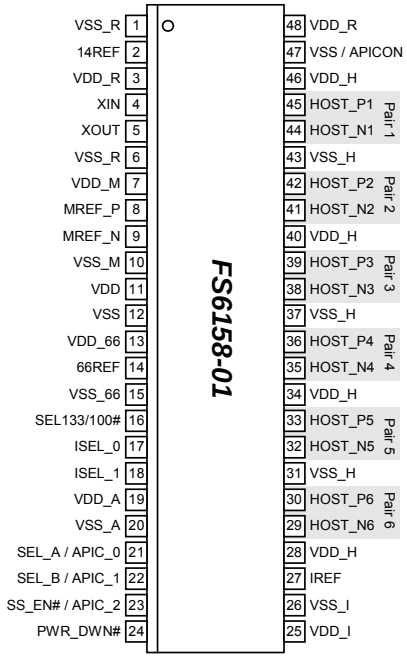

Table 1: Clock Parameters

CLOCK GROUP	# PINS	SUPPLY VOLTAGE	SUPPLY GROUP	FREQ. (MHz)	PHASE	SKEW (MAX)
HOST_P	6	3.3V	VDD_H	133.33 100.00	0°	100ps
HOST_N	6				180°	Pair to Pair
MREF_P	1	3.3V	VDD_M	66.67 50.00	0°	-
MREF_N	1				180°	
66REF	1	3.3V	VDD_66	66.67	0°	-
14REF	1	3.3V	VDD_R	14.318	0°	-
APIC (*optional*)	3	1.8V	VDD_A	33.33	0°	-

Table 2: Pin Descriptions

Key: AI = Analog Input; AO = Analog Output; DI = Digital Input; DI^U = Input with Internal Pull-Up; DI_D = Input with Internal Pull-Down; DIO = Digital Input/Output; DI-3 = Three-Level Digital Input, DO = Digital Output; P = Power/Ground; # = Active-low pin

PIN	TYPE	NAME	DESCRIPTION	SUPPLY
47	DI	APICON	Enables (logic-high) or disables (logic-low) the optional 1.8V APIC clocks	VDD_R
21	DIO	APIC_0	One of three optional APIC clocks, enabled or disabled by APICON	VDD_A
		SEL_A	One of two frequency select inputs, used in combination with SEL133/100#. Input signal levels are referred to VDD_H (3.3V) if APICON is low, or to VDD_A (1.8V) if APICON is high.	VDD_A, VDD_H
22	DIO	APIC_1	One of three optional APIC clocks, enabled or disabled by APICON	VDD_A
		SEL_B	One of two frequency select inputs, used in combination with SEL133/100#. Input signal levels are referred to VDD_H (3.3V) if APICON is low, or to VDD_A (1.8V) if APICON is high.	VDD_A, VDD_H
23	DIO	APIC_2	One of three optional APIC clocks, enabled or disabled by APICON	VDD_A
		SS_EN#	Active-low spread spectrum enable turns on spread spectrum modulation of PLL clocks. Input levels are referred to VDD_H (3.3V) if APICON is low, or to VDD_A (1.8V) if APICON is high.	VDD_A, VDD_H
2	DO	14REF	One 14.318MHz clock output, provided as a reference clock to the companion clock device	VDD_R
14	DO	66REF	One 66.67MHz clock output, provided as a reference clock to the companion clock device	VDD_66
27	AI	IREF	A fixed precision resistor from this pin to ground provides a reference current used for the differential current-mode HOST clock outputs	VDD_I
17, 18	DI	ISEL_0 ISEL_1	The logic setting on these two pins selects the multiplying factor of the IREF reference current for the HOST pair outputs	VDD_66
45, 44	AO	HOST_P1 HOST_N1	Host clock pair #1; one of six pairs of current-steering differential current-mode outputs. The current is established via a reference current at IREF and a multiplying factor set by ISEL_0:1	VDD_H
42, 41	AO	HOST_P2 HOST_N2	Host clock pair #2; one of six pairs of current-steering differential current-mode outputs	VDD_H
39, 38	AO	HOST_P3 HOST_N3	Host clock pair #3; one of six pairs of current-steering differential current-mode outputs	VDD_H
36, 35	AO	HOST_P4 HOST_N4	Host clock pair #4; one of six pairs of current-steering differential current-mode outputs	VDD_H
33, 32	AO	HOST_P5 HOST_N5	Host clock pair #5; one of six pairs of current-steering differential current-mode outputs	VDD_H
30, 29	AO	HOST_P6 HOST_N6	Host clock pair #6; one of six pairs of current-steering differential current-mode outputs	VDD_H
8	DO	MREF_P	One clock in a pair of outputs provided as a reference clock to a memory clock driver	VDD_M
9	DO	MREF_N	One clock (180° out of phase with MREF_P) in a pair of outputs provided as a reference clock to a memory clock driver	VDD_M
24	DI	PWR_DWN#	Asynchronous active-low LVTTL power-down signal shuts down oscillator and PLL, puts all clocks in low state. Complete clock cycles on all outputs will occur before shut down begins.	VDD_I
16	DI	SEL133/100#	Selects 133MHz or 100MHz Host clock frequency	VDD_66
11	P	VDD	3.3V core power supply	-
19	P	VDD_A	1.8V power supply for optional APIC clocks or a 3.3V supply to pins 21-23	-
13	P	VDD_66	3.3V power supply for 66REF clock output	-
28, 34, 40, 46	P	VDD_H	3.3V power supply for the differential HOST clock outputs	-
25	P	VDD_I	3.3V power supply for IREF current reference input	-
7	P	VDD_M	3.3V power supply for MREF clock outputs	-
3, 48	P	VDD_R	3.3V power supply for the 14REF clock output and the crystal oscillator	-
12	P	VSS	Core Ground	-
15	P	VSS_66	Ground for the 66REF clock output	-
20		VSS_A	Ground for the APIC clock outputs	
31, 37, 43	P	VSS_H	Ground for the differential HOST clock outputs	-
26	P	VSS_I	Ground for IREF current reference input	-
10	P	VSS_M	Ground for the MREF clock outputs	-
1, 6	P	VSS_R	Ground for the 14REF clock output and the crystal oscillator	-
4	AI	XIN	14.318MHz crystal oscillator input	VDD_R
5	AO	XOUT	14.318MHz crystal oscillator output	VDD_R

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2.0 Programming Information

Table 3: Function/Clock Enable Configuration

CONTROL INPUTS (2)				CLOCK OUTPUTS (MHz)					
PWR_DWN#	SEL133/100#	SEL_A	SEL_B	HOST_P1:6	HOST_N1:6	MREF_P, MREF_N	66REF	APIC_0:2 (*optional*)	14REF
1	0	0	0	100.00	100.00	50.00	66.67	33.33	14.318
1	0	0	1	100.00	100.00	low (1)	low (1)	low (1)	low (1)
1	0	1	0	reserved	reserved	reserved	reserved	reserved	reserved
1	0	1	1	tristate	tristate	tristate	tristate	tristate	tristate
1	1	0	0	133.33	133.33	66.67	66.67	33.33	14.318
1	1	0	1	reserved	reserved	reserved	reserved	reserved	reserved
1	1	1	0	reserved	reserved	reserved	reserved	reserved	reserved
1	1	1	1	XIN÷2	XIN÷2	XIN÷4	XIN÷4	XIN÷8	XIN
0	X	X	X	2× IREF	tristate	low	low	low	low

1. Certain clock outputs may be disabled through a combination of SEL_A, SEL_B, and SEL133/100# logic states as defined in Table 3. Enabled clocks will continue to run while disabled clocks are stopped low. Note that if clocks are disabled while active, glitches may occur.

Table 4: Synthesis Error

CLOCK	TARGET (MHz)	ACTUAL (MHz)	DEVIATION (ppm)
HOST_P1:6, HOST_N1:6	100.0000	99.9963	-36.657
	133.3333	133.3072	-195.924
MREF_P, MREF_N	50.0000	49.9982	-36.657
	66.6667	66.6536	-195.924
66REF	66.6667	66.6642	-36.657
APIC_0:2	33.3333	33.3321	-36.657

1. 48MHz USB clock is required to be +167ppm off from 48.000MHz to conform to USB standards.
2. Spread spectrum is disabled

Table 5: APICON Control

APICON	FREQUENCY SELECT CONTROL / APIC CLOCKS		
PIN 47	PIN 21	PIN 22	PIN 23
0	SEL_A Input (LVTTL)	SEL_B Input (LVTTL)	SS_EN# Input (LVTTL)
1	APIC_0 Output / SEL_A Latched Input	APIC_1 Output / SEL_B Latched Input	APIC_2 Output / SS_EN# Latched Input

3.0 HOST Buffer Current Control

The current supplied at the HOST outputs is controlled by two parameters:

1) the value of the programming resistor from the IREF pin to ground (VSS), and
2) the multiplier factor determined by the logic setting of the ISEL_0 and ISEL_1 pins.

3.1 Current Reference

The HOST output current is a mirrored and scaled copy of the reference current flowing through the programming resistor on the IREF pin. Conceptually, the circuit given in Figure 2 shows how the mirror current is generated.

The voltage that appears at the IREF pin is one-third of the voltage at the VDD_I pin. The reference current is

$$I_{REF} = \frac{\left(\frac{1}{3} \times \mathrm{VDD\_I}\right)}{R_{IREF}}.$$

3.2 Current Scaling

The mirrored reference current can be increased by adding one or more copies of the mirror current together. The additional current is controlled by the logic settings on the ISEL_0 and ISEL_1 pins.

Table 6: Current Multiplier

ISEL_0	ISEL_1	MULTPLIER
0	0	$I_O = 5\times I_{REF}$
0	1	$I_O = 6\times I_{REF}$
1	0	$I_O = 4\times I_{REF}$
1	1	$I_O = 7\times I_{REF}$

Figure 2: Current Reference Circuit

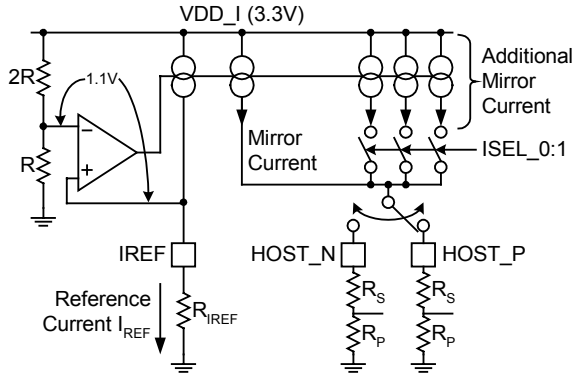


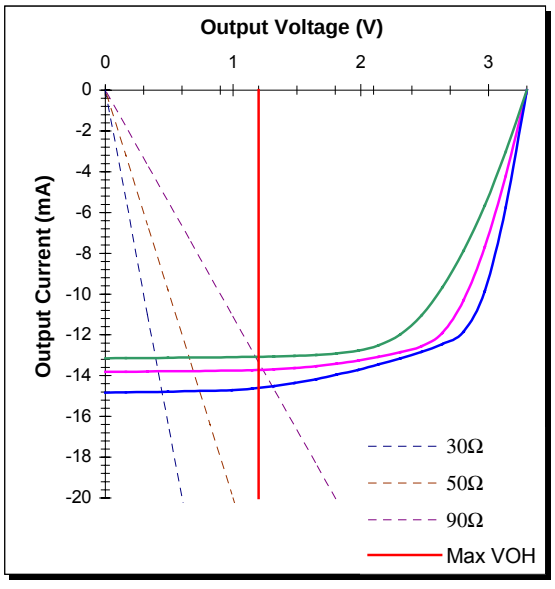
Table 7: HOST Current Selection

PROGRAM RESISTOR R_{IREF}	REFERENCE CURRENT I_{REF}	CURRENT MULTIPLIER	TRACE IMPEDANCE	OUTPUT VOLTAGE
475Ω (1%)	2.32mA	$I_O = 5\times I_{REF}$	60Ω	0.71V
			50Ω	0.59V
475Ω (1%)	2.32mA	$I_O = 6\times I_{REF}$	60Ω	0.85V
			50Ω	0.71V
475Ω (1%)	2.32mA	$I_O = 4\times I_{REF}$	60Ω	0.56V
			50Ω	0.47V
475Ω (1%)	2.32mA	$I_O = 7\times I_{REF}$	60Ω	0.99V
			50Ω	0.82V
221Ω (1%)	5mA	$I_O = 5\times I_{REF}$	30Ω	0.75V
			25Ω	0.62V
221Ω (1%)	5mA	$I_O = 6\times I_{REF}$	30Ω	0.90V
			25Ω	0.75V
221Ω (1%)	5mA	$I_O = 4\times I_{REF}$	30Ω	0.60V
			25Ω	0.50V
221Ω (1%)	5mA	$I_O = 7\times I_{REF}$	30Ω	1.05V
			25Ω	0.84V

NOTE: Shaded row indicates the Primary System Configuration

Table 8: HOST Buffer Clock Outputs

Output Voltage (V)	HIGH DRIVE CURRENT (mA) AT PRIMARY SYSTEM CONFIGURATION		
	MIN.	TYP.	MAX.
3.30	0.00	0.00	0.00
3.14	-3.03	-4.22	-5.76
2.97	-5.66	-7.68	-9.86
2.81	-7.87	-10.30	-11.85
2.64	-9.67	-11.91	-12.45
2.48	-11.05	-12.56	-12.84
2.31	-11.98	-12.85	-13.16
2.14	-12.52	-13.07	-13.45
1.98	-12.77	-13.26	-13.72
1.81	-12.91	-13.42	-13.96
1.65	-12.99	-13.54	-14.17
1.48	-13.04	-13.64	-14.36
1.32	-13.07	-13.70	-14.52
1.15	-13.08	-13.73	-14.64
0.99	-13.09	-13.75	-14.71
0.82	-13.11	-13.76	-14.74
0.66	-13.12	-13.78	-14.76
0.49	-13.13	-13.79	-14.78
0.33	-13.13	-13.80	-14.80
0.16	-13.14	-13.81	-14.82
0.00	-13.15	-13.82	-14.83



Data in this table represents nominal characterization data only

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4.0 Power Management

The PWR_DWN# signal is an asynchronous, active-low LVTTL input that places the device in a low power inactive state without removing power from the device. All internal clocks are turned off, and all clock outputs are held low.

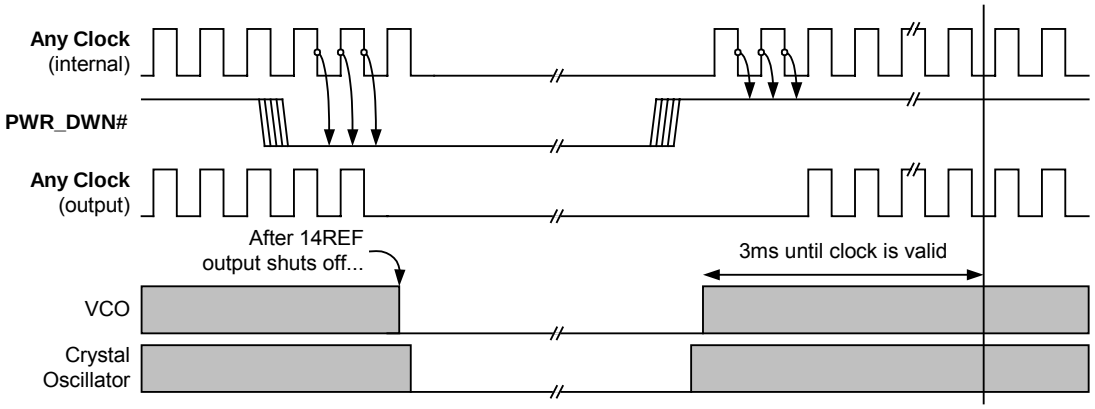
Since PWR_DWN# is asynchronous, the signal is synchronized internally to each individual clock. As shown in Figure 3, a falling-rising-falling edge sequence on any individual clock output is required before that clock output is disabled low. This edge sequence ensures that one complete clock cycle will occur before the clock stops.

Table 9: Latency Table

SIGNAL	SIGNAL STATE		LATENCY		
				MIN.	MAX.
PWR_DWN#	0	Power OFF	Output:	2 clocks	3 clocks
			Device:	2× 14REF clocks	3× 14REF clocks
	1	Power ON	3ms		

Upon the release of PWR_DWN# (power-up), external circuitry should allow a minimum of 3ms for the PLL to lock before enabling any clocks.

Figure 3: PWR_DWN# Timing



Shaded regions in the Crystal Oscillator and VCO waveforms indicate that the clock is valid and the Crystal Oscillator and VCO are active.

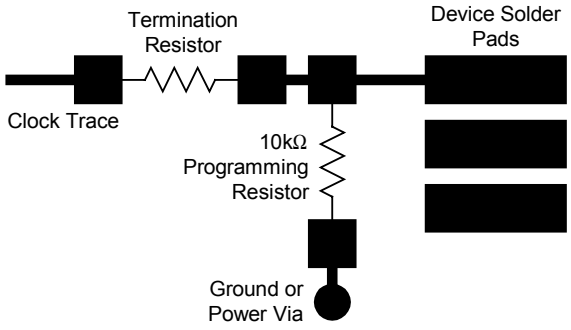
5.0 Dual Function I/O Pins

Several pins on this device serve as dual function input/output pins. During the initial application of VDD to the device, this type of pin functions as an input pin. Upon completion of power-up, the logic state present on the pin is latched internally, and the pin is converted to an output driver.

An external 10kΩ pull-down resistor to ground is required for a logic low and a 10kΩ pull-up resistor to the clock output VDD is required for a logic high. The 10kΩ resistor presents an insignificant load to the output driver that should not affect the output clock.

Note that the latching of the logic state occurs only on the application of the chip supply voltage (VDD). The logic state on the pin is not latched if the PWR_DWN# signal is used to power-down the device with VDD still applied.

Figure 4: I/O Pin Programming



6.0 Electrical Specifications

Table 10: Absolute Maximum Ratings

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These conditions represent a stress rating only, and functional operation of the device at these or any other conditions above the operational limits noted in this specification is not implied. Exposure to maximum rating conditions for extended conditions may affect device performance, functionality, and reliability.

PARAMETER	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage (V_{SS} = ground)	V_{DD}	V_{SS}-0.5	7	V
Input Voltage, dc	V_I	V_{SS}-0.5	V_{DD}+0.5	V
Output Voltage, dc	V_O	V_{SS}-0.5	V_{DD}+0.5	V
Input Clamp Current, dc (V_I < 0 or V_I > V_{DD})	I_{IK}	-50	50	mA
Output Clamp Current, dc (V_I < 0 or V_I > V_{DD})	I_{OK}	-50	50	mA
Storage Temperature Range (non-condensing)	T_S	-65	150	°C
Ambient Temperature Range, Under Bias	T_A	-55	125	°C
Junction Temperature	T_J		125	°C
Lead Temperature (soldering, 10s)			260	°C
Input Static Discharge Voltage Protection (MIL-STD 883E, Method 3015.7)			2	kV

CAUTION: ELECTROSTATIC SENSITIVE DEVICE

Permanent damage resulting in a loss of functionality or performance may occur if this device is subjected to a high-energy electrostatic discharge.

Table 11: Operating Conditions

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	MIN.	TYP.	MAX.	UNITS
Supply Voltage	V_{DD}	Core (VDD)	3.135	3.3	3.465	V
		Clock Buffers (VDD_66, VDD_H, VDD_I, VDD_M, VDD_R)	3.135	3.3	3.465	
		APIC Clock Buffers (VDD_A)	1.65	1.8	1.95	
Operating Temperature Range	T_A		0		70	°C
Crystal Resonator Frequency	f_{XTAL}		14.316	14.318	14.32	MHz
Crystal Resonator Load Capacitance	C_{XL}	XIN, XOUT pins	13.5	18	22.5	pF
Load Capacitance	C_L	MREF_P, MREF_N	10		30	pF
		APIC_0:2	10		20	
		66REF	10		20	
		14REF	10		20	
Load Resistance	R_L	HOST_P1 to HOST_P6, HOST_N1 to HOST_N6	20		105	Ω

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Table 12: DC Electrical Specifications

Unless otherwise stated, all power supplies = 3.3V ± 5%, no load on any output, and ambient temperature range T_A = 0°C to 70°C. Parameters denoted with an asterisk (*) represent nominal characterization data and are not currently production tested to any specific limits. MIN and MAX characterization data are ±3σfrom typical. Negative currents indicate current flows out of the device.

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	MIN.	TYP.	MAX.	UNITS
Overall						
Supply Current, Dynamic, with Loaded Outputs	I_{DD}	f_{HOST} = 133MHz; all supplies = 3.465V, R_{IREF}= 475Ω, $I_{OH} = 6 \times I_{REF}$				mA
Supply Current, Static	I_{DDs}	PWR_DWN# low, all supplies = 3.465V, R_{IREF}= 475Ω, $I_{OH} = 6 \times I_{REF}$				µA
Digital Inputs (PWR_DWN#, ISEL_0, ISEL_1, SEL133/100#)						
High-Level Input Voltage	V_{IH}		2.0		V_{DD}+0.3	V
Low-Level Input Voltage	V_{IL}		V_{SS}-0.3		0.8	V
Input Leakage Current	I_{IL}		-5		+5	µA
Crystal Oscillator Feedback (XIN)						
Threshold Bias Voltage	V_{TH}			1.5		V
High-Level Input Current	I_{IH}	V_{IH} = 3.3V		32		µA
Low-Level Input Current	I_{IL}	V_{IL} = 0V		-32		µA
Crystal Loading Capacitance *	$C_{L(xtal)}$	As seen by an external crystal connected to XIN and XOUT	13.5	18	22.5	pF
Input Loading Capacitance *	$C_{L(XIN)}$	As seen by an external clock driver on XOUT; XIN unconnected		36		pF
Crystal Oscillator Drive (XOUT)						
High Level Output Source Current	I_{OH}	$V_{I\ (XIN)}$ = 3.3V, V_O = 0V		-8.0		mA
Low Level Output Sink Current	I_{OL}	$V_{I\ (XIN)}$ = 0V, V_O = 3.3V		8.7		mA
Current Reference (IREF)						
Bias Voltage	V_{OH}	no load		1.1		V
Short Circuit Output Source Current	I_{OH}	V_O = 0V				mA
MREF_P, MREF_N, 14REF, and 66REF Clock Outputs (Type 5 Clock Driver)						
High Level Output Source Current	$I_{OH\ min}$	VDD_M, VDD_R, VDD_66 = 3.135V, V_O = 1.0V	-33			mA
	$I_{OH\ max}$	VDD_M, VDD_R, VDD_66 = 3.465V, V_O = 3.135V			-33	
Low Level Output Sink Current	$I_{OL\ min}$	VDD_M, VDD_R, VDD_66 = 3.135V, V_O = 1.95V	30			mA
	$I_{OL\ max}$	VDD_M, VDD_R, VDD_66 = 3.465V, V_O = 0.4V			38	
Output Impedance	z_{OL}	Measured at 1.65V, output driving low	12		55	Ω
	z_{OH}	Measured at 1.65V, output driving high	12		55	
Tristate Output Current	I_{OZ}		-10		10	µA
Short Circuit Output Source Current	I_{OSH}	V_O = 0V; shorted for 30s, max.		-51		mA
Short Circuit Output Sink Current	I_{OSL}	V_O = 3.3V; shorted for 30s, max.		62		mA

Table 13: DC Electrical Specifications, continued

Unless otherwise stated, all power supplies = 3.3V ± 5%, no load on any output, and ambient temperature range T_A = 0°C to 70°C. Parameters denoted with an asterisk (*) represent nominal characterization data and are not currently production tested to any specific limits. MIN and MAX characterization data are ±3σfrom typical. Negative currents indicate current flows out of the device.

PARAMETER		SYMBOL	CONDITIONS/DESCRIPTION	MIN.	TYP.	MAX.	UNITS
HOST_P1:4, HOST_N1:4 Clock Outputs (Type X1 Clock Buffer)							
Crossover Voltage		V_X	R_S = 33.2Ω, R_P = 49.9Ω, R_{IREF} = 475Ω, I_{OH} = 6× I_{REF}	45		55	%V_{OH}
High-Level Output Source Current		I_{OH}	V_O = 0.65V, R_{IREF} = 475Ω, I_{OH} = 6 × I_{REF}	12.9			mA
			V_O = 0.74V, R_{IREF} = 475Ω, I_{OH} = 6 × I_{REF}			14.9	
Output Source Current Tolerance		ΔI_{OH}	V_{DD} = 3.30V, over settings in Table 7	-7		+7	%I_{OH}
			VDD_I=3.3V±5%, over settings in Table 7	-12		+12	
Output Impedance		z_{OH}	$\Delta V_O/\Delta I_O$, where V_{O1} = 1.0V, V_{O2} = V_{SS}, R_{IREF} = 475Ω, I_{OH} = 6× I_{REF}	3000			Ω
Tristate Output Current		I_{OZ}		-10		10	µA
SEL_A / APIC_0, SEL_B / APIC_1, and SS_EN# / APIC_3 Latched Inputs / Clock Outputs (1.8V Clock Buffer)							
High-Level Input Voltage	Input	V_{IH}	VDD_A = 3.3V, LVTTL Input (APICON=0)	2.0		V_{DD}+0.3	V
			VDD_A = 1.8V, Latched Input (APICON=1)	1.17		V_{DD}+0.3	
Low-Level Input Voltage		V_{IL}	VDD_A = 3.3V, LVTTL Input (APICON=0)	V_{SS}-0.3		0.8	V
			VDD_A = 1.8V, Latched Input (APICON=1)	V_{SS}-0.3		0.63	
Input Leakage Current		I_{IL}		-5		+5	µA
High Level Output Source Current	Output	I_{OH}	VDD_A = 1.8V, V_O = 1.4V			-25	mA
Low Level Output Sink Current		I_{OL}	VDD_A = 1.8V, V_O = 0.4V	24			mA
Output Impedance		z_{OL}	Measured at 0.7V, output driving low	11		37	Ω
		z_{OH}	Measured at 0.7V, output driving high	18		41	
Tristate Output Current		I_{OZ}					µA
Short Circuit Output Source Current		I_{OSH}	V_O = 0V; shorted for 30s, max.		-97		mA
Short Circuit Output Sink Current		I_{OSL}	V_O = 1.8V; shorted for 30s, max.		64		mA

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Table 14: AC Timing Specifications

Unless otherwise stated, all power supplies = 3.3V, no load on any output, and ambient temperature T_A = 25°C. Parameters denoted with an asterisk (*) represent nominal characterization data and are not currently production tested to any specific limits. MIN and MAX characterization data are ±3σ from typical. Spread spectrum modulation is disabled except for Rise/Fall time measurements.

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	MIN.	TYP.	MAX.	UNITS
Overall						
Spread Spectrum Modulation Frequency *	f_m	SS_EN# low			31.5	kHz
Spread Spectrum Modulation Index *	δ_m	SS_EN# low			-0.5	%
Tristate Enable Delay *	t_{DZL}, t_{DZH}	SEL_A:B=00, SEL133/100#=0	1.0		10	ns
Tristate Disable Delay *	t_{DLZ}, t_{DHZ}	SEL_A:B=11, SEL133/100#=0	1.0		10	ns
Clock Stabilization (on power-up) *	t_{STB}	via PWR_DWN#			3.0	ms
HOST_P1:4, HOST_N1:4 Clock Outputs						
Clock Skew *	$t_{sk(o)}$	HOST pair to HOST pair @ V_X, R_{IREF} = 475Ω, $I_{OH} = 6 \times I_{REF}$, R_S = 33.2Ω, R_P = 49.9Ω			100	ps
Duty Cycle *	d_t	Ratio of high pulse width to one clock period at V_X, R_{IREF} = 475Ω, $I_{OH} = 6 \times I_{REF}$, R_S=33.2Ω, R_P=49.9Ω	45		55	%
Jitter, Long Term ($\sigma_y(\tau)$) *	$t_{j(LT)}$	On rising edges 500µs apart at V_X relative to an ideal clock, R_{IREF} = 475Ω, $I_{OH} = 6 \times I_{REF}$, R_S = 33.2Ω, R_P = 49.9Ω				ps
Jitter, Period (peak-peak) *	$t_{j(\Delta P)}$	Rising edge to rising edge at V_X, R_{IREF} = 475Ω, $I_{OH} = 6 \times I_{REF}$, R_S = 33.2Ω, R_P = 49.9Ω			150	ps
Rise Time *	t_r	Rising edge to rising edge at V_X, R_{IREF} = 475Ω, $I_{OH} = 6 \times I_{REF}$, R_S = 33.2Ω, R_P = 49.9Ω	175		450	ps
Rise/Fall Time Matching*		Rising edge to rising edge at V_X, R_{IREF} = 475Ω, $I_{OH} = 6 \times I_{REF}$, R_S = 33.2Ω, R_P = 49.9Ω			20	%
MREF_P, MREF_N Clock Outputs						
Duty Cycle *	d_t	Ratio of high pulse width to one clock period, measured at 1.5V	45		55	%
Jitter, Long Term ($\sigma_y(\tau)$) *	$t_{j(LT)}$	On rising edges 500µs apart at 1.5V relative to an ideal clock, C_L=30pF				ps
Jitter, Period (peak-peak) *	$t_{j(\Delta P)}$	From rising edge to rising edge at 1.5V, C_L=30pF			250	ps
Rise Time *	$t_{r\ min}$	Measured @ 0.4V – 2.4V; C_L=10pF	0.4			ns
	$t_{r\ max}$	Measured @ 0.4V – 2.4V; C_L=30pF			1.6	
Fall Time *	$t_{f\ min}$	Measured @ 2.4V – 0.4V; C_L=10pF	0.4			ns
	$t_{f\ max}$	Measured @ 2.4V – 0.4V; C_L=30pF			1.6	

Table 15: AC Timing Specifications, continued

Unless otherwise stated, all power supplies = 3.3V, no load on any output, and ambient temperature T_A = 25°C. Parameters denoted with an asterisk (*) represent nominal characterization data and are not currently production tested to any specific limits. MIN and MAX characterization data are ±3σ from typical. Spread spectrum modulation is disabled except for Rise/Fall time measurements.

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	MIN.	TYP.	MAX.	UNITS
66REF Reference Clock Output						
Duty Cycle *	d_t	Ratio of high pulse width to one clock period, measured at 1.5V	45		55	%
Jitter, Long Term ($\sigma_y(\tau)$) *	$t_{j(LT)}$	On rising edges 500µs apart at 1.5V relative to an ideal clock, C_L=20pF				ps
Jitter, Period (peak-peak) *	$t_{j(\Delta P)}$	From rising edge to rising edge at 1.5V, C_L=20pF				ps
Rise Time *	$t_{r\ min}$	Measured @ 0.4V – 2.4V; C_L=10pF	0.5			ns
	$t_{r\ max}$	Measured @ 0.4V – 2.4V; C_L=20pF			2.0	
Fall Time *	$t_{f\ min}$	Measured @ 2.4V – 0.4V; C_L=10pF	0.5			ns
	$t_{f\ max}$	Measured @ 2.4V – 0.4V; C_L=20pF			2.0	
14REF Reference Clock Output						
Duty Cycle *	d_t	Ratio of high pulse width to one clock period, measured at 1.5V	45		55	%
Jitter, Long Term ($\sigma_y(\tau)$) *	$t_{j(LT)}$	On rising edges 500µs apart at 1.5V relative to an ideal clock, C_L=20pF				ps
Jitter, Period (peak-peak) *	$t_{j(\Delta P)}$	From rising edge to rising edge at 1.5V, C_L=20pF				ps
Rise Time *	$t_{r\ min}$	Measured @ 0.4V – 2.4V; C_L=10pF	0.5			ns
	$t_{r\ max}$	Measured @ 0.4V – 2.4V; C_L=20pF			2.0	
Fall Time *	$t_{f\ min}$	Measured @ 2.4V – 0.4V; C_L=10pF	0.5			ns
	$t_{f\ max}$	Measured @ 2.4V – 0.4V; C_L=20pF			2.0	

Figure 5: DC Measurement Points

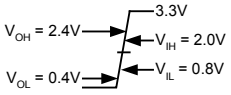

Figure 6: Timing Diagram

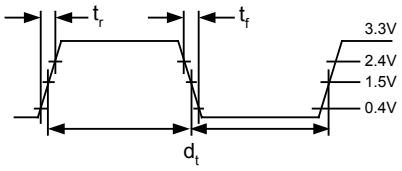

Figure 7: HOST Clock Measurement Point

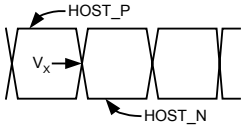

Figure 8: HOST Clock Test Point

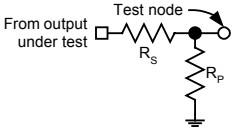

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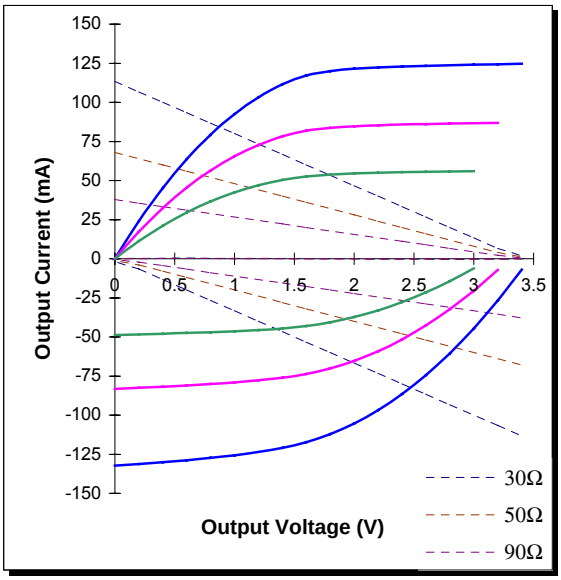
Table 16: MCLK_P, MCLK_N, 14REF, 66REF Clock Outputs

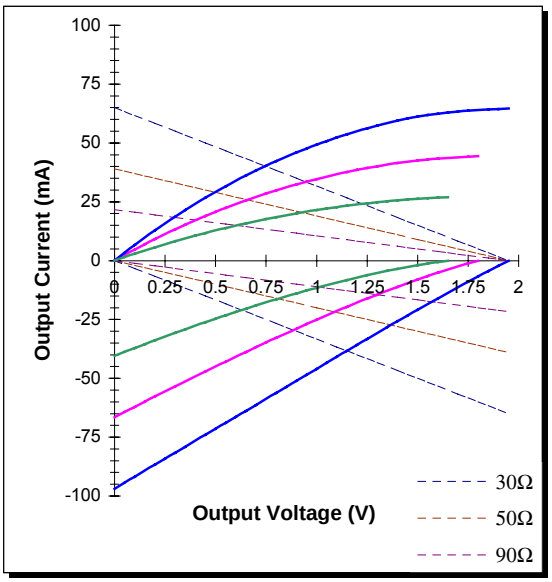
Voltage (V)	High Drive Current (mA)			Voltage (V)	Low Drive Current (mA)		
	MIN.	TYP.	MAX.		MIN.	TYP.	MAX.
0	0	0	0	0	-49	-83	-132
0.2	11	17	24	0.2	-48	-83	-131
0.4	21	32	45	0.4	-48	-82	-130
0.6	30	45	64	0.6	-47	-81	-129
0.8	37	56	79	0.8	-47	-80	-127
1.0	43	65	92	1.0	-46	-79	-126
1.2	47	73	103	1.2	-46	-78	-124
1.4	50	78	112	1.4	-45	-76	-121
1.6	53	82	117	1.6	-43	-74	-117
1.8	54	84	120	1.8	-41	-70	-112
2.0	55	85	121	2.0	-37	-65	-105
2.2	55	85	122	2.2	-33	-59	-97
2.4	55	86	123	2.4	-28	-52	-87
2.6	56	86	123	2.6	-22	-43	-74
2.8	56	86	124	2.8	-14	-32	-60
3.0	56	87	124	3.0	-6	-20	-45
3.2		87	124	3.2		-7	-27
3.4			125	3.4			-7



Data in this table represents nominal characterization data only

Table 17: APIC_0:2 Clock Outputs

Voltage (V)	High Drive Current (mA)			Voltage (V)	Low Drive Current (mA)		
	MIN.	TYP.	MAX.		MIN.	TYP.	MAX.
0	0	0	0	0	-40	-67	-97
0.1	3	5	7	0.1	-37	-62	-92
0.2	6	9	13	0.2	-34	-58	-87
0.3	8	13	19	0.3	-31	-53	-82
0.4	11	17	24	0.4	-28	-49	-76
0.5	13	21	29	0.5	-25	-45	-71
0.6	15	24	34	0.6	-22	-41	-66
0.7	17	27	38	0.7	-19	-37	-61
0.8	19	30	42	0.8	-16	-33	-56
0.9	20	32	46	0.9	-14	-29	-51
1.0	21	35	49	1.0	-12	-25	-46
1.2	24	39	55	1.2	-7	-18	-36
1.4	26	41	59	1.4	-3	-11	-26
1.5	26	43	61	1.5	-2	-8	-21
1.6	27	43	62	1.6	-1	-5	-16
1.7		44	63	1.7		-2	-11
1.8		44	64	1.8		0	-7
1.9			64	1.9			-2



Data in this table represents nominal characterization data only

7.0 Package Information

Table 18: 48-pin SSOP (0.300") Package Dimensions

	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.095	0.110	2.41	2.79
A_1	0.008	0.016	0.20	0.41
b	0.008	0.0135	0.20	0.34
c	0.005	0.010	0.13	0.25
D	0.620	0.630	15.75	16.00
E	0.395	0.420	10.03	10.67
E_1	0.291	0.299	7.39	7.59
e	0.025 BSC		0.64 BSC	
h	0.015	0.025	0.38	0.64
L	0.020	0.040	0.51	1.01
θ	0°	8°	0°	8°

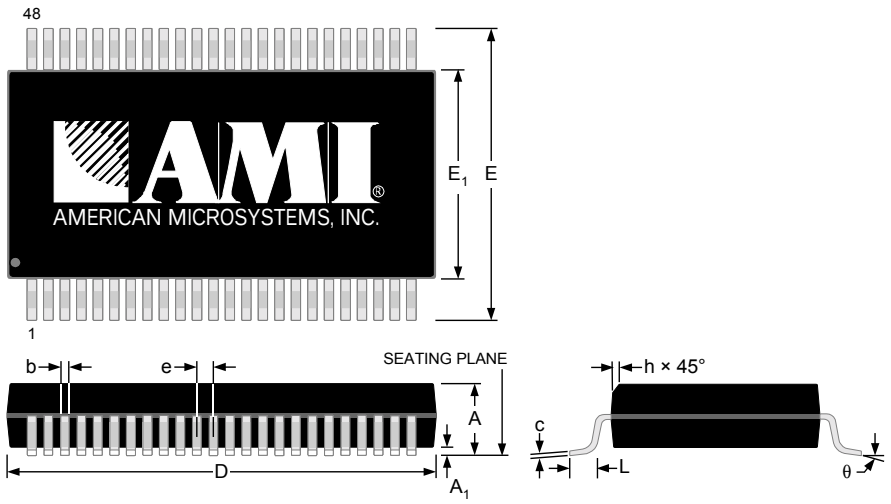


Table 19: 48-pin SSOP (0.300") Package Characteristics

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	TYP.	UNITS
Thermal Impedance, Junction to Free-Air	Θ_{JA}	Air flow = 0 m/s	93	°C/W
Lead Inductance, Self	L_{11}	Longest lead	5.5	nH
Lead Inductance, Mutual	L_{12}	Longest lead to any 1st adjacent lead	3.0	nH
	L_{13}	Longest lead to any 2nd adjacent lead	2.1	
Lead Capacitance, Bulk	C_{11}	Longest lead to V_{SS}	0.94	pF
Lead Capacitance, Mutual	C_{12}	Longest lead to any 1st adjacent lead	0.46	pF
	C_{13}	Longest lead to any 2nd adjacent lead	0.05	

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Table 20: 48-pin TSSOP (6.1mm) Package Dimensions

	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	-	0.047	-	1.20
A_1	0.002	0.006	0.05	0.15
b	0.0067	0.011	0.17	0.27
c	0.0035	0.008	0.09	0.20
D	0.488	0.496	12.40	12.60
E	0.318 BSC		8.10 BSC	
E_1	0.236	0.244	6.00	6.20
e	0.019 BSC		0.50 BSC	
L	0.018	0.030	0.45	0.75
S	0.008	-	0.20	-
θ_1	0°	8°	0°	8°
θ_2	12° REF		12° REF	
θ_3	12° REF		12° REF	

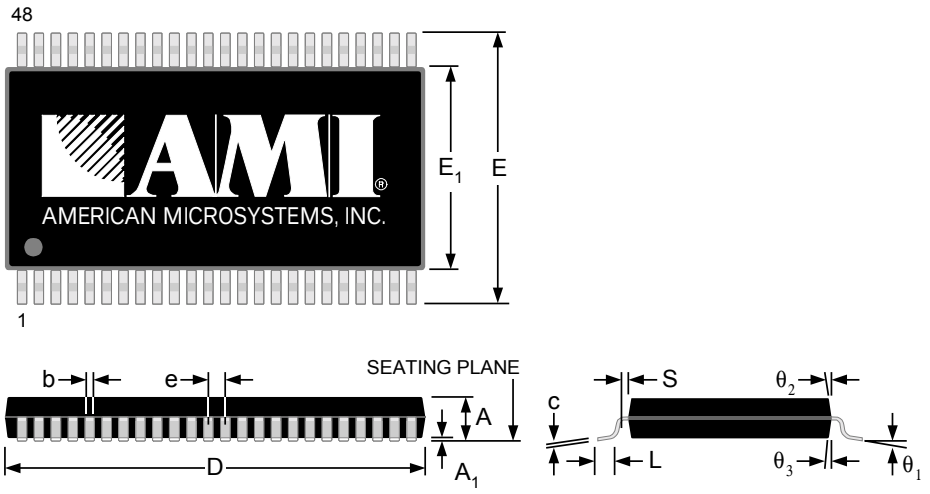

Table 21: 48-pin TSSOP (6.1mm) Package Characteristics

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	TYP.	UNITS
Thermal Impedance, Junction to Free-Air	Θ_{JA}	Air flow = 0 m/s	89	°C/W
Lead Inductance, Self	L_{11}	Longest lead	3.50	nH
Lead Inductance, Mutual	L_{12}	Longest lead to any 1st adjacent lead	1.82	nH
	L_{13}	Longest lead to any 2nd adjacent lead	1.17	
Lead Capacitance, Bulk	C_{11}	Longest lead to V_{SS}	0.63	pF
Lead Capacitance, Mutual	C_{12}	Longest lead to any 1st adjacent lead	0.30	pF
	C_{13}	Longest lead to any 2nd adjacent lead	0.03	

8.0 Ordering Information

DEVICE NUMBER	ORDERING CODE	PACKAGE TYPE	OPERATING TEMPERATURE RANGE	SHIPPING CONFIGURATION
FS6158-01	11915-801	48-pin (0.300") SSOP	0° C to 70° C (Commercial)	Tape and Reel
	11915-811	48-pin (0.300") SSOP	0° C to 70° C (Commercial)	Tubes
	11915-201	48-pin (6.1mm) TSSOP	0° C to 70° C (Commercial)	Tape and Reel
	11915-211	48-pin (6.1mm) TSSOP	0° C to 70° C (Commercial)	Tubes

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