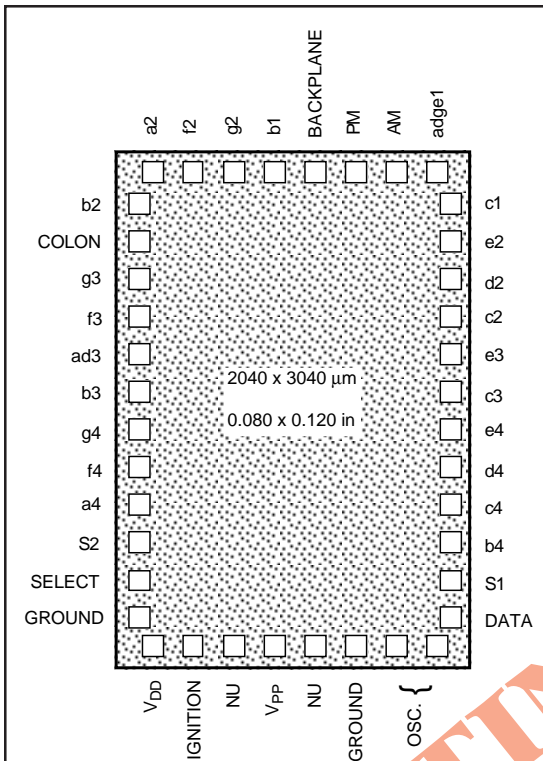


5616

2-FUNCTION, 4-DIGIT LCD AUTOMOTIVE CLOCK—PROGRAMMABLE



Dwg. No. PC-001

ABSOLUTE MAXIMUM RATINGS

| | |
|---|--------------------------------------|
| Supply Current, I_{DD} | 2.0 mA |
| Input Voltage Range, V_{IN} (except V_{PP}) | -0.3 V to V_{DD} |
| (Programming Power Voltage, V_{PP}) | 18.5 V |
| Input Current (except V_{PP}), I_{IN} | ± 10 mA |
| Power Dissipation, P_D | 300 mW |
| Operating Temperature Range, T_A | -40°C to +85°C |
| Storage Temperature Range, T_S | -65°C to +150°C |

Caution: These CMOS devices have static protection, but are susceptible to damage if exposed to extremely high static electrical charges.

The SCL5616HW is a 2-function digital automotive clock circuit. Fabricated on a single monolithic chip using silicon-gate CMOS PROM technology, it offers low cost, low power, and high reliability. It also includes digital frequency correction, stored in the internal nonvolatile memory, for easy adjustment of the oscillator nominal frequency.

The SCL5616HW is supplied in wafer form and is rated for continuous operation over the automotive temperature range of -40°C to +85°C.

FEATURES

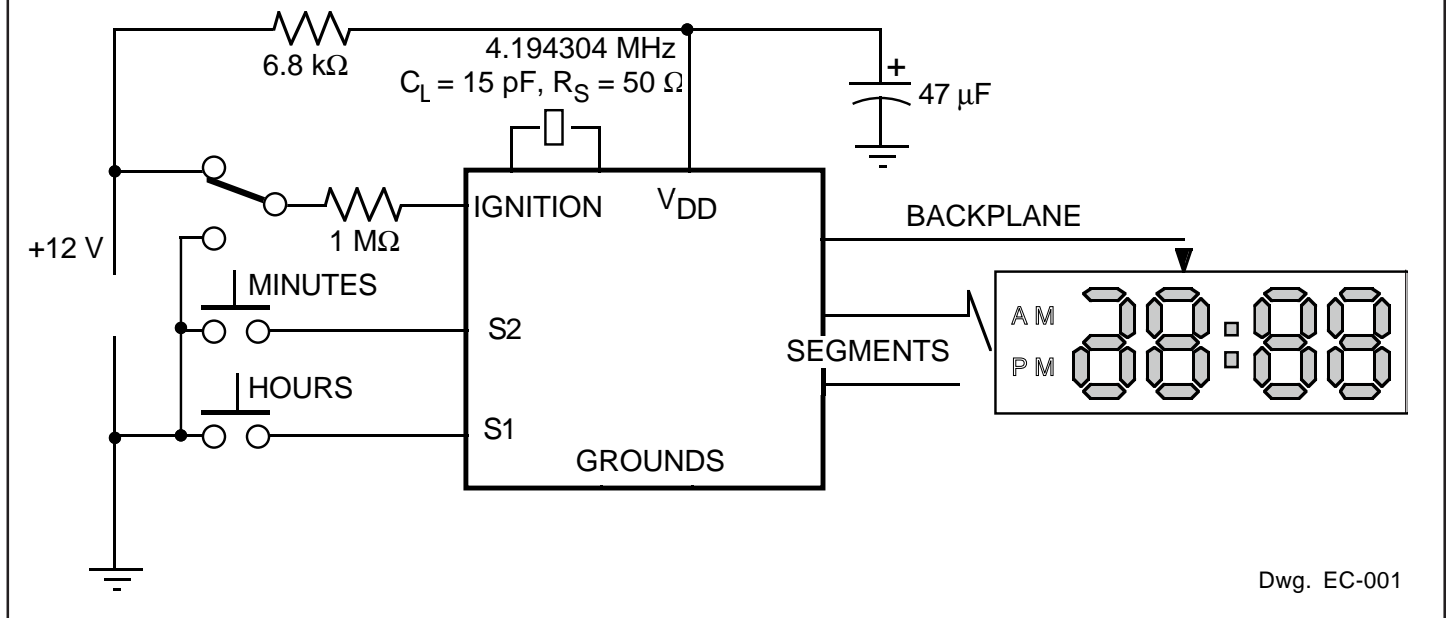
- Digital Tuning of Crystal Frequency
- PROM for Storing Frequency Correction Information
- 12 or 24 Hour Timekeeping Option
- Flashing Colon
- Two Switches Control All Setting Functions
- High Noise Immunity
- Internal Power-Up Reset Circuitry
- Internal Voltage Regulation

Always order by complete part number: SCL5616HW.

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2-FUNCTION, 4-DIGIT LCD AUTOMOTIVE CLOCK

TYPICAL APPLICATION



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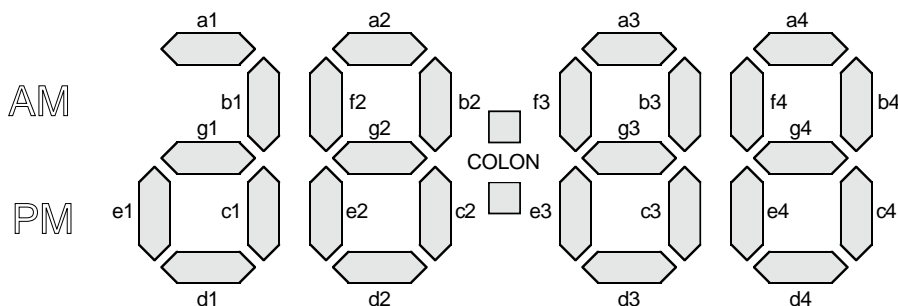
2-FUNCTION, 4-DIGIT LCD AUTOMOTIVE CLOCK

ELECTRICAL CHARACTERISTICS at $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, in Typical Application (unless otherwise noted).

| Characteristic | Symbol | Test Conditions | Limits | | | |
|--------------------------|------------------|---|--------|-----------|-----------|------------------|
| | | | Min. | Typ. | Max. | Units |
| Operating Voltage Range | V_{DD} | $T_A = +25^{\circ}\text{C}$ | 4.5 | — | — | V |
| Zener Voltage | V_{DD} | $I_{DD} = 1.0 \text{ mA}$ | 5.5 | — | 6.8 | V |
| Segment Output Current | I_{OUT} | $V_{DD} = 5.0 \text{ V}, V_{OUT} = 4.8 \text{ V}$ | -20 | — | — | μA |
| | | $V_{DD} = 5.0 \text{ V}, V_{OUT} = 0.2 \text{ V}$ | 120 | — | — | μA |
| Backplane Output Current | I_{OUT} | $V_{DD} = 5.0 \text{ V}, V_{OUT} = 4.8 \text{ V}$ | -80 | — | — | μA |
| | | $V_{DD} = 5.0 \text{ V}, V_{OUT} = 0.2 \text{ V}$ | 240 | — | — | μA |
| LCD Drive Signal | V_{DISP} | $V_{DD} \geq 5.0 \text{ V}$ | 4.0 | — | — | V |
| Input Current | I_{IN} | S1, S2, DATA, or SELECT | -55 | — | -700 | μA |
| Oscillator Frequency | f_{OSC} | | — | 4.194 304 | — | MHz |
| Oscillator Starting Time | t_{OSC} | $V_{DD} = \text{Zener voltage}$ | — | — | 200 | ms |
| Oscillator Stability | Δf_{OSC} | $\Delta V_{DD} = \pm 100 \text{ mV}$ | — | — | ± 1.0 | ppM |
| Backplane Frequency | f_{BP} | | — | 64 | — | Hz |
| Switch Debounce Time | t_{DB} | | 0 | — | 62.5 | ms |
| Osc. Feedback Resistance | R_{OSC} | | — | 16 | — | $\text{M}\Omega$ |
| Osc. Input Capacitance | C_{OSCI} | | — | 15 | — | pF |
| Osc. Output Capacitance | C_{OSCO} | | — | 30 | — | pF |
| Supply Current | I_{DD} | $V_{DD} = 5.0 \text{ V}$ | — | — | 1.0 | mA |

NOTE: Negative current is defined as coming out of (sourcing) the specified device terminal.

DISPLAY FORMAT



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2-FUNCTION, 4-DIGIT LCD AUTOMOTIVE CLOCK

FUNCTIONAL DESCRIPTION

DATA Logic Levels are V_{DD} and Ground

Power-Up Reset . When power up occurs, the hours and minutes counters are reset, and the clock starts running:

Operation

12-Hour mode and counting starts from 1:00 AM

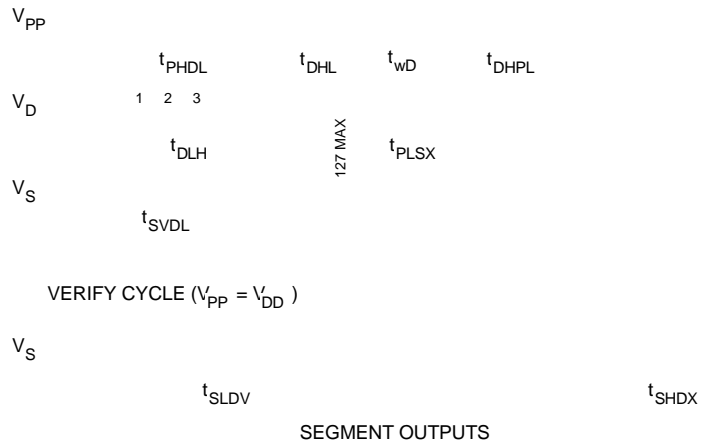
Programming Modes . Data is loaded by pulling DATA low (1 μ s pulse duration) n times to set the desired bits for frequency correction into the data input register. This information is latched in the RAM, thus allowing the testing of the oscillator frequency adjustment without storing the selected pattern in the PROM cells. The data latched in the RAM is stored in the PROM cells when DATA is held low for a minimum of 10 ms.

The data stored in the data input register is cleared on any SELECT transition (low to high or high to low). It is also cleared when the program power voltage (V_{PP}) is reduced from 18 V to V_{DD} . Clearing the data input register does not affect the data latched in the RAM.

| Program V_{PP} | DATA V_D | SELECT V_S | Operation |
|---------------------|---------------|-----------------|------------------------------------|
| 18 V | Pulse | Ground | DATA load for frequency correction |
| 18 V | Ground | V_{DD} | DATA store |
| V_{DD} | V_{DD} | Ground | Verify stored data |

FREQUENCY CORRECTION

FREQUENCY CORRECTION



Dwg. No. WC-001-1



Frequency Correction. The on-chip oscillator circuit increases the crystal frequency approximately 40 ppm. This ensures that the typical crystal will operate within the tuning range. With V_S at ground, data pulses are then used to trim the internal clock frequency by 2 to 254 ppm to the required value. The quantity of data pulses needed (1 to 127) is

$$n = \frac{f_{BP} - 64}{128 \times 10^{-6}}$$

where f_{BP} is the measured frequency at BACKPLANE. Prior to trimming, it must be between 64.000 128 Hz and 64.016 256 Hz.

Operating Modes. The operating modes of the clock are controlled by the voltages applied to V_{PP} , SELECT, IGNITION, and switches S1 and S2.

| Program | SELECT | | | | |
|----------|----------|--------|--------|----------|---------------|
| V_{PP} | V_S | S1 | S2 | IGNITION | Mode |
| V_{DD} | V_{DD} | Open | Open | X | Clock running |
| V_{DD} | V_{DD} | Ground | Ground | 12 V | Diagnostic |
| 18 V | Ground | Open | Open | X | Programming |

X = Irrelevant, ground or 12 V

Clock Running Mode. During the clock running mode, setting functions are achieved by either momentary or continuous operation of switches S1 and S2, which are enabled by IGNITION. Hours or minutes are incremented on S1 or S2 (respectively) depression and continue at a 1 Hz rate while the switch is depressed.

| S1 | S2 | IGNITION | Operation |
|--------|--------|----------|---|
| Open | Open | X | Clock running |
| X | X | Ground | Setting disabled |
| Ground | Open | 12 V | Set hours |
| Open | Ground | 12 V | Set Minutes |
| Ground | Ground | 12 V | Change counting sequence (12 to 24 hour or 24 to 12 hour) |

X = Irrelevant, ground or 12 V for IGNITION, ground or open for S1 and S2

Diagnostic Mode. To enter the diagnostic mode, S1 and S2 are operated with IGNITION connected to 12 V. All segments are displayed for as long as S1 and S2 are depressed. On opening S1 and S2, the clock will leave the diagnostic mode and go through a power-up sequence. In the SCL5616HW, the counting sequence will change (from 12 hour to 24 hour or from 24 hour to 12 hour). To inhibit the power-up reset, hold the DATA input low (ground). The counting mode will change without resetting the hours or minutes counters.

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2-FUNCTION, 4-DIGIT LCD AUTOMOTIVE CLOCK

Stored Data Verification. In the verify mode, the complement value of the information stored in the PROM cells is brought out directly to the segment output terminals for easy verification of the stored data. If a bit is programmed (high), the appropriate segment output is turned ON (low). The segments represent the binary equivalent of the number of frequency correction data pulses entered.

| | | | | | | | |
|----------------------------|----|----|----|----|----|----|----|
| Frequency Selection Pulses | 64 | 32 | 16 | 8 | 4 | 2 | 1 |
| Segment | b4 | c4 | d4 | e4 | c3 | e3 | c2 |

**RECOMMENDED FLASH
PROGRAMMING CHARACTERISTICS**
at $T_A = +25^\circ\text{C}$, Logic Levels are V_{DD} and Ground
(except PROGRAM High)

| Characteristic | Symbol | Min. | Max. | Units |
|-----------------------------------|------------|------|------|---------------|
| PROGRAM High (18 V) to DATA Low | t_{PHDL} | 1.0 | — | μs |
| SELECT Valid to DATA Low | t_{SVDL} | 25 | — | μs |
| DATA Low to DATA High | t_{DLH} | 1.0 | 1.5 | μs |
| DATA High to DATA Low | t_{DHL} | 1.0 | — | μs |
| DATA Store Pulse Duration | t_{WD} | 10 | — | ms |
| DATA High to PROGRAM Low | t_{DHPL} | 1.0 | — | μs |
| PROGRAM Low to SELECT Change | t_{PLSX} | 1.0 | — | μs |
| SELECT Low (Verify) to DATA Valid | t_{SLDV} | — | 1.0 | μs |
| DATA Hold from End of Verify | t_{SHDX} | — | 10 | ns |

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