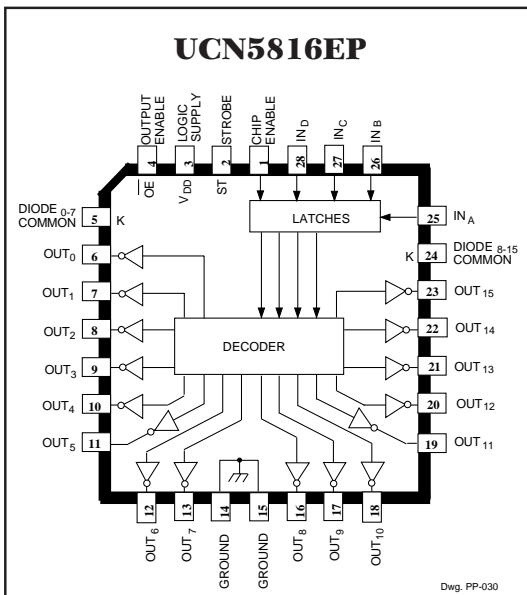


5816

4-TO-16 LINE LATCHED DECODER/DRIVERS



The UCN5816A and UCN5816EP 4-to-16 line latched decoder/drivers combine low-power CMOS inputs and logic with 16 high-current, high-voltage bipolar outputs. The CMOS inputs cause minimal loading and are compatible with standard CMOS, PMOS, and NMOS logic. TTL or DTL circuits may require the use of appropriate pull-up resistors to ensure an input logic high. The logic operates over a supply range of 5 V to 12 V. A CHIP ENABLE function can be used with two devices for 5-to-32 line decoding applications.

The 16 bipolar power outputs are open-collector 60 V Darlington drivers capable of sinking 350 mA continuously. Internal transient-suppression diodes provide protection for use with inductive loads. For ink-jet printer applications, the A5817SEP addressable 28-line decoder/driver is recommended.

The UCN5816A is supplied in a 28-pin dual in-line plastic package with 0.600" (15.24 mm) row spacing. The UCN5816EP is furnished in a 28-lead plastic chip carrier (quad pack) for minimum-area surface-mount applications. Both devices will drive 350 mA loads continuously over the full operating temperature range.

FEATURES

- Addressable Data Entry
- 60 V Minimum Output Breakdown
- CMOS, PMOS, NMOS, TTL Compatible Inputs
- Low-Power CMOS Logic and Latches
- Output Transient Protection
- Output Enable and Strobe Functions

ABSOLUTE MAXIMUM RATINGS at $T_A = 25^\circ\text{C}$

Output Voltage, V_{CE}	60 V
Logic Supply Voltage, V_{DD}	15 V
Input Voltage Range, V_{IN}	-0.3 V to $V_{DD} + 0.3$ V
Output Current, I_C	500 mA
Package Power Dissipation, P_D	See Graph
Operating Temperature Range, T_A	-20°C to $+85^\circ\text{C}$
Storage Temperature Range, T_S	-55°C to $+150^\circ\text{C}$

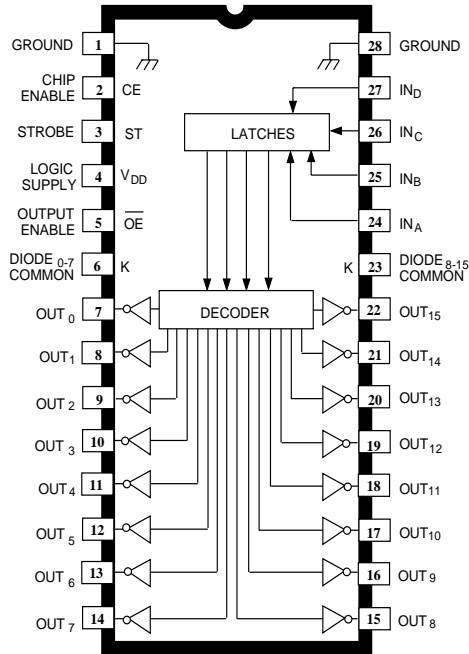
Caution: CMOS devices have input static protection but are susceptible to damage when exposed to extremely high static electrical charges.

Always order by complete part number:

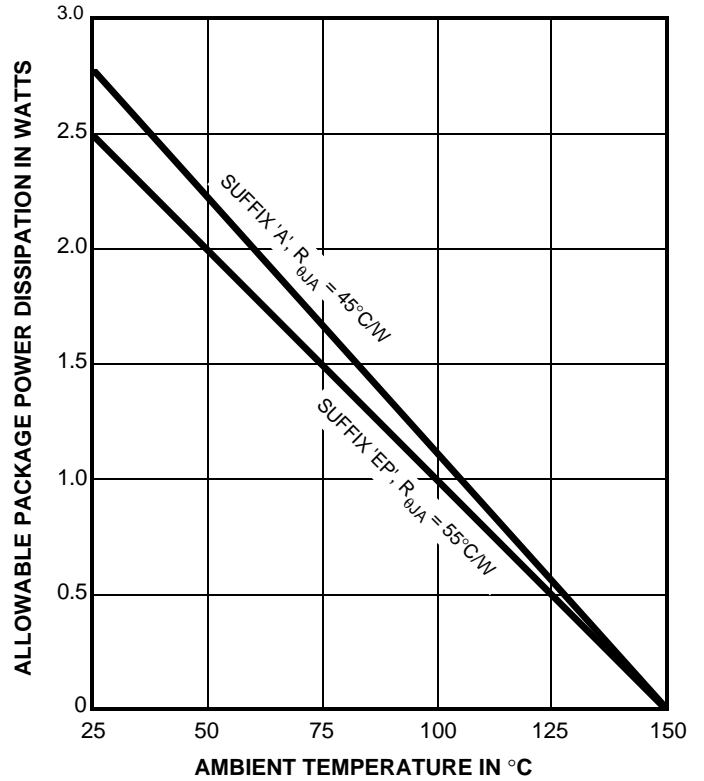
Part Number	Package
UCN5816A	28-Pin DIP
UCN5816EP	28-Lead PLCC

5816 4-TO-16 LINE LATCHED DECODER/DRIVERS

UCN5816A

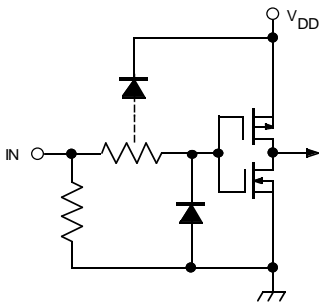


Dwg. PP-031

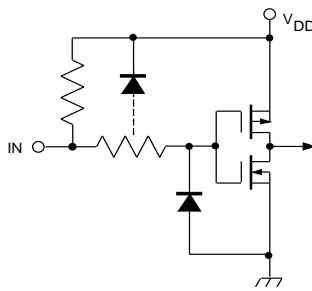


Dwg. GP-028-1A

TYPICAL INPUT CIRCUITS

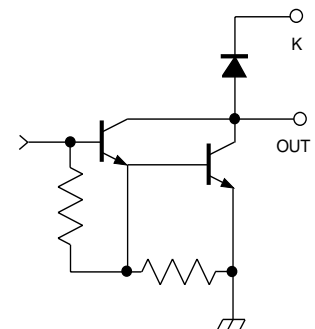


Dwg. EP-010-4A



Dwg. EP-010-3

TYPICAL OUTPUT DRIVER



Dwg. EP-021-4

5816

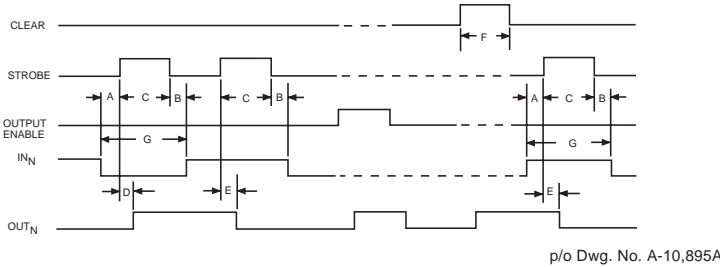
4-TO-16 LINE LATCHED DECODER/DRIVERS

ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$, $V_{DD} = 5\text{ V}$ (unless otherwise specified).

Characteristic	Symbol	Test Conditions	Limits			Units
			Min.	Typ.	Max.	
Output Leakage Current	I_{CEX}	$V_{CE} = 60\text{ V}$, $T_A = +25^\circ\text{C}$	—	—	50	μA
Output Saturation Voltage	$V_{CE(SAT)}$	$I_C = 100\text{ mA}$	—	0.9	1.1	V
		$I_C = 200\text{ mA}$	—	1.1	1.3	V
		$I_C = 350\text{ mA}$, $V_{DD} = 7.0\text{ V}$	—	1.3	1.6	V
Input Voltage	$V_{IN(0)}$		-0.3	—	0.8	V
	$V_{IN(1)}$	$V_{DD} = 12\text{ V}$	10.5	—	—	V
$V_{DD} = 5.0\text{ V}$		3.5	—	5.3	V	
Input Resistance	R_{IN}	$V_{DD} = 12\text{ V}$	50	200	—	$\text{k}\Omega$
		$V_{DD} = 5.0\text{ V}$	100	600	—	$\text{k}\Omega$
Supply Current	$I_{DD(ON)}$	$V_{DD} = 12\text{ V}$, Outputs Open	—	2.0	3.0	mA
		$V_{DD} = 5.0\text{ V}$, Outputs Open	—	1.0	1.5	mA
	$I_{DD(OFF)}$	All Drivers OFF, All Inputs = 0 V, $OE = V_{DD} = 5.0\text{ V}$	—	—	100	μA
		All Drivers OFF, All Inputs = 0 V, $OE = V_{DD} = 12\text{ V}$	—	—	200	μA
Clamp Diode Leakage Current	I_R	$V_R = 60\text{ V}$, $T_A = +25^\circ\text{C}$	—	—	50	μA
		$V_R = 60\text{ V}$, $T_A = +70^\circ\text{C}$	—	—	100	μA
Clamp Diode Forward Voltage	V_F	$I_F = 350\text{ mA}$	—	1.5	2.0	V

5816

4-TO-16 LINE LATCHED DECODER/DRIVERS



p/o Dwg. No. A-10,895A

TIMING CONDITIONS (Logic Levels are V_{DD} and Ground)

- A. Minimum Data Active Time Before Strobe Enabled (Data Set-Up Time) **50 ns**
- B. Minimum Data Active Time After Strobe Disabled (Data Hold Time) **50 ns**
- C. Minimum Strobe Pulse Duration **125 ns**
- D. Typical Time Between Strobe Activation and Output On to Off Transition **500 ns**
- E. Typical Time Between Strobe Activation and Output Off to On Transition **500 ns**
- G. Minimum Data Pulse Duration **225 ns**

TRUTH TABLE

STROBE	CHIP ENABLE	IN _D (MSB)	IN _C	IN _B	IN _A (LSB)	OUTPUT ENABLE	OUTPUTS (OFF unless otherwise specified)
1	1	0	0	0	0	0	OUT ₀ ON
1	1	0	0	0	1	0	OUT ₁ ON
1	1	0	0	1	0	0	OUT ₂ ON
1	1	0	0	1	1	0	OUT ₃ ON
1	1	0	1	0	0	0	OUT ₄ ON
1	1	0	1	0	1	0	OUT ₅ ON
1	1	0	1	1	0	0	OUT ₆ ON
1	1	0	1	1	1	0	OUT ₇ ON
1	1	1	0	0	0	0	OUT ₈ ON
1	1	1	0	0	1	0	OUT ₉ ON
1	1	1	0	1	0	0	OUT ₁₀ ON
1	1	1	0	1	1	0	OUT ₁₁ ON
1	1	1	1	0	0	0	OUT ₁₂ ON
1	1	1	1	0	1	0	OUT ₁₃ ON
1	1	1	1	1	0	0	OUT ₁₄ ON
1	1	1	1	1	1	0	OUT ₁₅ ON
0	1	X	X	X	X	0	Q ₀
X	0	X	X	X	X	X	All OFF
X	X	X	X	X	X	1	All OFF

Q₀ = The output condition prior to the high-to-low transition of the STROBE input.
X = Irrelevant

Information present at the inputs is transferred to the latches when the STROBE is high. The latches will continue to accept new data as long as the STROBE is held high. With the STROBE in the low state, no information can be loaded into the latches. Depending on the four address inputs, the 4-to-16 line decoder enables one of the 16 output sink drivers. When the OUTPUT ENABLE is high, all of the outputs are disabled (OFF) without affecting the information stored in the latches. When the OUTPUT ENABLE is low, the outputs are controlled by the information in the latches. When the CHIP ENABLE is low, all of the outputs are disabled (OFF). With two decoder/drivers and an inverter, the CHIP ENABLE function can be used for 5-to-32 line decoding applications.

