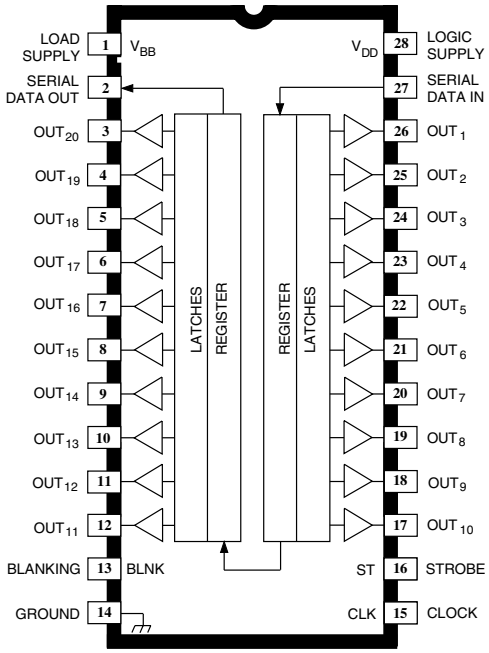
6812

Data Sheet
26182.126A

DABiC-IV, 20-BIT SERIAL-INPUT, LATCHED SOURCE DRIVER

A6812xA



Dwg. PP-029-7

ABSOLUTE MAXIMUM RATINGS
at T_A = 25°C

Logic Supply Voltage, V_{DD} ..... **7.0 V**
Driver Supply Voltage, V_{BB} ..... **60 V**
Continuous Output Current Range,
I_{OUT} ..... **-40 mA to +15 mA**
Input Voltage Range,
V_{IN} ..... **-0.3 V to V_{DD} + 0.3 V**
Package Power Dissipation,
P_D ..... **See Graph**
Operating Temperature Range, T_A
(Suffix 'E–') ..... **-40°C to +85°C**
(Suffix 'S–') ..... **-20°C to +85°C**
Storage Temperature Range,
T_S ..... **-55°C to +125°C**

Caution: These CMOS devices have input static protection (Class 2) but are still susceptible to damage if exposed to extremely high static electrical charges.

The A6812– devices combine a 20-bit CMOS shift register, accompanying data latches and control circuitry with bipolar sourcing outputs and pnp active pull downs. Designed primarily to drive vacuum-fluorescent displays, the 60 V and -40 mA output ratings also allow these devices to be used in many other peripheral power driver applications. The A6812– features an increased data input rate (compared with the older UCN/UCQ5812-F) and a controlled output slew rate.

The CMOS shift register and latches allow direct interfacing with microprocessor-based systems. With a 3.3 V or 5 V logic supply, they will operate to at least 10 MHz.

A CMOS serial data output permits cascade connections in applications requiring additional drive lines. Similar devices are available as the A6809– and A6810– (10 bits), A6811– (12 bits), and A6818– (32 bits).

The A6812– output source drivers are npn Darlingtons, capable of sourcing up to 40 mA. The controlled output slew rate reduces electromagnetic noise, which is an important consideration in systems that include telecommunications and/or microprocessors and to meet government emissions regulations. For inter-digit blanking, all output drivers can be disabled and all sink drivers turned on with a BLANKING input high. The pnp active pull-downs will sink at least 2.5 mA.

Two temperature ranges are available for optimum performance in commercial (suffix S-) or industrial (suffix E-) applications. Package styles are provided for through-hole DIP (suffix -A), surface-mount SOIC (suffix -LW), or minimum-area surface-mount PLCC (suffix -EP). Copper lead frames, low logic-power dissipation, and low output-saturation voltages allow these drivers to source 25 mA from all outputs continuously to more than +43°C (suffix -LW), +61°C (suffix -EP), or +77°C (suffix -A).

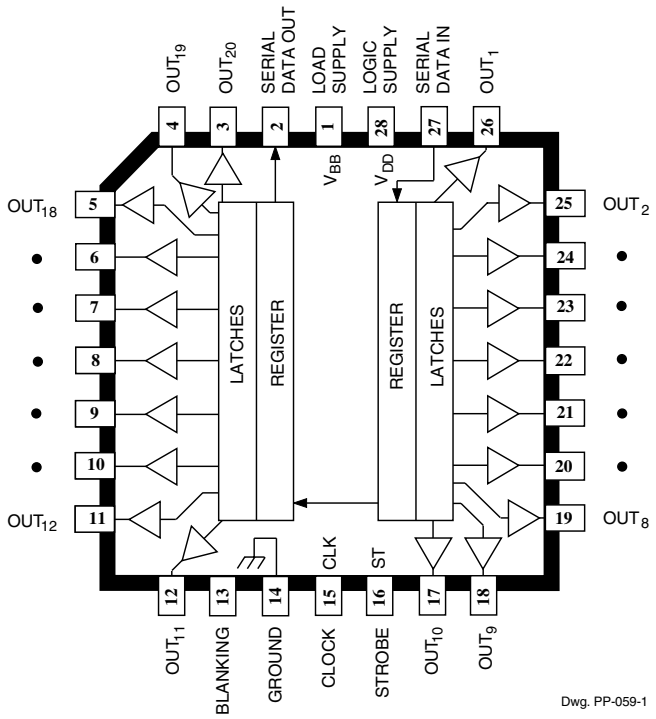
FEATURES

- Controlled Output Slew Rate
- High-Speed Data Storage
- 60 V Minimum Output Breakdown
- High Data Input Rate
- PNP Active Pull-Downs
- Low Output-Saturation Voltages
- Low-Power CMOS Logic and Latches
- Improved Replacements for TL5812–, UCN5812–, and UCQ5812–

Complete part number includes a suffix to identify operating temperature range (E- or S-) and package type (-A, -EP, or -LW). Always order by complete part number, e.g., **A6812SLW** .

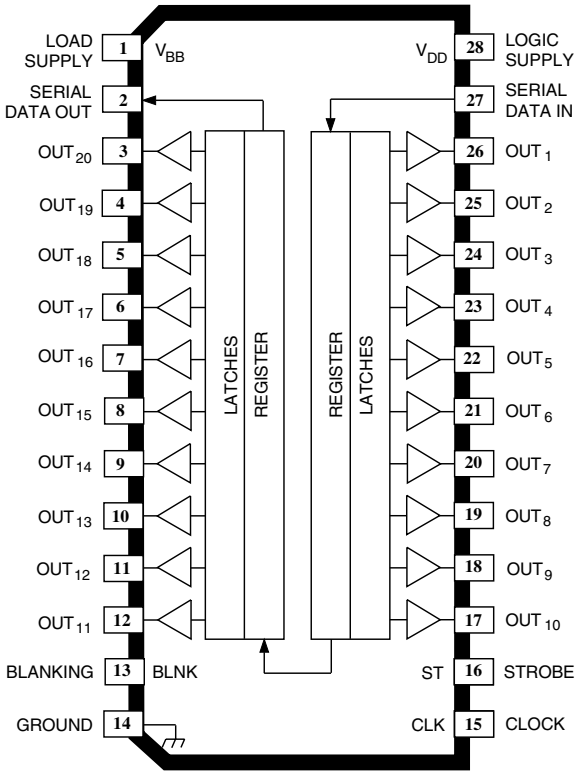
6812
20-BIT SERIAL-INPUT, LATCHED SOURCE DRIVER

A6812xEP



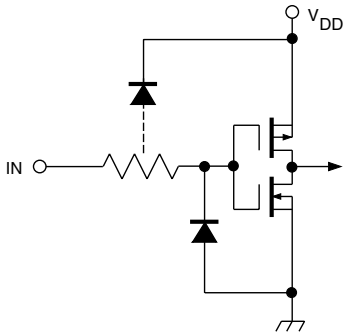
Dwg. PP-059-1

A6812xLW



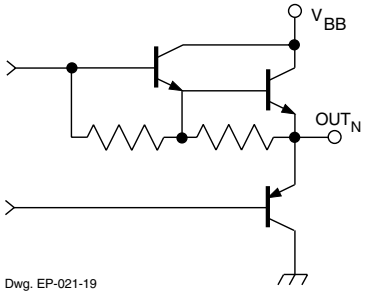
Dwg. PP-029-8

TYPICAL INPUT CIRCUIT

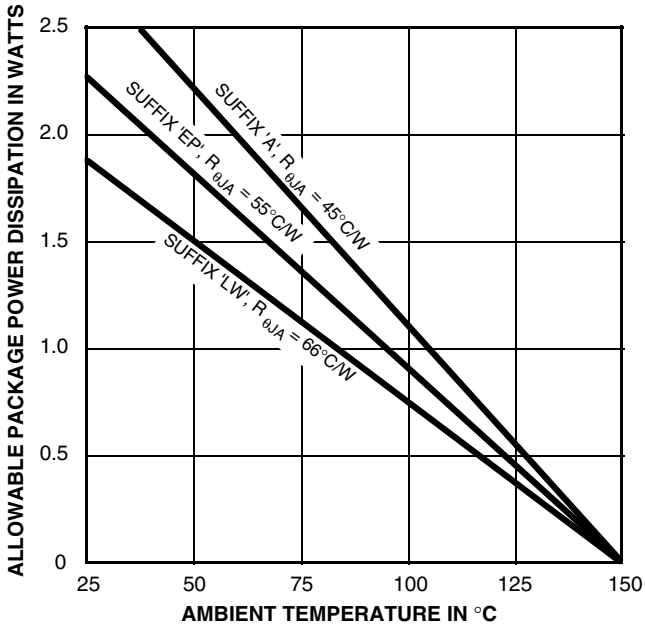


Dwg. EP-010-5

TYPICAL OUTPUT DRIVER



Dwg. EP-021-19



Dwg. GP-024-2

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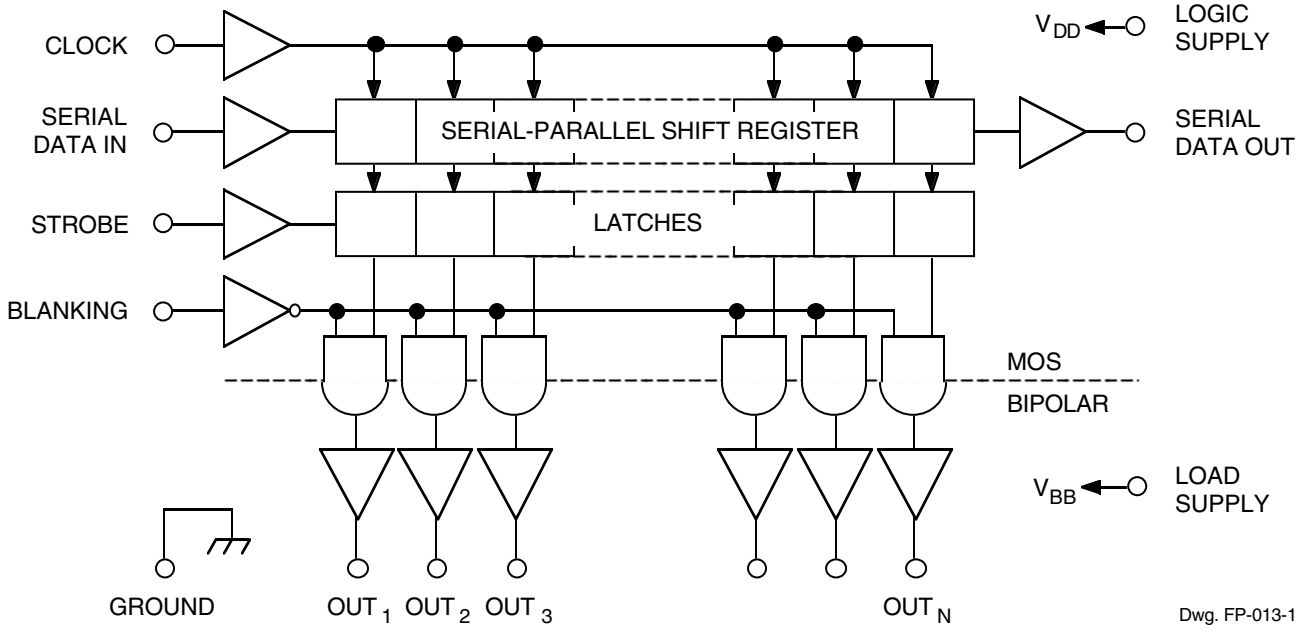
FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

Serial Data Input	Clock Input	Shift Register Contents I_1 I_2 I_3 ... I_{N-1} I_N	Serial Data Output	Strobe Input	Latch Contents I_1 I_2 I_3 ... I_{N-1} I_N	Blanking	Output Contents I_1 I_2 I_3 ... I_{N-1} I_N
H	↑	H R_1 R_2 ... R_{N-2} R_{N-1}	R_{N-1}				
L	↑	L R_1 R_2 ... R_{N-2} R_{N-1}	R_{N-1}				
X	↓	R_1 R_2 R_3 ... R_{N-1} R_N	R_N				
		X X X ... X X	X	L	R_1 R_2 R_3 ... R_{N-1} R_N		
		P_1 P_2 P_3 ... P_{N-1} P_N	P_N	H	P_1 P_2 P_3 ... P_{N-1} P_N	L	P_1 P_2 P_3 ... P_{N-1} P_N
					X X X ... X X	H	L L L ... L L

L = Low Logic Level H = High Logic Level X = Irrelevant P = Present State R = Previous State

6812
20-BIT SERIAL-INPUT, LATCHED SOURCE DRIVER

ELECTRICAL CHARACTERISTICS at T_A = +25°C (A6812S-) or over operating temperature range (A6812E-), V_{BB} = 60 V unless otherwise noted.

Characteristic	Symbol	Test Conditions	Limits @ V_{DD} = 3.3 V			Limits @ V_{DD} = 5 V			Units
			Mln.	Typ.	Max.	Min.	Typ.	Max.	
Output Leakage Current	I_{CEX}	V_{OUT} = 0 V	—	<-0.1	-15	—	<-0.1	-15	µA
Output Voltage	$V_{OUT(1)}$	I_{OUT} = -25 mA	57.5	58.3	—	57.5	58.3	—	V
	$V_{OUT(0)}$	I_{OUT} = 1 mA	—	1.0	1.5	—	1.0	1.5	V
Output Pull-Down Current	$I_{OUT(0)}$	V_{OUT} = 5 V to V_{BB}	2.5	5.0	—	2.5	5.0	—	mA
Input Voltage	$V_{IN(1)}$		2.2	—	—	3.3	—	—	V
	$V_{IN(0)}$		—	—	1.1	—	—	1.7	V
Input Current	$I_{IN(1)}$	V_{IN} = V_{DD}	—	<0.01	1.0	—	<0.01	1.0	µA
	$I_{IN(0)}$	V_{IN} = 0 V	—	<-0.01	-1.0	—	<-0.01	-1.0	µA
Input Clamp Voltage	V_{IK}	I_{IN} = -200 µA	—	-0.8	-1.5	—	-0.8	-1.5	V
Serial Data Output Voltage	$V_{OUT(1)}$	I_{OUT} = -200 µA	2.8	3.05	—	4.5	4.75	—	V
	$V_{OUT(0)}$	I_{OUT} = 200 µA	—	0.15	0.3	—	0.15	0.3	V
Maximum Clock Frequency	f_c		10*	—	—	10*	—	—	MHz
Logic Supply Current	$I_{DD(1)}$	All Outputs High	—	0.25	0.75	—	0.3	1.0	mA
	$I_{DD(0)}$	All Outputs Low	—	0.25	0.75	—	0.3	1.0	mA
Load Supply Current	$I_{BB(1)}$	All Outputs High, No Load	—	3.0	6.0	—	3.0	6.0	mA
	$I_{BB(0)}$	All Outputs Low	—	0.2	20	—	0.2	20	µA
Blanking-to-Output Delay	$t_{dis(BQ)}$	C_L = 30 pF, 50% to 50%	—	0.7	2.0	—	0.7	2.0	µs
	$t_{en(BQ)}$	C_L = 30 pF, 50% to 50%	—	1.8	3.0	—	1.8	3.0	µs
Strobe-to-Output Delay	$t_{p(STH-QL)}$	R_L = 2.3 kΩ, C_L ≤ 30 pF	—	0.7	2.0	—	0.7	2.0	µs
	$t_{p(STH-QH)}$	R_L = 2.3 kΩ, C_L ≤ 30 pF	—	1.8	3.0	—	1.8	3.0	µs
Output Fall Time	t_f	R_L = 2.3 kΩ, C_L ≤ 30 pF	2.4	—	12	2.4	—	12	µs
Output Rise Time	t_r	R_L = 2.3 kΩ, C_L ≤ 30 pF	2.4	—	12	2.4	—	12	µs
Output Slew Rate	dV/dt	R_L = 2.3 kΩ, C_L ≤ 30 pF	4.0	—	20	4.0	—	20	V/µs
Clock-to-Serial Data Out Delay	$t_{p(CH-SQX)}$	I_{OUT} = ±200 µA	—	50	—	—	50	—	ns

Negative current is defined as coming out of (sourcing) the specified device terminal.

Typical data is is for design information only and is at T_A = +25°C.

* Operation at a clock frequency greater than the specified minimum is possible but not warranteed.

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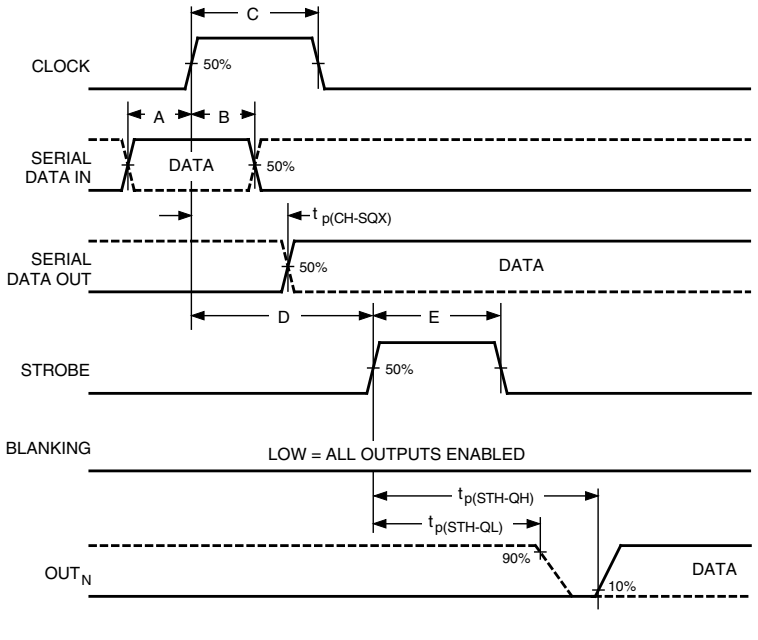
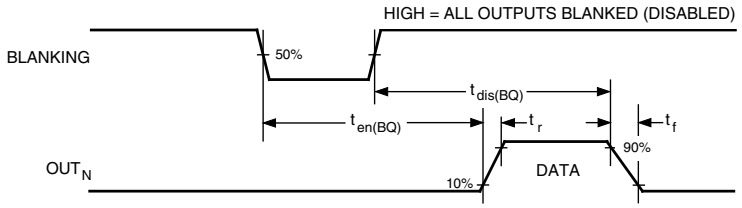
TIMING REQUIREMENTS and SPECIFICATIONS
(Logic Levels are V_{DD} and Ground)



Dwg. WP-029



Dwg. WP-030

A. Data Active Time Before Clock Pulse (Data Set-Up Time), $t_{su(D)}$ ..... **25 ns**
B. Data Active Time After Clock Pulse (Data Hold Time), $t_{h(D)}$ ..... **25 ns**
C. Clock Pulse Width, $t_{w(CH)}$ ..... **50 ns**
D. Time Between Clock Activation and Strobe, $t_{su(C)}$ .... **100 ns**
E. Strobe Pulse Width, $t_{w(STH)}$ ..... **50 ns**

NOTE – Timing is representative of a 10 MHz clock. Higher speeds may be attainable with increased supply voltage; operation at high temperatures will reduce the specified maximum clock frequency.

Serial Data present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

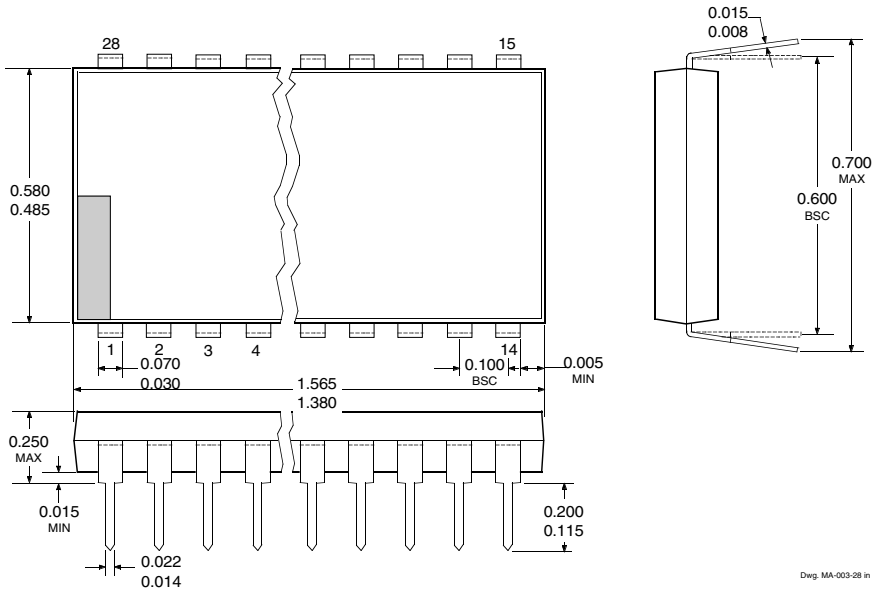
Information present at any register is transferred to the respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the BLANKING input be high during serial data entry.

When the BLANKING input is high, the output source drivers are disabled (OFF); the pnp active pull-down sink drivers are ON. The information stored in the latches is not affected by the BLANKING input. With the BLANKING input low, the outputs are controlled by the state of their respective latches.

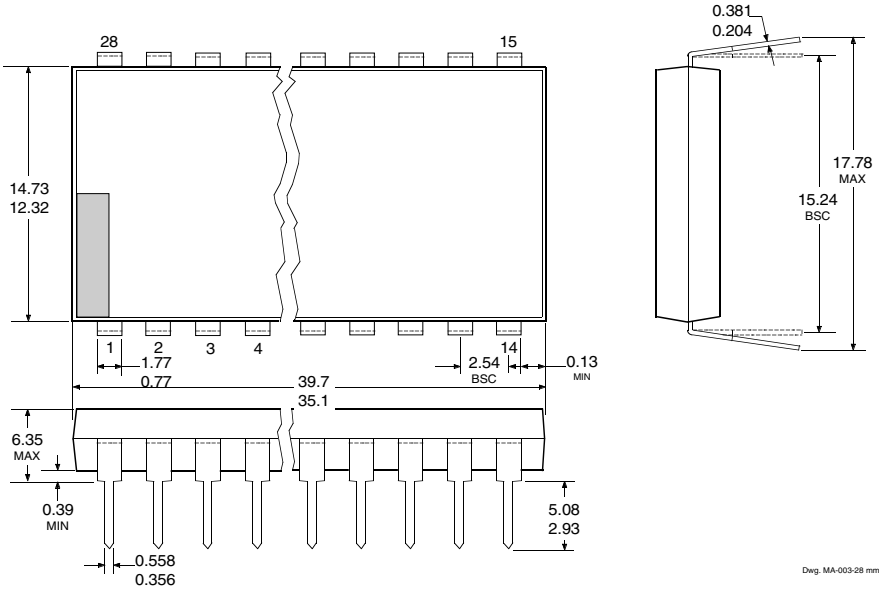
6812
20-BIT SERIAL-INPUT, LATCHED SOURCE DRIVER

A6812EA & A6812SA

Dimensions in Inches
(controlling dimensions)



Dimensions in Millimeters
(for reference only)



NOTES: 1. Exact body and lead configuration at vendor's option within limits shown.
2. Lead spacing tolerance is non-cumulative.
3. Lead thickness is measured at seating plane or below.
4. Supplied in standard sticks/tubes of 12 devices.

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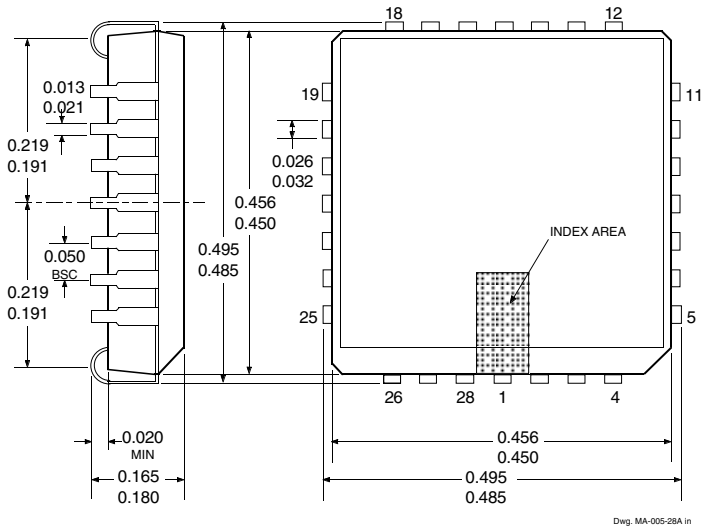
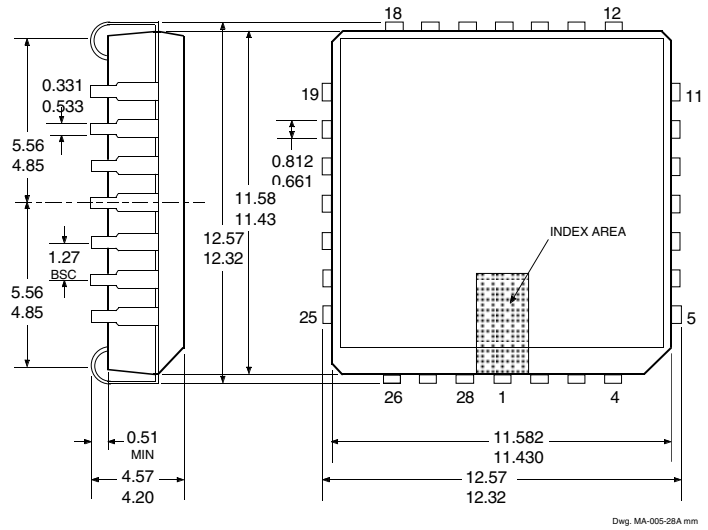
A6812EEP & A6812SEP

(add “TR” to part number for tape and reel)
Dimensions in Inches
(controlling dimensions)



Dimensions in Millimeters
(for reference only))

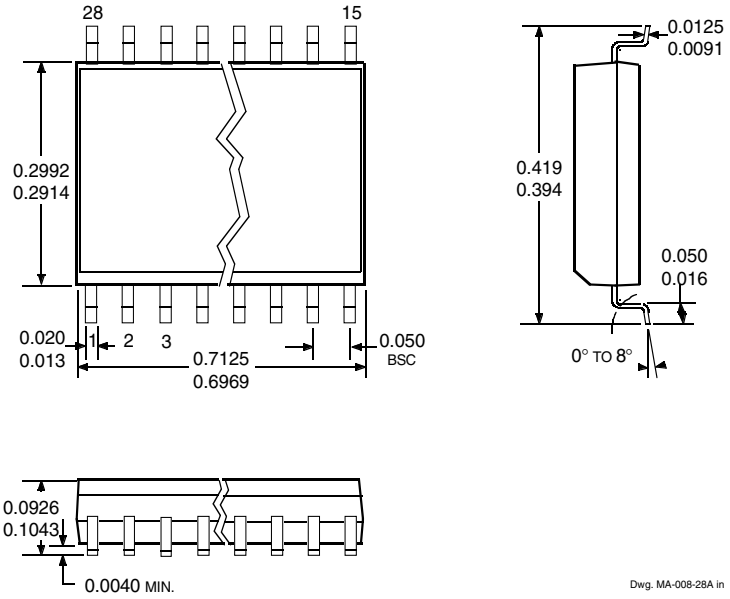


NOTES: 1. Exact body and lead configuration at vendor’s option within limits shown.
2. Lead spacing tolerance is non-cumulative.
3. Supplied in standard sticks/tubes of 38 devices or add “TR” to part number for tape and reel.

6812
20-BIT SERIAL-INPUT, LATCHED SOURCE DRIVER

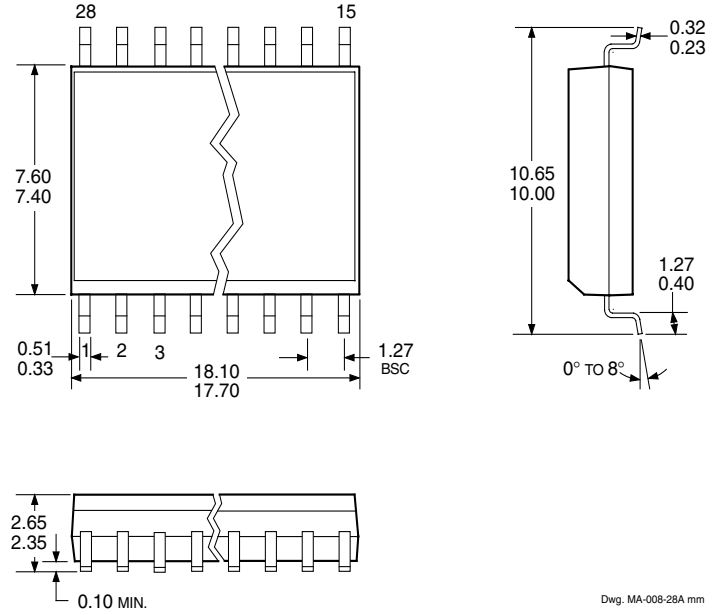
A6812ELW & A6812SLW

(add “TR” to part number for tape and reel)
Dimensions in Inches
(for reference only)



Dwg. MA-008-28A in

Dimensions in Millimeters
(controlling dimensions)



Dwg. MA-008-28A mm

NOTES: 1. Exact body and lead configuration at vendor’s option within limits shown.
2. Lead spacing tolerance is non-cumulative.
3. Supplied in standard sticks/tubes of 27 devices or add “TR” to part number for tape and reel.

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6812
20-BIT SERIAL-INPUT, LATCHED SOURCE DRIVER

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20-BIT SERIAL-INPUT, LATCHED SOURCE DRIVER

POWER INTERFACE DRIVERS

Function	Output Ratings*		Part Number†
SERIAL-INPUT LATCHED DRIVERS			
8-Bit (saturated drivers)	-120 mA	50 V‡	5895
8-Bit	350 mA	50 V	5821
8-Bit	350 mA	80 V	5822
8-Bit	350 mA	50 V‡	5841
8-Bit	350 mA	80 V‡	5842
8-Bit (constant-current LED driver)	75 mA	17 V	6275
8-Bit (DMOS drivers)	250 mA	50 V	6595
8-Bit (DMOS drivers)	350 mA	50 V‡	6A595
8-Bit (DMOS drivers)	100 mA	50 V	6B595
10-Bit (active pull-downs)	-25 mA	60 V	5810-F and 6809/10
12-Bit (active pull-downs)	-25 mA	60 V	5811 and 6811
16-Bit (constant-current LED driver)	75 mA	17 V	6276
20-Bit (active pull-downs)	-25 mA	60 V	5812-F and 6812
32-Bit (active pull-downs)	-25 mA	60 V	5818-F and 6818
32-Bit	100 mA	30 V	5833
32-Bit (saturated drivers)	100 mA	40 V	5832
PARALLEL-INPUT LATCHED DRIVERS			
4-Bit	350 mA	50 V‡	5800
8-Bit	-25 mA	60 V	5815
8-Bit	350 mA	50 V‡	5801
8-Bit (DMOS drivers)	100 mA	50 V	6B273
8-Bit (DMOS drivers)	250 mA	50 V	6273
SPECIAL-PURPOSE DEVICES			
Unipolar Stepper Motor Translator/Driver	1.25 A	50 V‡	5804
Addressable 8-Bit Decoder/DMOS Driver	250 mA	50 V	6259
Addressable 8-Bit Decoder/DMOS Driver	350 mA	50 V‡	6A259
Addressable 8-Bit Decoder/DMOS Driver	100 mA	50 V	6B259
Addressable 28-Line Decoder/Driver	450 mA	30 V	6817

* Current is maximum specified test condition, voltage is maximum rating. See specification for sustaining voltage limits. Negative current is defined as coming out of (sourcing) the output.

† Complete part number includes additional characters to indicate operating temperature range and package style.

‡ Internal transient-suppression diodes included for inductive-load protection.

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