

# AS3902

# **ISM 433 MHz ASK Transmitter**

Preliminary Data Sheet Rev. A7, December 2000



# Key Features

- Supports the European 433 MHz ISM band.
- No frequency pulling by (antenna) load variation due to PLL synthesizer.
- Designed to be conform to EN 300 220-1 requirements.
- ASK data rate range from 0 to 32 kbit/s.
- Supports clock and reset signals for the external  $\mu C.$  Therefore no separate  $\mu C$  XTAL is required.
- Supports total shut down mode without any running XTAL oscillator.
- Typically 2 external resistors and 3 capacitors required.
- FSK operation by XTAL pulling possible.
- 315 MHz US ISM band application possible.
- Wide supply range between 2.7 V to 5 V.
- Low TX current, typical 8 mA @ transmitting a High ("H"), 1 mA @ transmitting a Low ("L").
- Wide operating temperature range from -40 °C to +85 °C.
- Miniature surface mount 8 pin MSOP (preferred) or SOIC package.

# **General Description**

The AS3902 is a single channel low power 433 MHz ASK transmitter. It uses a fully integrated PLL stabilized RF-oscillator which avoids frequency pulling by approaching the antenna with objects as it occurs at SAW resonator based transmitters. ASK modulation is performed by switching the transmitter on and off by an applied data stream.

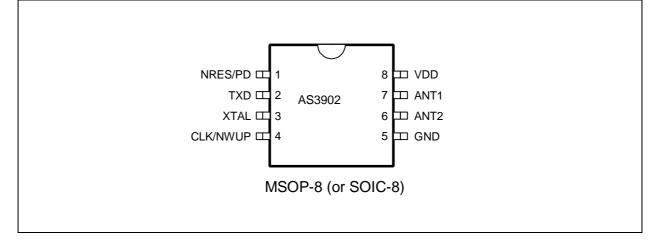
The AS3902 contains a bi-directional three line micro-controller ( $\mu$ C) interface to support the  $\mu$ C with a clock and a reset signal and to operate the highly efficient power up/down management (including clock-free total shut-down) of the AS3902 by the  $\mu$ C.

As external components the AS3902 need only a reference XTAL, three capacitors and up to two resistors.

# Applications

- Short range radio data transmission.
- Remote keyless entry systems.
- Domestic and consumer remote control units.
- Cordless alarm systems.
- Remote metering.
- Low power telemetry.





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# 1 Functional Description

The AS3902 consists of a reference XTAL oscillator, a single channel RF- synthesizer, a driving amplifier and a  $\mu$ C interface, including microprocessor clock divider and a sophisticated power up/down circuitry.

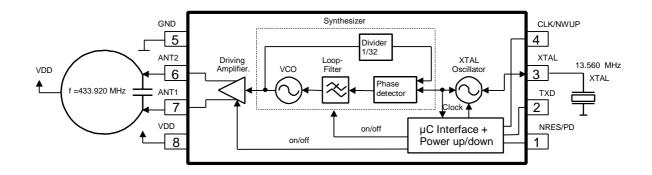


Figure 1: Block diagram of the AS3902.

### 1.1 RF Synthesizer

The RF synthesizer is a fully integrated single channel device with internal loop filter, generating the 433 MHz transmit carrier frequency  $f_{RF}$  by a fix, 32 times, multiplication of the reference XTAL frequency  $f_{XTAL}$ .

### 1.2 Microprocessor Clock

The microprocessor clock frequency  $f_{\text{CLK}}$  is generated by dividing the XTAL frequency  $f_{\text{XTAL}}$  by 4.



### 1.3 Modulation

ASK modulation with a data rate from 0 up to 32 kbit/s (for continuous 101010... modulation pattern) is done by turning the synthesizer and the driving amplifier on and off, whereas a TXD = "H" means a turned on state.

When TXD = "H", at first the synthesizer is turned on. The following turning on of the driving amplifier is internally delayed for  $t_{DRON}$  of 21 µs (=72 clock pulses of the µC clock) to allow the synthesizer to lock and settle its frequency prior to transmitting. When TXD becomes "L", both, synthesizer and driving amplifier are turned off to save power. In this case the synthesizer turn off is delayed for 21 µs.

## 1.4 Driving Amplifier

The driving amplifier has a differential open collector output optimized for driving of small, symmetrical high-impedance loop antennas. The amplifier drives a nominal RF current of 0.7 mA<sub>rms</sub>. The maximal differential voltage swing is about 4 V<sub>PP</sub> (1.4 V<sub>RMS</sub>). Therefore the output power is a function of the connected load impedance. With a 2 k $\Omega$  differential load a nominal output power (to the antenna) of ≈1 mW is obtained. Please note that the finally radiated power (from antenna) is lower and strongly dependent on the efficiency (function of the size) of the antenna to be used.

### 1.5 µC Interface and Power Management

The AS3902 contains a direct interface to a microcontroller ( $\mu$ C). The  $\mu$ C interface of the AS3902 consists of the following three pins:

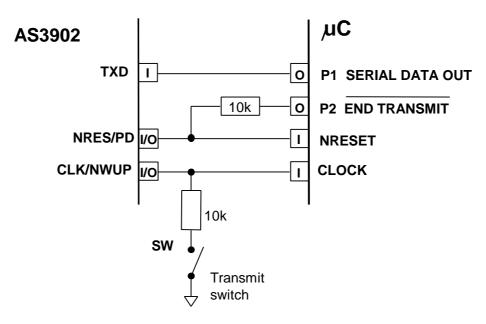
"Transmit data input" (TXD).

"Active "L" µC reset output/transmitter power down input" (NRES/PD).

"µC clock output/active "L" wake-up input" (CLK/NWUP).

These lines support the  $\mu$ C with the required reset and clock signals and control the AS3902 internal power on/off circuit which wakes up and shuts down the whole transmitter consisting of the AS3902 and the  $\mu$ C.

Figure 2 shows a typical interconnection of the AS3902 with a typical  $\mu$ C. Figure 3 presents a related timing for power up and down of the transmitter.



#### Figure 2: Interconnection of the AS3902 with a typical $\mu$ C.

Note: At room temperature, resistor values of  $\approx 10 \ k\Omega$  are suggested for the  $\mu$ C interface. For other temperatures to be calculated from figure 6.



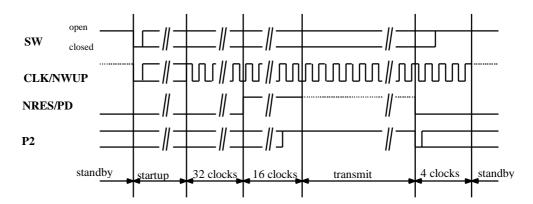


Figure 3:  $\mu$ C interface timing for a transmission cycle.

Note: The dashed lines indicate weak high or low state when the CLK/NWUP or NRES/PD output of the AS3902 is disabled (in high-resistive Z state) and pulled "H" or "L" by the internal pull-up device or by the μC via a resistor. These weak states can be overridden by the AS3902 if the respective outputs are enabled. Whenever a line is pulled via an external resistor, however, this should override the internal pull-up devices of the AS3902.

#### **1.5.1** Interface Description

It is assumed that the  $\mu$ C remains in low power standby mode as long as the P2 pin is kept "L" and no clock cycles are applied.

**Standby:** During standby (default after  $V_{cc}$ -on) the XTAL oscillator is turned off and AS3902 holds the  $\mu$ C in a reset state:

The AS3902 NRES/PD pin is active and set to "L", holding the  $\mu$ C in reset state. In standby mode the AS3902 internal NRES/PD pull-up is disabled and does not drain current from the supply.

The AS3902 CLK/NWUP output is disabled, (in high resistive "Z" state) and internally pulled up to "H".

(Re)starting the transmitter: Closing the push button (giving a falling edge on CLK/NWUP-CLOCK line) starts up the AS3902. It turns on its XTAL oscillator and after the oscillator start up phase it turns the CLK/NWUP pin to active (CMOS level) mode and provides a clock to the  $\mu$ C.

After a delay of  $32 \ \mu$ C clock cycles the NRES/PD pin of the AS3902 is set to "H" for 16 clock cycles. The transmitter is now in active mode. The NRES/PD acts in AS3902 active mode as an input waiting for a "L" to trigger the transmission of the transmitter to standby mode.

During this active mode the  $\mu$ C can turn on and off the synthesizer and driving amplifier in the rhythm of the data on the TX - P1 (Serial data out) line and transmit ASK data.

**Bringing the transmitter to standby:** After completing the transmission, the  $\mu$ C may indicate "end of transmission" by setting P2 (not end of transmit) to "L" and pulls the NRES/PD-NRESET line to "L". Sensing this, 4 clock cycles later the AS3902 will switch back to standby mode, disabling the CLK/NWUP output, setting the active NRES/PD pin to "L" and turning off the XTAL oscillator.

**Repetitive transmission:** If the button is still pressed when the  $\mu$ C indicates "end of transmission" by setting P2 pin to "L" and pulling the NRES/PD-NRESET line to "L", 4  $\mu$ C clock periods later the sequence above will be repeated starting from the 32 clock delay period. Due to the sophisticated tri-state - active/inactive pull-up configuration of the NRES/PD pin the

AS3902 does not drain current during its standby periods.



#### **Electrical Characteristics** 2

Symbol	Parameter Min Max		Мах	Units	Note
VDD	Positive supply voltage	-0.5	7	V	
GND	Negative supply voltage	0	0	V	
V <sub>IN</sub>	Voltage on input pins	-0.5	VDD+0.5	V	
ESD	Electrostatic discharge		1000	V	1)
T <sub>STG</sub>	Storage temperature	-55	125	°C	
T <sub>LEAD</sub>	Lead temperature		260	°C	2)

### 2.1 Absolute Maximum Ratings (non operating)

Note:

HBM: R = 1.5 k\Omega, C = 100 pF. The pins ANT1, ANT2 and XTAL have 500 V ESD protection.

1) 2) 260 °C for 10 s (reflow and wave soldering), 360 °C for 3 s (manual soldering).

## 2.2 Operating Conditions

Symbol	Parameter	Min	Тур	Max	Unit	Note
VDD	Positive supply voltage	2.7	3.0	5.0	V	
GND	Negative supply voltage	0	0	0	V	
IDD	Supply current in active mode transmitted "L" (TXD="L").		1	1500	μA	1)
IDD	Supply current in active mode, transmitted "H" (TXD="H").		7.7	9	mA	2)
IDD(off)	Supply current in standby mode			1	μA	
T <sub>AMB</sub>	Ambient temperature range	-40		+85	°C	

Note: 1) 2)

 $T_{AMB}$  =23 °C, Synthesizer and driving amplifier are turned off, for worst case process and maximum supply voltage: 5mA  $T_{AMB}$  =23 °C, Synthesizer and driving amplifier are turned on, for worst case process and maximum supply voltage: 12mA



### 2.3 ASK Operation

Symbol	Parameter	Conditions	Min	Тур	Max	Units	Note
f <sub>RF</sub>	Transmit frequency (Europe)	f <sub>XTAL</sub> = 13.560 MHz		433,920		MHz	1)
P <sub>OUT</sub> ,H	Available output power	In 2 kΩ, TXD = "H"		0		dB <sub>m</sub>	2)
P <sub>OUT</sub> ,L	Leakage output power	In 2 kΩ, TXD = "L"		-inf.	-80	dB <sub>m</sub>	
P <sub>OUT</sub> 3rd	Radiated third harmonic output power	Antenna attenuation > 20 dB		-30		dB <sub>C</sub>	
P <sub>SP</sub>	Spurious power	In distance of $f_{CLK}$ or $f_{XTAL}$ from carrier.		-25		dB <sub>C</sub>	3)
f <sub>CLK</sub>	µC clock frequency			3.390		MHz	
t <sub>swm</sub>	Minimum switch close time			1		ms	
t <sub>STUP</sub>	Start up time	Until clock output		2		ms	
t <sub>DRON</sub>	Driving amplifier turn on delay			21		μs	
R <sub>ASK</sub>	ASK data rate range	For a RF packet duty cycle ≥45 %.	0		32	kb/s	4)
t <sub>r,f</sub>	Carrier rise / fall time			8		μs	

Note:

1) 2) XTAL tolerances will slightly change the typical transmit frequency.

Output power depends on load impedance, differential output current is typical 0.7 mA<sub>rms</sub>. Maximum differential voltage swing is typical 4  $V_{PP}$  (1.4  $V_{RMS}$ ). Actual E.I.R.P. depends on antenna efficiency. Measurement bandwidth (according to EN 300 220-1) see also figure 10. Actual radiated spurious power depends on antenna efficentcy and antenna selectivity. Measured with loop antenna (demo board).

3)

4) Guaranteed, higher data rates possible.



### 2.4 Digital Pin Characteristics

 $T_{AMB}$  = 23 °C, VDD = 3.0 V, unless specified otherwise. GND is the 0 V reference. Input parameters for bi-directional pins (CLK/NWUP, NRES/PD) are valid at disabled outputs.

Symbol	Parameter	Conditions	Min	Тур	Max	Units	Note
CLK/NWU	IP (μC clock output / wak	e-up input)					
VOH	High level output voltage	IOH =-1 mA	VDD-0.5	-		V	
VOL	Low level output voltage	IOL =1 mA		-	0.6	V	
tr	Rise time	CLoad = 10 pF		20		ns	
td	Fall time	CLoad = 10 pF		20		ns	
jcc	Cycle to cycle jitter				+/-5	%	1)
VIH	High level input voltage		VDD-0.5	-		V	
VIL	Low level input voltage			-	0.3	V	
IIH	High level input current	VIH = VDD			1	μA	
IIL	Low level input current	VIL =0 V; Due to internal pull-up	-17			μA	2)
TX (serial	data input)					1	1
VIH	High level input voltage		VDD-0.5	-		V	
VIL	Low level input voltage			-	0.3	V	
IIH	High level input current	VIH= VDD; Due to internal pull-down			35	μA	
IIL	Low level input current	VIL =0 V	-1			μA	
NRES/PD	(µC reset output / transm	nitter power down i	input)				
VOH	High level output voltage	IOH = -1mA	VDD-0.5	-		V	
VOL	Low level output voltage	IOL = 1mA		-	0.6	V	
VIH	High level input voltage		VDD-0.5	-		V	
VIL	Low level input voltage			-	0.3	V	
IIH	High level input current	VIH = VDD			1	μA	
IIL	Low level input current	VIL =0 V; Due to internal pull-up	-17			μA	2)

Note:

1) 2) guaranteed by design

cf. Figure 6



Pin #	Pin Name	Input / Output	Description
1	NRES/PD	Dig. tri-state I/O, pull up during active cycle	μC reset output/transmitter power down input
2	TXD	Dig. Input with pull down	Transmit data input
3	XTAL	Analog I/O	XTAL pin
4	CLK/NWUP	Dig. tri-state I/O with pull up	μC clock output/wake-up input (push but- ton)
5	GND	Power	Ground
6	ANT2	Analog open collector output	To loop antenna
7	ANT1	Analog open collector output	To loop antenna
8	VDD	Power	Positive supply

# 3 Pin-out Information

# **4** Application Schematic

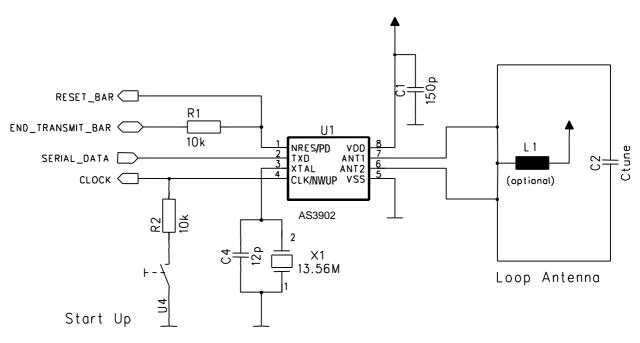


Figure 5: Basic application schematic of the AS3902.



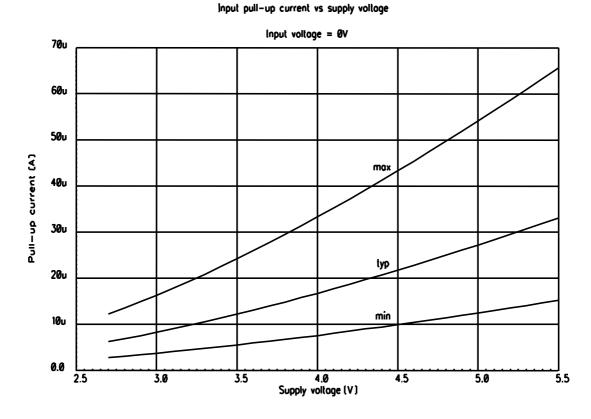
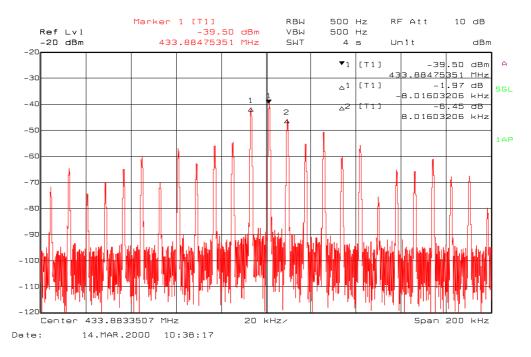


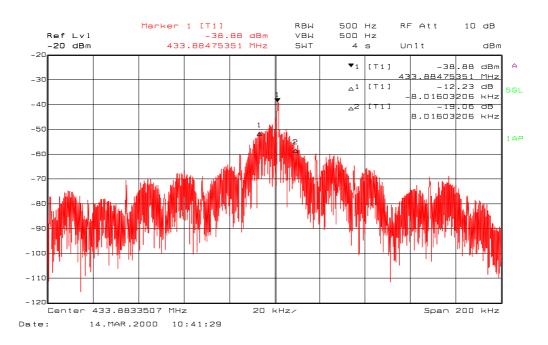
Figure 6: Pull up characteristics for the CLK/NWUP and NRES/PD pin.



# 5 Typical Measurements



*Figure 7:* Narrow band output spectrum of the AS3902 modulated with a 0101-.. data pattern at 16 kbit/s.



*Figure 8:* Narrow band output spectrum of the AS3902 modulated with pseudo random data at 16 kbit/s.



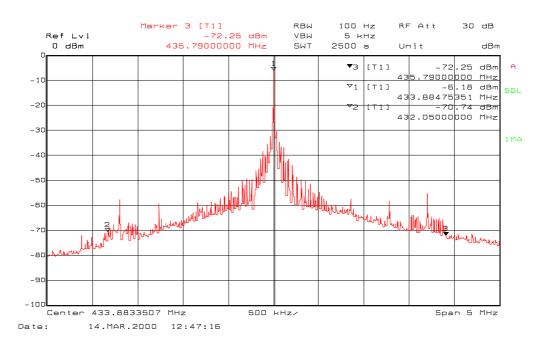
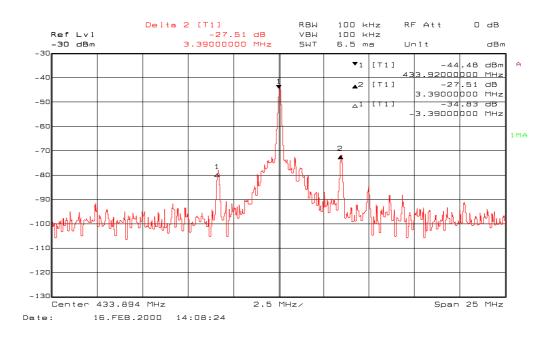
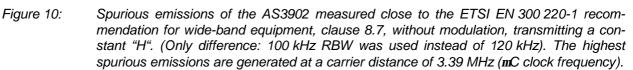


Figure 9: Modulation bandwidth of the AS3902 at 16 kbit/s, measured close to the ETSI EN 300 220-1 recommendation for wide-band equipment, clause 8.6. (Only difference: 5 kHz VBW was used instead of 10 kHz). From EN 300 220-1 the modulation bandwidth is defined to be the frequency difference between the points wherein the power level is above -36 dBm. Therefore the bandwidth value is dependent on the E.I.R.P. and should be within the ISM band limits. The marker settings correspond to the limits of the 433 MHz ISM band.







The EN 300 220-1 specifies an absolute level of -36 dBm E.I.R.P. for spurious emissions. This limits the maximum E.I.R.P. for a transmitter using the AS3902 to about -11 dBm.

Measurement was performed over a free-space link using R&S HL040 antenna for reception.

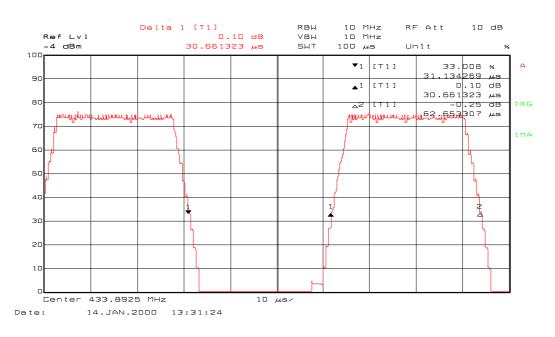


Figure 11: Demodulated RF wave for 10101... data pattern at 32kbit/s (linear scale)



# 6 Package Information

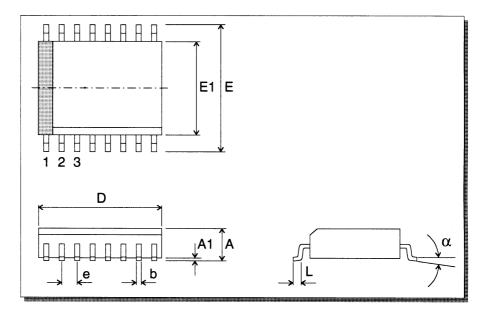


Figure 12:	Physical package dimensions.
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Symbol	8 pi	n SOIC Dimens	sions	8 pin MSOP Dimensions			
	Minimal (mm/mil)	Nominal (mm/mil)	Maximal (mm/mil)	Minimal (mm/mil)	Nominal (mm/mil)	Maximal (mm/mil)	
Α	1.35/0.053		1.75/0.069	0.94/0.037	1.01/0.04	1.09/0.043	
A1	0.10/0.004		0.25/0.010	0.05/0.002	0.10/0.004	0.15/0.006	
b	0.33/0.013		0.51/0.020	0.32/0.0125	0.33/0.0130	0.34/0.0135	
D	4.80/0.189	-	5.00/0.197	2.90/0.114	3.00/0.118	3.10/0.122	
е	1.27/0.050			0.65/0.0256 BSC			
E	5.80/0.228		6.20/0.244	4.75/0.187	4.90/0.193	5.05/0.199	
E1	3.80/0.150	-	4.00/0.157	2.90/0.114	0.30/0.118	3.10/0.122	
L	0.40/0.016		1.27/0.050	0.53/0.0209	0.55/0.0215	0.56/0.0221	
α	0°		8°	0°	3°	6°	

AS's are functional and in-spec circuits which are usually available as samples with documentation and demoboard. However they are intentionally to be used as a basis for ASIC derivatives. If an AS fits into a customer's application as it is, it will be immediately qualified and transfered to an ASSP to be ordered as a regular AS product.

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