

Features

- Depop Circuitry Integrated
- Thermal Shutdown Circuitry Integrated
- Bridge-Tied Load (BTL) or Single-Ended (SE) Modes Operation
- Output Power at 1% THD+N, $V_{DD}=5V$
 - 2.2W/Ch (typ) into a 3 Ω Load
 - 1.8W/Ch (typ) into a 4 Ω Load
 - 1.2 W/Ch (typ) into a 8 Ω Load
- Shutdown Control Mode, $I_{SD} = 0.5 \mu A$
- Output Power (SE) at 0.5% THD+N, $V_{DD}=5V$
 - 90mW/Ch (typ.) into a 32 Ω Load
- Various Power Packages Available
SOP, TSSOP, TSSOP-P

Applications

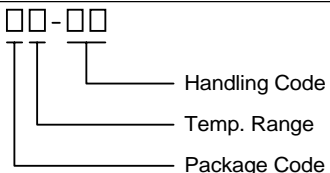
- Stereo Audio Power Amplifier for Notebook Computer
- Portable Televisions
- Portable and Desktop Computers

General Description

The APA4863 is a stereo bridge-tied audio power amplifier in various power packages , including SOP , TSSOP and TSSOP-P . When connecting to a 5V voltage supply , the APA4863 is capable of delivering 2.2W/1.8W/1.2W of continuous RMS power per channel into 3 Ω /4 Ω /8 Ω bridge-tied loads with less than 1% THD+N respectively . When APA4863 operates in the single-ended load , it is capable of delivering 90mW of continuous RMS power per channel into 32 Ω load . The APA4863 simplifies design and frees up board space for other features .

The APA4863 also served well in low-voltage applications , which provides 750mW (1% THD+N) per channel into 4 Ω loads with a 3.3V supply voltage . Both of the depop circuitry and the thermal shutdown protection circuitry are integrated in the APA4863 , that reduces pops and clicks noise during power up and when using the shutdown mode and protects the chip from being destroyed by over-temperature failure . To simplify the audio system design in notebook computer applications , the APA4863 combines a stereo bridge-tied loads mode for speaker drive and a stereo single-end mode for headphone drive into a single chip , where both modes are easily switched by the HP-IN input control pin signal . For power sensitive applications , the APA4863 also features a shutdown function which keeps the supply current only 0.5 μA (typ.) .

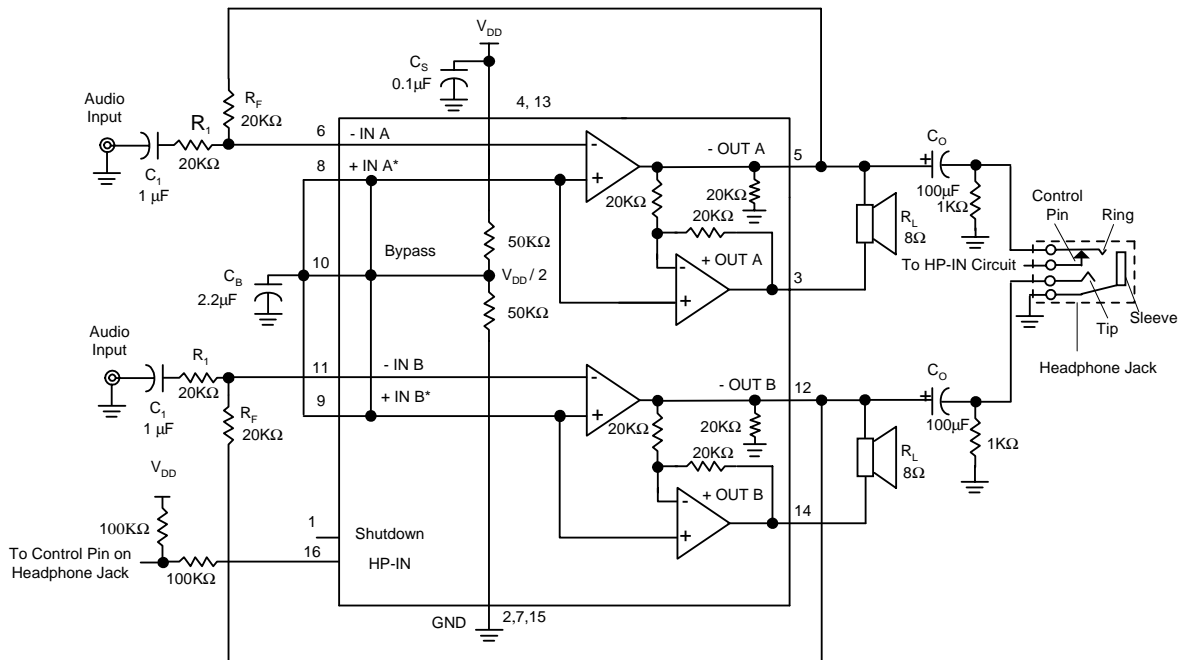
Ordering Information

<p>APA4863 □□-□□</p>  <p>Handling Code</p> <p>Temp. Range</p> <p>Package Code</p>	<p>Package Code</p> <p>K: SOP R: TSSOP-P*</p> <p>O: TSSOP</p> <p>Temp. Range</p> <p>I : -40 to 85 °C</p> <p>Handling Code</p> <p>TU : Tube</p> <p>TR : Tape & Reel TY: Tray</p>
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* TSSOP-P is a standard TSSOP package with a thermal pad exposed on the bottom of the package.

ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

Block Diagram



* +INA and +INB pins are connected to Bypass pin inside the IC.

Absolute Maximum Ratings

(Over operating free-air temperature range unless otherwise noted.)

Symbol	Parameter	Rating	Unit
V_{DD}	Supply Voltage	6	V
T_A	Operating Ambient Temperature Range	-40 to 85	°C
T_J	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature Range	-65 to +150	°C
T_S	Soldering Temperature, 10 seconds	260	°C
V_{ESD}	Electrostatic Discharge	-2000 to 2000 *1	V

Note: *1. Human body model : C=100pF, R=1500Ω, 3 positive pulses plus 3 negative pulses

Recommended Operating Conditions

			Min.	Typ.	Max.	Unit
Supply Voltage, V_{DD}			3	5	5.5	V
Operating free-air temperature, T_A	$V_{DD}=5V$, 250mW/Ch average power	4- Ω stereo BTL drive, with proper PCB design	-20		85	$^{\circ}C$
	$V_{DD}=5V$, 1.8 W/Ch average power	4- Ω stereo BTL drive, with proper PCB design and 300 CFM forced-air cooling	-20		85	
Common mode input voltage, V_{ICM}	$V_{DD}=5 V$		1.25		4.5	V
	$V_{DD}=3.3V$		1.25		2.7	

Dissipation Rating Table

Package	Air Flow (CFM)	Thermal Resistance $\theta_{JA}(^{\circ}C/W)$	$T_A \leq 25^{\circ}C$	$T_A = 70^{\circ}C$
SO16 +	0	50	2.5W	1.6W
TSSOP ++	0	73.2	1.7W	1.1W
	200	66.6	1.8W	1.2W
TSSOP-P ++	0	37.6	3.3W	2.1W
	200	32.3	3.8W	2.4W

+ : The parameter is measured with the recommended copper heat sink pattern on an 2-layer PCB, 11.7 in² 3.0x2.4 in² in PCB, 1oz. copper, 3.0x1.5 in² in coverage at Top-layer and Bottom-layer at 100% coverage (7.2in²).

++: The parameter is measured with the JEDEC standard test boards (multi-layer PCB).

Electical Characteristics

Electrical Characteristics for Entire IC

The following specifications apply for $V_{DD} = 5V$ unless otherwise noted. Limits apply for $T_A = 25^{\circ}C$

Symbol	Parameter	Test Conditions	APA4863			Unit
			Min.	Typ.	Max.	
V_{DD}	Supply Voltage		3		5.5	V
I_{DD}	Quiescent Power Supply Current	$V_{IN}=0V, I_O=0A, HP-IN=0V$ $V_{IN}=0V, I_O=0A, HP-IN=4V$		9 5	13.5 7.5	mA
I_{SD}	Shutdown Current	$V_{PIN1} = V_{DD}$	5	0.5		μA
V_{IH}	Headphone High Input Voltage		4			V
V_{IL}	Headphone Low Input Voltage				0.8	V

Electical Characteristics Cont.

Electrical Characteristics for BTL Mode Operation

The following specifications apply for $V_{DD}=5V$ unless otherwise noted. Limits apply for $T_A=25^\circ C$

Symbol	Parameter	Test Conditions	APA4863	Unit
			Typ.	
V_{OS}	Output Offset Voltage	$V_{IN}=0V$	5	mV
P_O	Output Power	THD=1%, $f=1kHz$ $R_L=3\Omega$ $R_L=4\Omega$ $R_L=8\Omega$	2.2 1.8 1.2	W
		THD=10%, $f=1kHz$ $R_L=3\Omega$ $R_L=4\Omega$ $R_L=8\Omega$	2.7 2.3 1.5	
THD+N	Total Harmonic Distortion + Noise	$A_{VD}=2$, $f=1kHz$ $R_L=4\Omega$, $P_O=1.8W$ $R_L=8\Omega$, $P_O=1W$	0.3 0.15	%
RSRR	Power Supply Rejection Ratio	$V_{DD}=5V$, $V_{RIPPLE}=200mV_{RMS}$, $R_L=8\Omega$ $C_B=2.2\mu F$	64	dB
X_{TALK}	Channel Separation	$f=1kHz$, $C_B=2.2\mu F$, $P_O=1W$, $R_L=8\Omega$	90	dB
SNR	Signal-to-Noise Ratio	$V_{DD}=5V$, $P_O=1.1W$, $R_L=8\Omega$	95	dB

Electrical Characteristics for SE Mode Operation

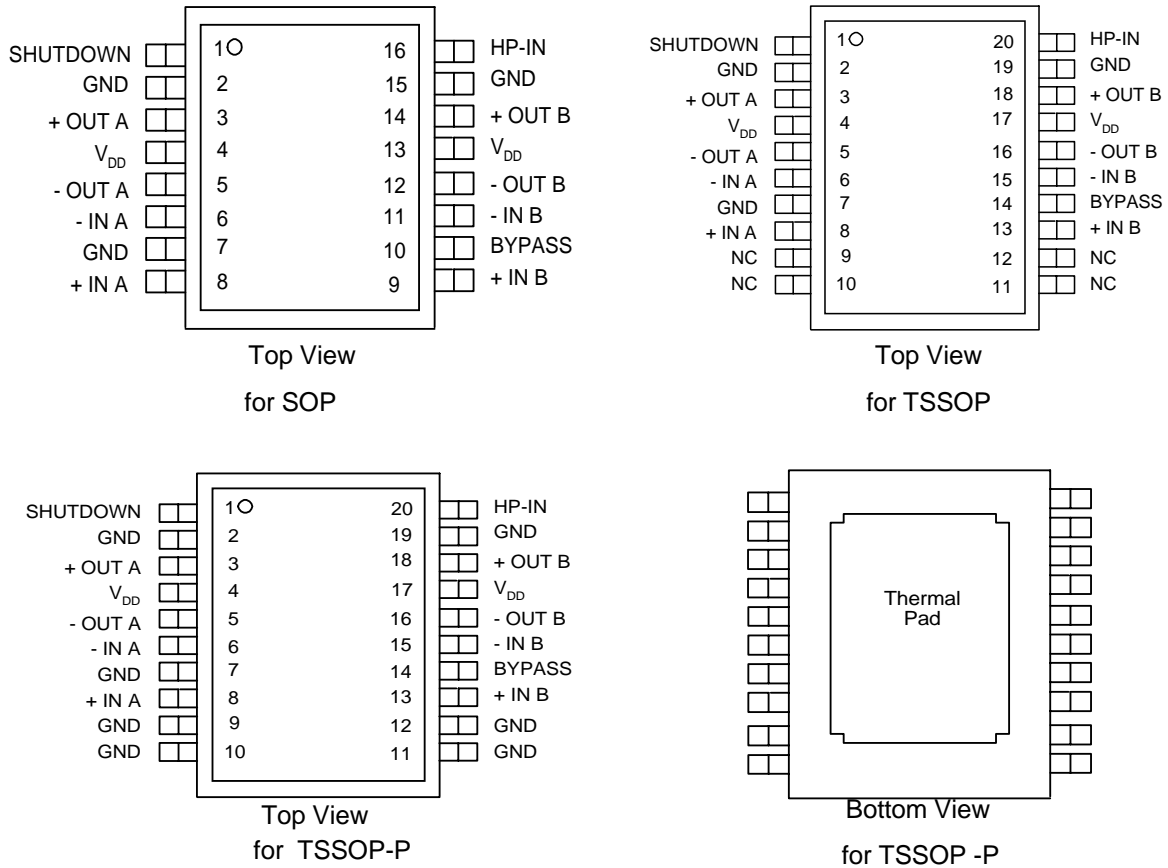
The following specifications apply for $V_{DD}=5V$ unless otherwise noted. Limits apply for $T_A=25^\circ C$

Symbol	Parameter	Test Conditions	APA4863	Unit
			Typ.	
V_{OS}	Output Offset Voltage	$V_{IN}=0V$	5	mV
P_O	Output Power	THD=0.5%, $f=1kHz$, $R_L=32\Omega$	90	mW
		THD=1%, $f=1kHz$, $R_L=8\Omega$	320	
		THD=10%, $f=1kHz$, $R_L=8\Omega$	400	
THD+N	Total Harmonic Distortion plus Noise	$A_V=-1$, $P_O=75mW$, $f=1kHz$, $R_L=32\Omega$	0.02	%
RSRR	Power Supply Rejection Ratio	$V_{RIPPLE}=200mV_{RMS}$, $f=1kHz$, $C_B=2.2\mu F$, $R_L=8\Omega$	49	dB
X_{TALK}	Channel Separation	$f=1kHz$, $C_B=2.2\mu F$, $P_O=32mW$, $R_L=32\Omega$	85	dB
SNR	Signal-to-Noise Ratio	$V_{DD}=5V$, $P_O=340mW$, $R_L=8\Omega$	95	dB

Truth Table for Logic Inputs

Shutdown	HP-IN	APA4863 Mode
Low	Low	Bridge -Tied
Low	High	Single-Ended
High	Low	APA4863 Shutdown
High	High	APA4863 Shutdown

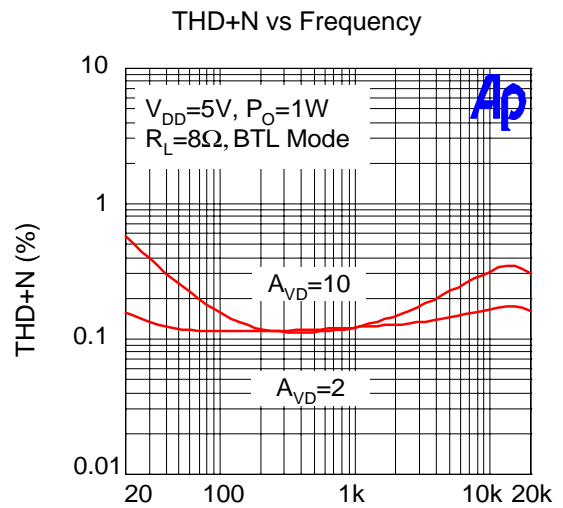
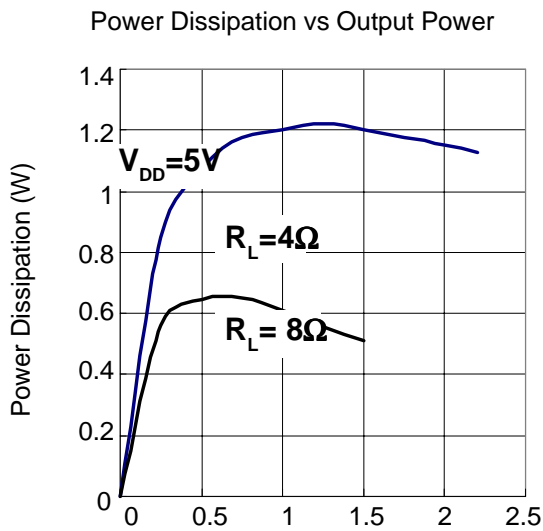
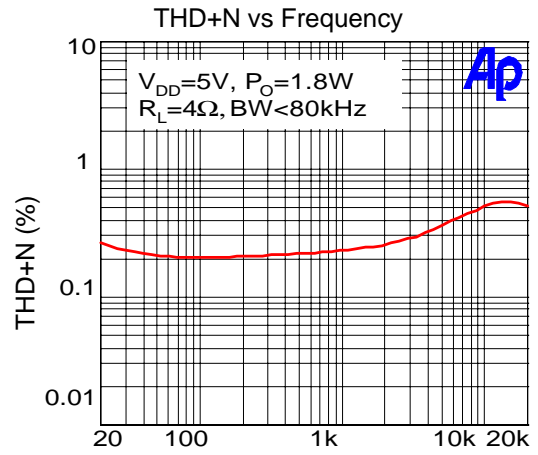
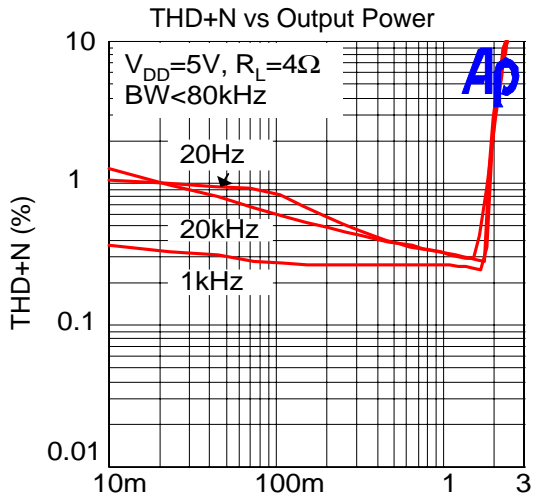
Pin Description



Pin Description

Name	I/O	Description
GND		Ground connection of circuitry
V _{DD}	I	Supply voltage input
+ INA	I	Non-inverting input of channel A, connected to bypass pin inside the IC
- INA	I	Input pin of channel A
+ OUT A	O	A channel + output in BTL mode, high impedance in SE mode
- OUT A	O	A channel - output in BTL mode, + output in SE mode
+ IN B	I	Non-inverting input of channel B, connected to bypass pin inside the IC
- IN B	I	Input pin of channel B
+ OUT B	O	B channel + output in BTL mode, high impedance in SE mode
- OUT B	O	B channel - output in BTL mode, + output in SE mode
BYPASS		Connect to voltage divider for internal mid-supply bias
HP-IN	I	Headphone control pin input, hold high for single-ended mode operation
SHUTDOWN	I	Shutdown mode control pin input, places entire IC in shutdown mode when held high, I _{DD} = 0.5μA

Typical Characteristics



Typical Characteristics Cont.

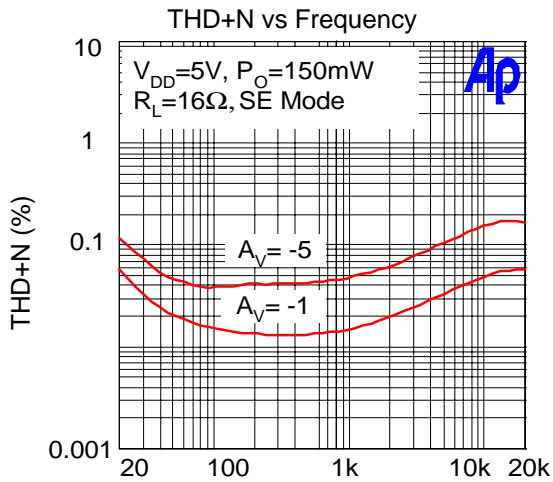


Figure 5 : Frequency (Hz)

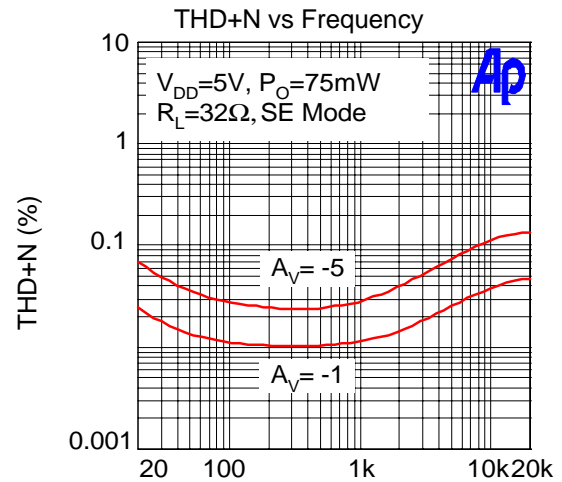


Figure 6 : Frequency (Hz)

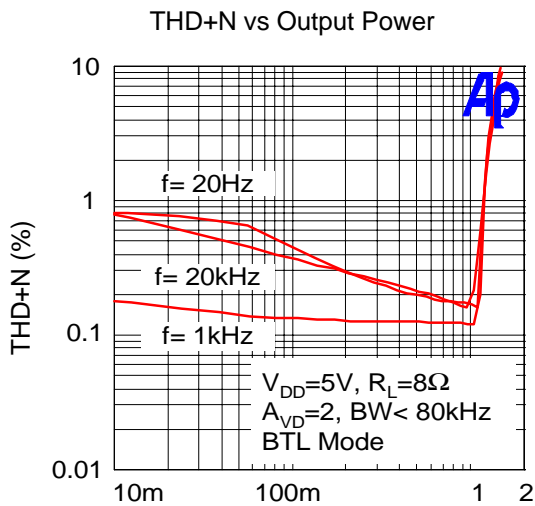


Figure 7 : Output Power (W)

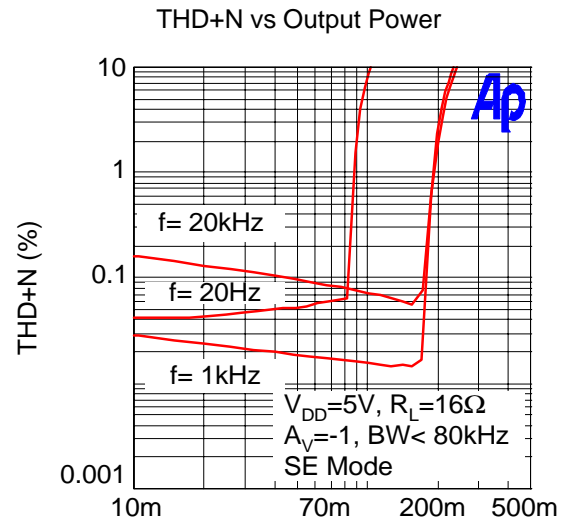


Figure 8 : Output Power (W)

Typical Characteristics Cont.

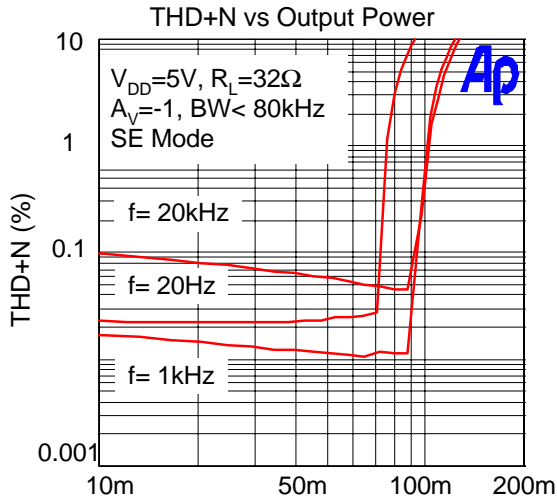


Figure 9 : Output Power (W)

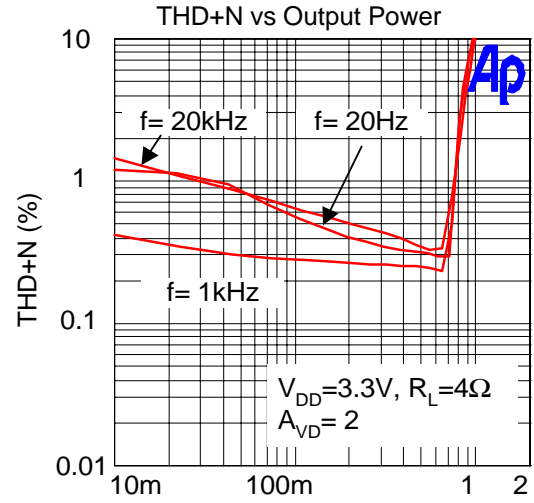


Figure 10 : Output Power (W)

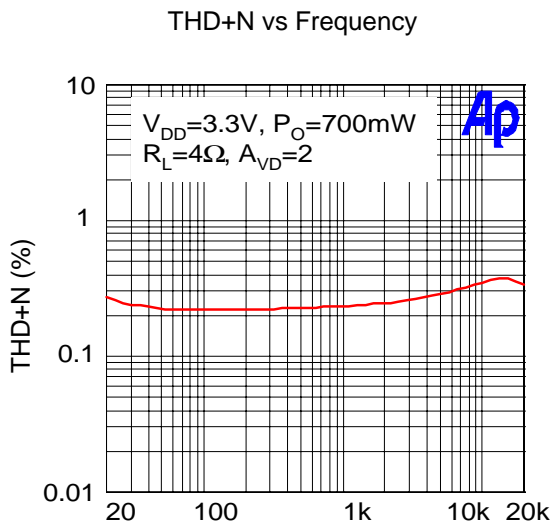


Figure 11 : Frequency (Hz)

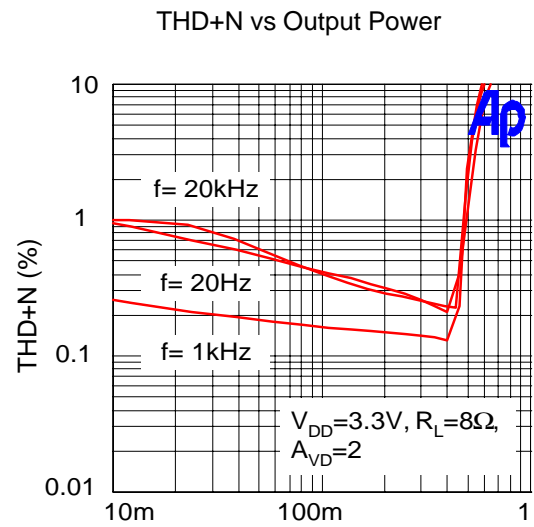


Figure 12 : Output Power (W)

Typical Characteristics Cont.

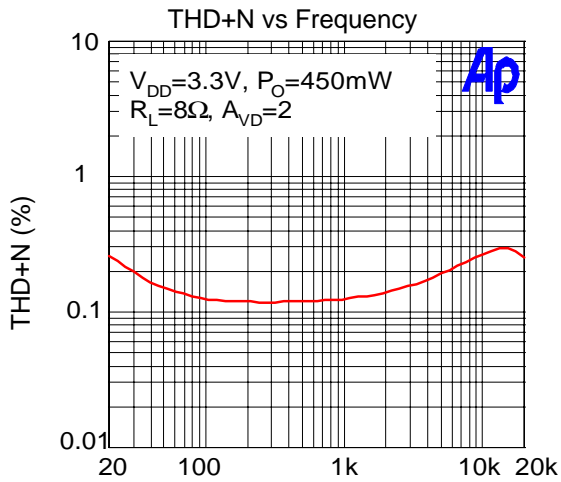


Figure 13 : Frequency (Hz)

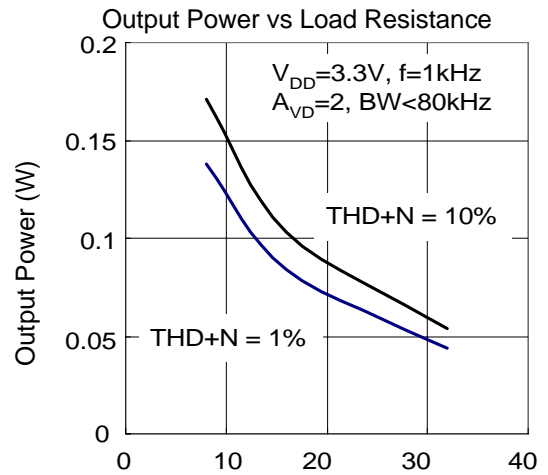


Figure 14 : Load Resistance (Ω)

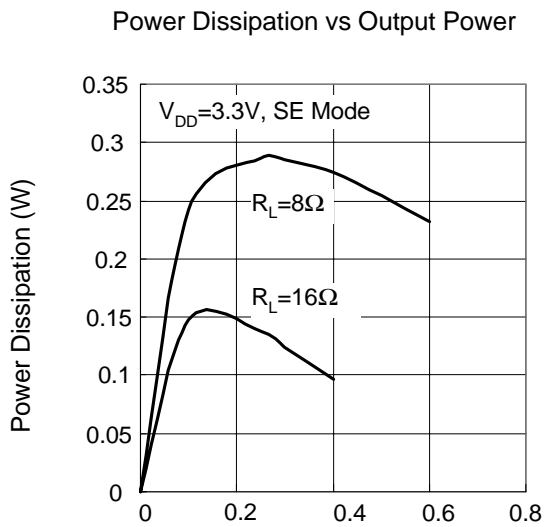


Figure 15 : Output Power (W)

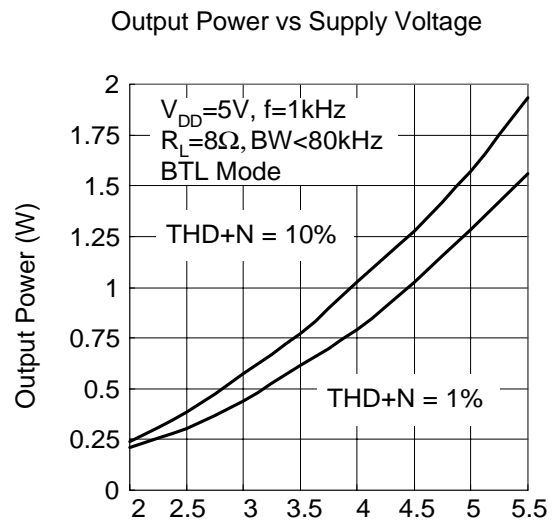


Figure 16 : Supply Voltage (V)

Typical Characteristics Cont.

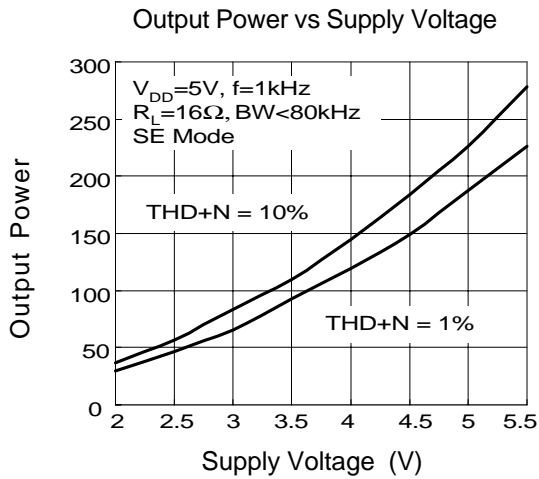


Figure 17

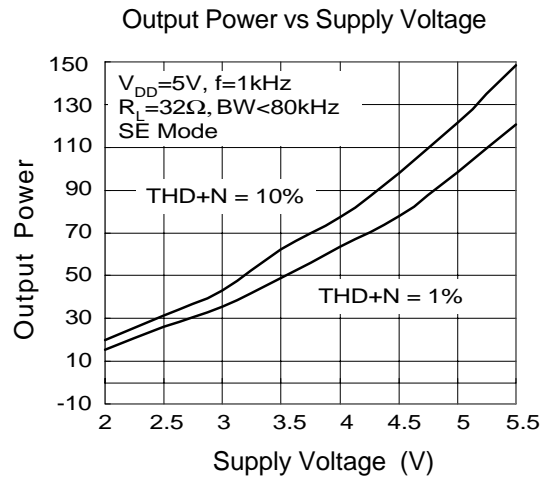


Figure 18

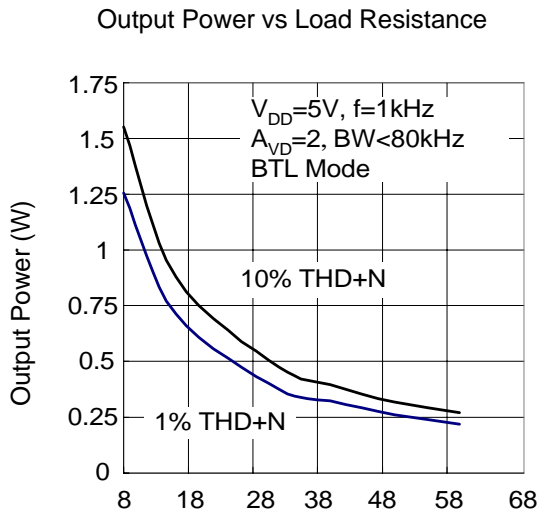


Figure 19 : Load Resistance (Ω)

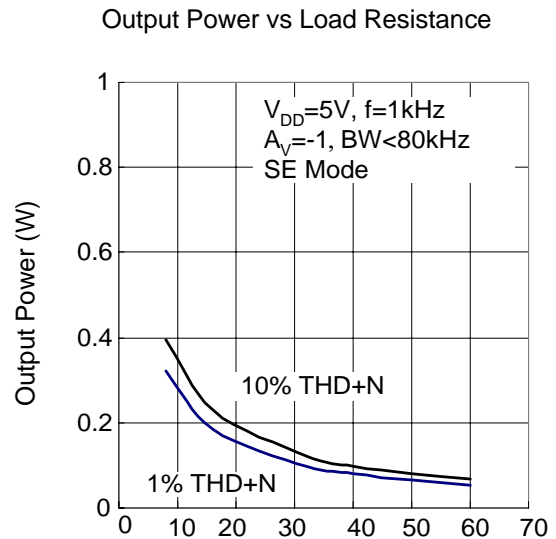


Figure 20 : Load Resistance (Ω)

Typical Characteristics Cont.

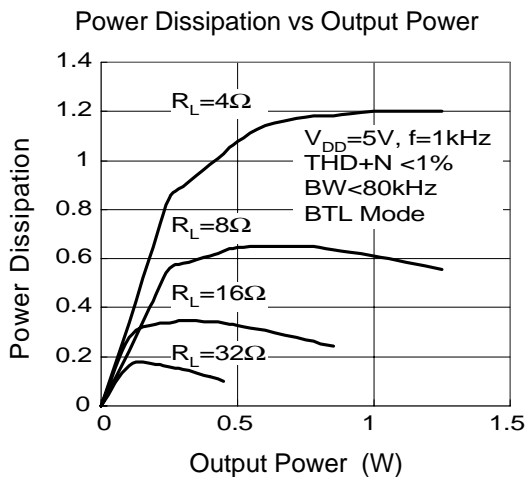


Figure 21

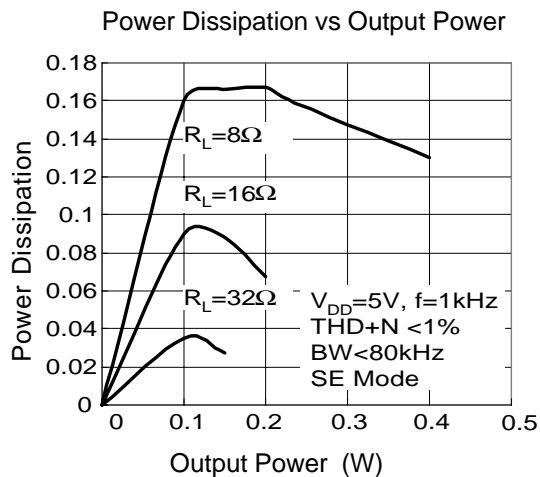


Figure 22

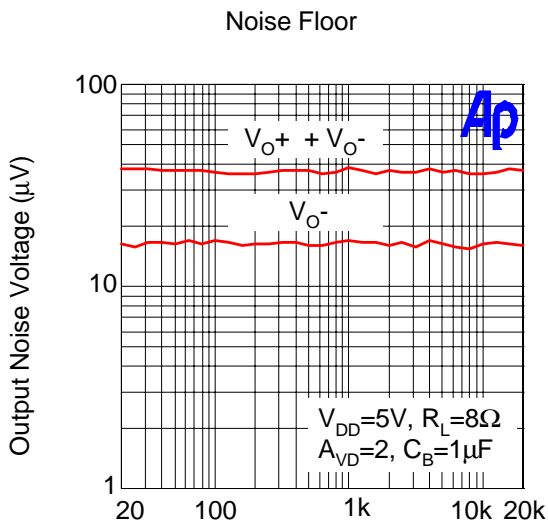


Figure 23 : Frequency (Hz)

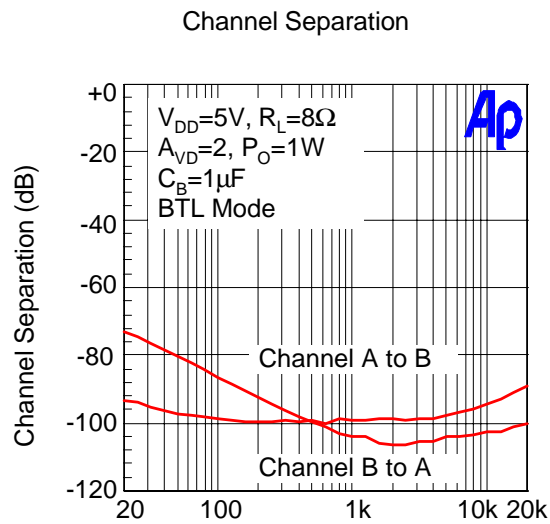


Figure 24 : Frequency (Hz)

Typical Characteristics Cont.

Channel Separation

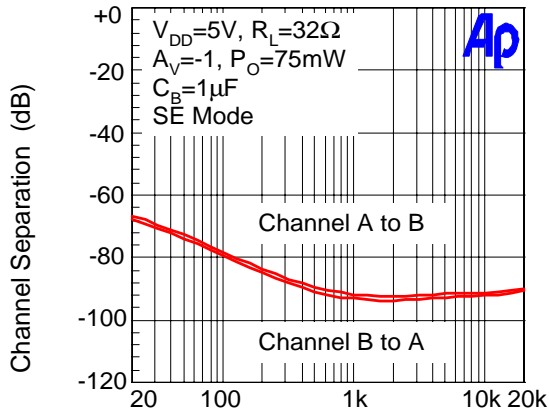


Figure 25 : Frequency (Hz)

Open Loop Frequency Response

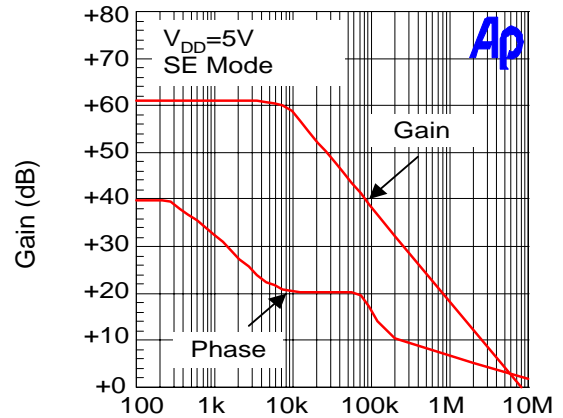


Figure 26 : Frequency (Hz)

Supply Current vs Supply Voltage

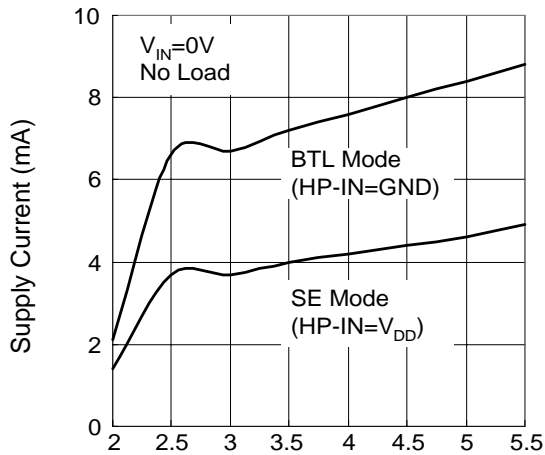
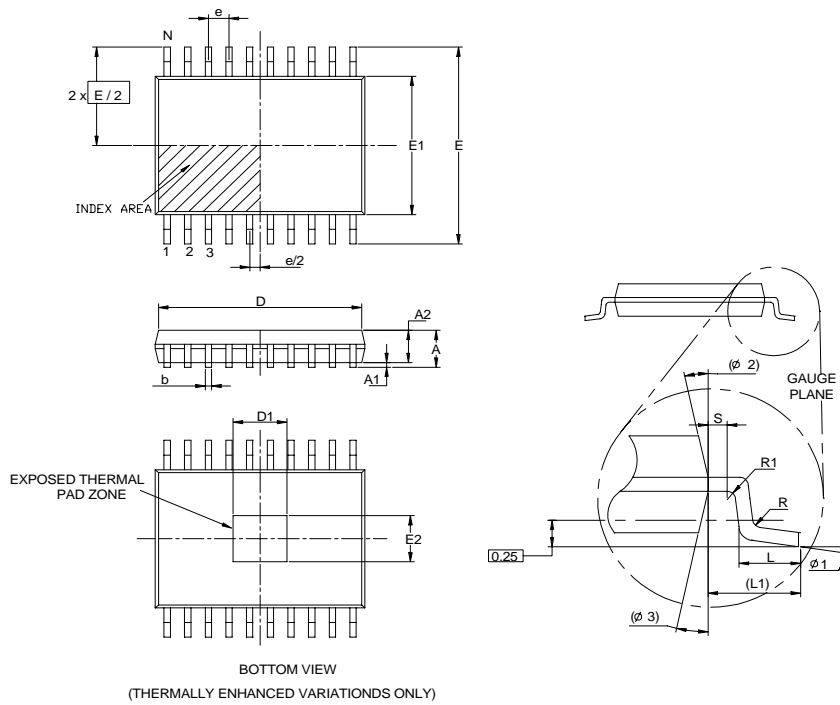


Figure 27 : Supply Voltage(V)

Packaging Information

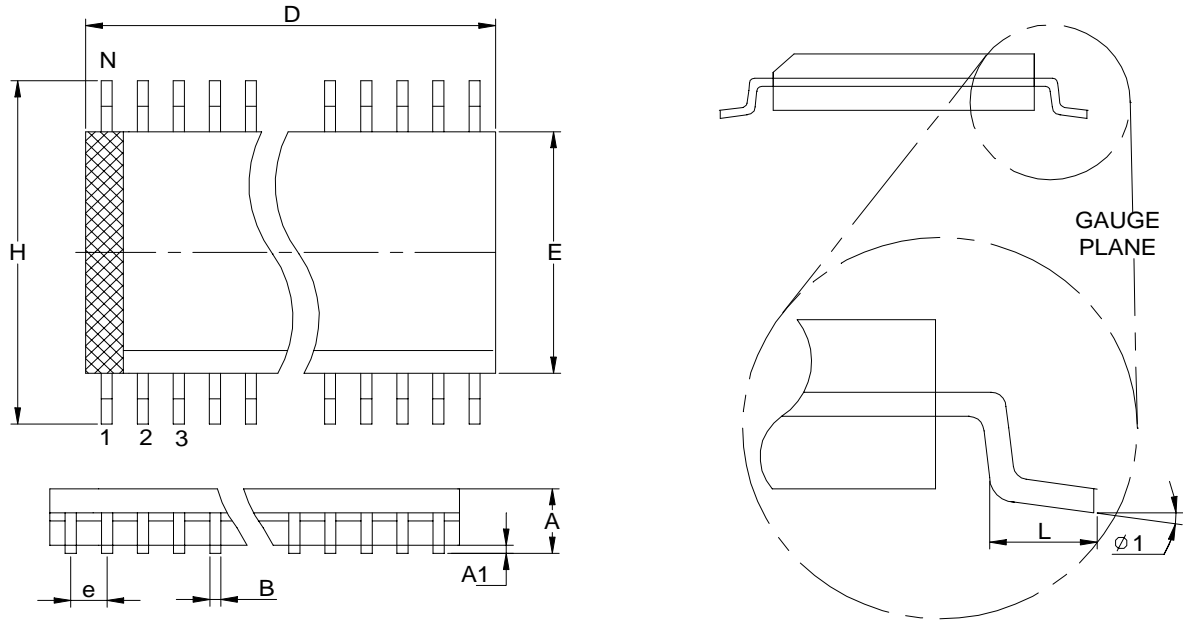
TSSOP/ TSSOP-P (Reference JEDEC Registration MO-153)



Dim	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A		1.2		0.047
A1	0.00	0.15	0.000	0.006
A2	0.80	1.05	0.031	0.041
D	6.4 (N=20PIN) 7.7 (N=24PIN)	6.6 (N=20PIN) 7.9 (N=24PIN)	0.252 (N=20PIN) 0.303 (N=24PIN)	0.260 (N=20PIN) 0.311 (N=24PIN)
D1	2.20 (N=20PIN) 2.70 (N=24PIN) Thermally Enhanced		0.087 (N=20PIN) 0.106 (N=24PIN) Thermally Enhanced	
e	0.65 BSC		0.026 BSC	
E	6.40 BSC		0.252 BSC	
E1	4.30	4.50	0.169	0.177
E2	1.50		0.059	
L	0.45	0.75	0.018	0.030
L1	1.0 REF		0.039REF	
R	0.09		0.004	
R1	0.09		0.004	
S	0.2		0.008	
phi 1	0°	8°	0°	8°
phi 2	12° REF		12° REF	
phi 3	12° REF		12° REF	

Packaging Information

SO – 300mil (Reference JEDEC Registration MS-013)



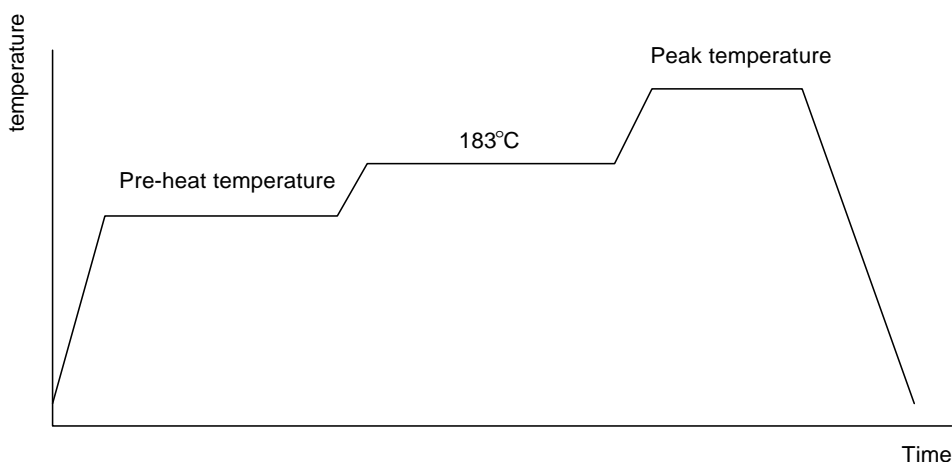
Dim	Millimeters		Variations- D			Dim	Inches		Variations- D		
	Min.	Max.	Variations	Min.	Max.		Min.	Max.	Variations	Min.	Max.
A	2.35	2.65	SO-16	10.10	10.50	A	0.093	0.1043	SO-16	0.398	0.413
A1	0.10	0.30	SO-18	11.35	11.76	A1	0.004	0.0120	SO-18	0.447	0.463
B	0.33	0.51	SO-20	12.60	13	B	0.013	0.020	SO-20	0.496	0.512
D	See variations		SO-24	15.20	15.60	D	See variations		SO-24	0.599	0.614
E	7.40	7.60	SO-28	17.70	18.11	E	0.2914	0.2992	SO-28	0.697	0.713
e	1.27BSC		SO-14	8.80	9.20	e	0.050BSC		SO-14	0.347	0.362
H	10	10.65				H	0.394	0.419			
L	0.40	1.27				L	0.016	0.050			
N	See variations					N	See variations				
φ 1	0°	8°				φ 1	0°	8°			

Physical Specifications

Terminal Material	Solder-Plated Copper (Solder Material : 90/10 or 63/37 SnPb)
Lead Solderability	Meets EIA Specification RSI86-91, ANSI/J-STD-002 Category 3.
Packaging	2000 devices per reel

Reflow Condition (IR/Convection or VPR Reflow)

Reference JEDEC Standard J-STD-020A APRIL 1999



Classification Reflow Profiles

	Convection or IR/ Convection	VPR
Average ramp-up rate(183°C to Peak)	3°C/second max.	10 °C /second max.
Preheat temperature 125 ± 25°C)	120 seconds max	
Temperature maintained above 183°C	60 – 150 seconds	
Time within 5°C of actual peak temperature	10 –20 seconds	60 seconds
Peak temperature range	220 +5/-0°C or 235 +5/-0°C	215-219°C or 235 +5/-0°C
Ramp-down rate	6 °C /second max.	10 °C /second max.
Time 25°C to peak temperature	6 minutes max.	

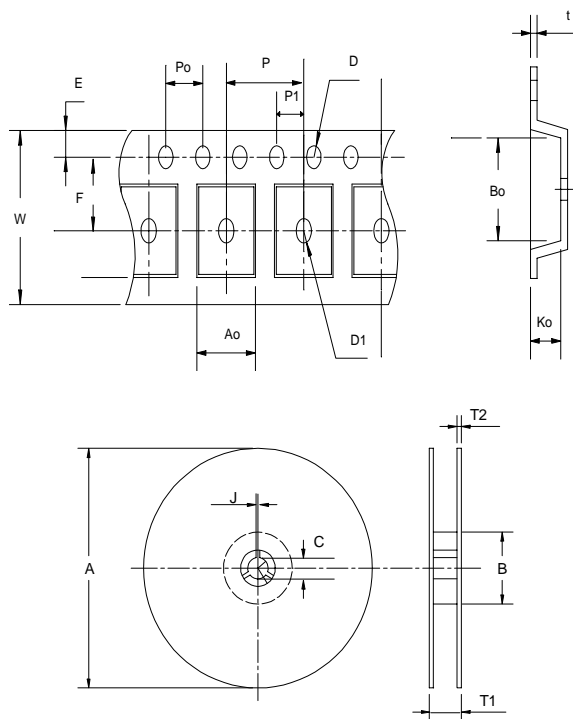
Package Reflow Conditions

pkg. thickness ≥ 2.5mm and all bgas	pkg. thickness < 2.5mm and pkg. volume ≥ 350 mm ³	pkg. thickness < 2.5mm and pkg. volume < 350mm ³
Convection 220 +5/-0 °C		Convection 235 +5/-0 °C
VPR 215-219 °C		VPR 235 +5/-0 °C
IR/Convection 220 +5/-0 °C		IR/Convection 235 +5/-0 °C

Reliability test program

Test item	Method	Description
SOLDERABILITY	MIL-STD-883D-2003	245°C , 5 SEC
HOLT	MIL-STD-883D-1005.7	1000 Hrs Bias @ 125 °C
PCT	JESD-22-B, A102	168 Hrs, 100 % RH , 121°C
TST	MIL-STD-883D-1011.9	-65°C ~ 150°C, 200 Cycles
ESD	MIL-STD-883D-3015.7	VHBM > 2KV, VMM > 200V
Latch-Up	JESD 78	10ms , I _{tr} > 100mA

Carrier Tape & Reel Dimensions



Application	A	B	C	J	T1	T2	W	P	E
SOP-16W	330±3	100 ± 2	13 + 0.5	2 ± 0.5	16.4 +0.3 -0.2	2.5± 0.5	16 ± 0.2	12± 0.1	1.75± 0.1
Application	F	D	D1	Po	P1	Ao	Bo	Ko	t
SOP-16W	7.5 ± 0.1	1.5 +0.1	1.5 +0.25	4.0 ± 0.1	2.0 ± 0.1	10.9 ± 0.1	10.8± 0.1	3.0± 0.1	0.3±0.013

(mm)

Cover Tape Dimensions

Carrier Width	16
Cover Tape Width	13.3

(mm)

Customer Service

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