Advanced PWM and Linear Power Control

Features

- 2 Regulated Voltage are provided
  - – Switching Power for Fixed Voltage (1.25V / 2.05V) or Adjustable Voltage
  - – Linear Regulator for FBVDDQ(2.5V)
- Simple Single-Loop Control Design
  - – Voltage-Mode PWM Control
- Excellent Output Voltage Regulation
  - – PWM Output : ±1%
  - – Linear Output : ±3%
- Fast Transient Response
  - – High-Bandwidth Error Amplifier
  - – Full 0% to 100% Duty Ratio
- Power-Good Output Voltage Monitor
- Over-Voltage and Over-Current Fault Monitors
- Small Converter Size
  - – Constant Frequency Operation(200kHz)
  - – Reduce External Component Count

Applications

- Motherboard Power Regulation for Computers
- Low-Voltage Distributed Power Supplies
- VGA Card Power Regulation
- Termination Voltage

General Description

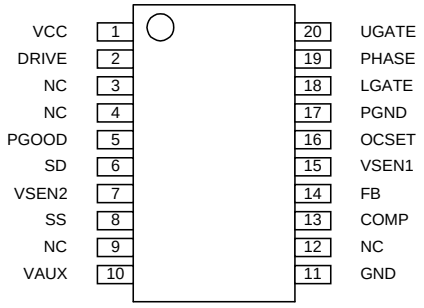
The APW7035 integrates PWM controller and linear controller , as well as the monitoring and protection functions into a single package , which provides two controlled power outputs with over-voltage and over-current protections. The PWM controller regulates the DDR reference voltage (1.25V) or GPU Voltage (2.05V) with a synchronous-rectified buck converter. The linear controller regulates power for Memory Voltage.

The precision reference and voltage-mode PWM control provide ±1% static regulation. The linear controller drives an external N-channel MOSFET to provide adjustable voltage.

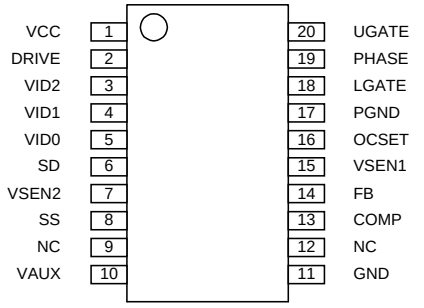
The APW7035 monitors all the output voltages , and a single Power Good signal is issued when the PWM Voltage is within ±10% of the DAC setting and the Linear regulator output levels are above their under-voltage thresholds. Additional built-in over-voltage protection for the PWM output uses the lower MOSFET to prevent output voltages above 115% of the DAC setting. The PWM over-current function monitors the output current by using the voltage drop across the upper MOSFET's $R_{DS(ON)}$, eliminating the need for a current sensing resistor.

The APW7035A/B/C/D support a TTL 3-input Digital to Analog converter that adjusts the synchronous-rectified buck converter output from 1.00V to 3.20V , referenc to Table1.

Pin Description



APW7035-12/19



APW7035A/B/C/D

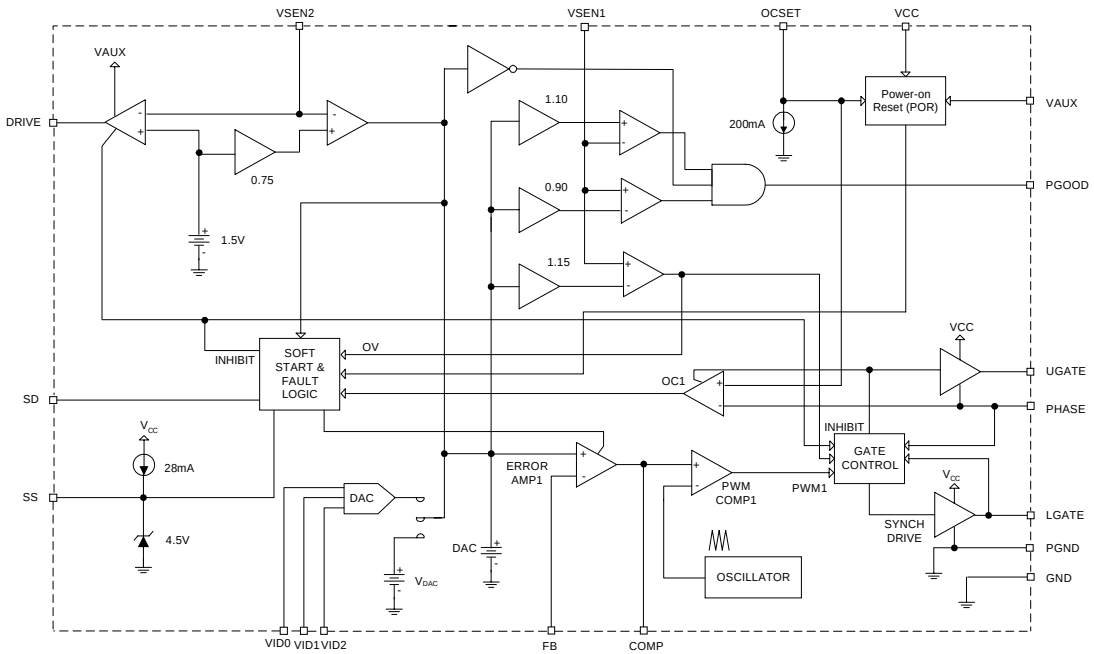
Ordering Information

APW7035 □□ □□-□□

- Handling Code
- Temp. Range
- Package Code
- Voltage Code

Voltage Code
12 : 1.25V 20 : 2.05V A : 1.00V~1.35V
B : 1.40V~1.75V C : 1.80V~2.40V D : 2.50V~3.20V
Package Code
K : SOP
Temp. Range
C : 0 to 70 °C
Handling Code
TU : Tube TR : Tape & Reel

Block Diagram



Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{CC}	Supply Voltage	15	V
V_I , V_O	Input , Output or I/O Voltage	GND -0.3 V to V_{CC} +0.3	V
T_A	Operating Ambient Temperature Range	0 to 70	°C
T_J	Junction Temperature Range	0 to 125	°C
T_{STG}	Storage Temperature Range	-65 to +150	°C
T_S	Soldering Temperature	300 ,10 seconds	°C

Thermal Characteristics

Symbol	Parameter	Value	Unit
$R_{\theta JA}$	Thermal Resistance in Free Air SOIC SOIC (with 3in^2 of Copper)	 75 65	°C/W

Electrical Characteristics

(Recommended operating conditions , Unless otherwise noted) Refer to Block and Simplified Power System Diagrams , and Typical Application Schematic.

Symbol	Parameter	Test Conditions	APW7035			Unit
			Min.	Typ.	Max.	
V_{CC} Supply Current						
I_{CC}	Nominal Supply Current	UGATE, LGATE, DRIVE open		9		mA
Power-on Reset						
	Rising VCC Threshold	Vocset=4.5V			10.7	V
	Falling VCC Threshold	Vocset=4.5V	8.2			V
	Rising VAUX Threshold	Vocset=4.5V		2.5		V
	VAUX Threshold Hysteresis	Vocset=4.5V		0.5		V
	Rising V_{OCSET} Threshold			1.26		V
Oscillator						
F_{OCS}	Free Running Frequency	RT= Open	185	200	215	kHz
ΔV_{OSC}	Ramp Amplitude	RT= Open		1.9		V_{P-P}

Electrical Characteristics Cont.

(Recommended operating conditions , Unless otherwise noted) Refer to Block and Simplified Power System Diagrams , and Typical Application Schematic.

Symbol	Parameter	Test Conditions	APW7035			Unit
			Min.	Typ.	Max.	
DAC and Bandgap Reference						
V_{DAC}	DACOUT Voltage accuracy		-1.0		+1.0	%
V_{BG}	Bandgap Reference Voltage			1.265		V
	Bandgap Reference Tolerance		-2.5		+2.5	%
Linear Regulators						
	Regulation			3		%
	Output Drive Current	VAUX-V_{DRIVE} >0.6V	20	40		mA
Synchronous PWM Controller Error Amplifier						
	DC Gain			88		dB
GBWP	Gain-Bandwidth Product			15		MHz
SR	Slew Rate	COMP=10pF		6		V/μs
PWM Controller Gate Driver						
I_{UGATE}	UGATE Source	V_{CC}=12V, V_{UGATE} =6V		1		A
R_{UGATE}	UGATE Sink	$V_{UGATE1-PHASE}$ =1V			3.5	Ω
I_{LGATE}	LGATE Source	V_{CC}=12V, V_{LGATE} =1V		1		A
R_{LGATE}	LGATE Sink	V_{LGATE}= 1V			3	Ω
Protection						
	VSEN1 Over-Voltage	VSEN1 Rising		115	120	%
Protection						
I_{OCSET}	OCSET Current Source	V_{OCSET}= 4.5V_{DC}	170	200	230	μA
I_{SS}	Soft Start Current			28		μA
Power Good						
	VSEN1 Upper Threshold	VSEN1 Rising		109		%
	VSEN1 Under Voltage	VSEN1 Rising		93		%
	VSEN1 Hysteresis	Upper /Lower Threshold		2		%
V_{PGOOD}	PGOOD Voltage Low	I_{PGOOD}= -4mA			0.8	V

Functional Pin Description

VCC (Pin 1)

Provide a 12V bias supply for the IC to this pin. This pin also provides the gate bias charge for all the MOSFETs controlled by the IC. The voltage at this pin is monitored for Power-On Reset (POR) purposes.

DRIVE (Pin 2)

Connect this pin to the gate of an external MOSFET. This pin provides the drive for the FBVDDQ regulator's pass transistor.

Functional Pin Description cont.

NC (Pin 3, Pin 4 and Pin 5)

No Connect. (APW7035-12,19)

PGOOD (Pin 5)

PGOOD is an open drain output used to indicate the status of the output voltages. This pin is pulled low when the synchronous regulator output is not within ±10% of the DAC reference voltage or Linear regulator outputs are below under-voltage thresholds. (APW7035-A,B,C,D)

VID2 , VID1 , VID0 (Pin 3,4 and 5)

VID0-2 are the TTL-compatible input pins to the 3-bit DAC. The logic states of these three pins program the internal voltage reference (DAC). The level of DAC sets the microprocessor core converter output voltage , as well as the corresponding PGOOD and OVP thresholds. (APW7035-A,B,C,D)

SD (Pin 6)

The pin shuts down all the outputs. A TLL-compatible , logic lebel high signal applied at this pin immediately discharges the soft-start capacitor , disbling all the output.

VSEN2 (Pin 7)

Connect this pin to a resistor divider to set the linear regulator (FBVDDQ) output voltage.

SS (Pin 8)

Connect a capacitor from this pin to ground. This capacitor , along with an internal 28µA current source , sets the soft-start interval of the converter.

NC (Pin 9 and Pin12)

No Connection.

VAUX (Pin 10)

This pin provides boost current for the linear regulator's output drives in the event bipolar NPN transistors (instead of N-channel MOSFETs) are employed as pass elements. The voltage at this pin is monitored for power-on reset purposes.

GND (Pin 11)

Signal ground for the IC. All voltage levels are measured with respect to this pin.

FB and COMP (Pin 13, and 14)

COMP and FB are the available external pins of the PWM converter error amplifier. The FB pin is the inverting input of the error amplifier. Similarly , the COMP pin is the error amplifier output. These pins are used to compensate the voltage-mode control feedback loop of the synchronous PWM converter.

VSEN1 (Pin 15)

This pin is connected to the PWM converter's output voltage. The PGOOD and OVP comparator circuits use this signal to report output voltage status and for over- voltage protection.

OCSET (Pin 16)

Connect a resistor from this pin to the drain of the respective upper MOSFET. This resistor , an internal 200µA current source , and the upper MOSFET's on-resistance set the converter over-current trip point. An over-current trip cycles the soft-start function. The voltage at this pin is monitored for power-on reset (POR) purposes and pulling this pin low with an open drain device will shutdown the IC.

PGND (Pin 17)

This is the power ground connection. Tie the synchronous PWM converter's lower MOSFET source to this pin.

LGATE (Pin 18)

Connect LGATE to the PWM converter's lower MOSFET gate. This pin provides the gate drive for the lower MOSFET.

Functional Pin Description cont.

PHASE (Pin 19)

Connect the PHASE pin to the PWM converter's upper MOSFET source. This pin represents the gate drive return current path and is used to monitor the voltage drop across the upper MOSFET for over-current protection.

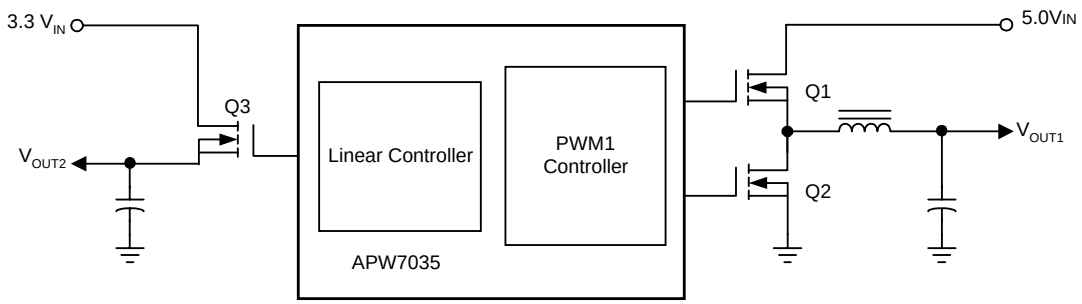
UGATE (Pin 20)

Connect UGATE pin to the PWM converter's upper MOSFET gate. This pin provides the gate drive for the upper MOSFET.

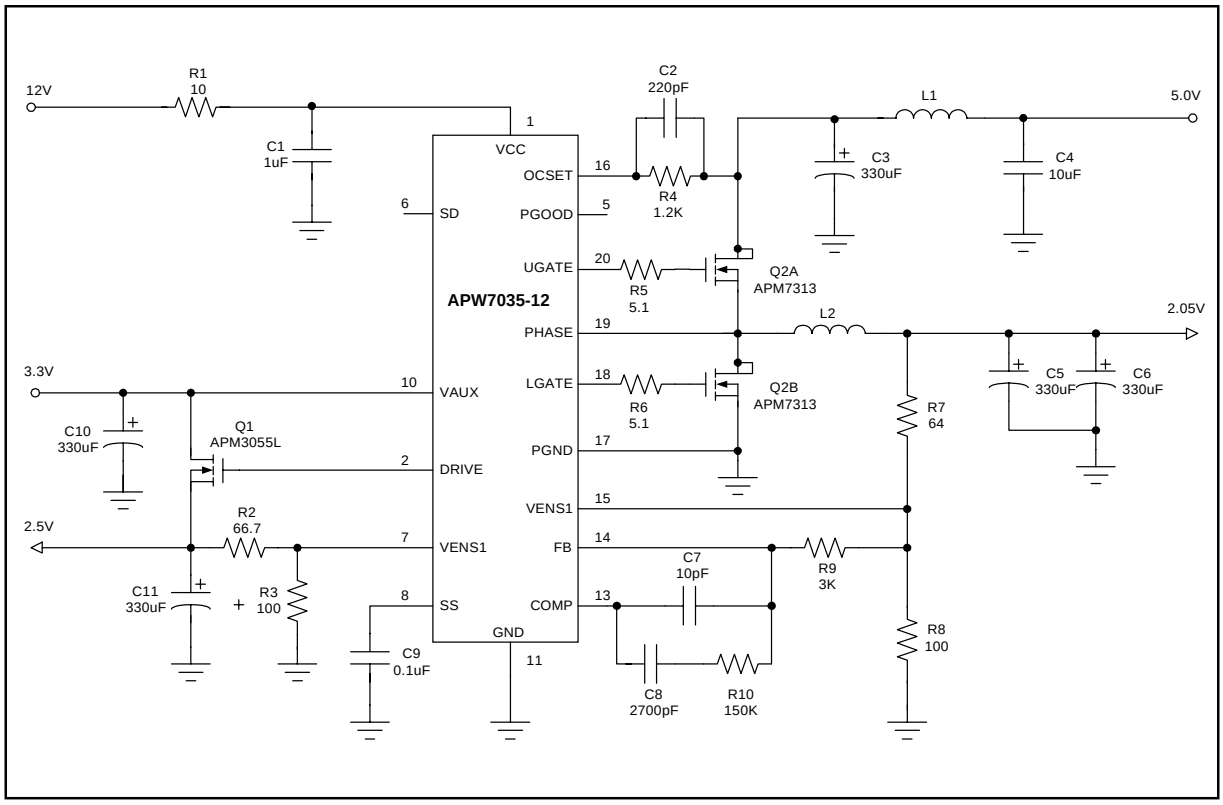
Table1 Output Voltage Program

VID2	VID1	VID0	APW7035-A	VID2	VID1	VID0	APW7035-B
0	0	0	1.35V	0	0	0	1.75V
0	0	1	1.30V	0	0	1	1.70V
0	1	0	1.25V	0	1	0	1.65V
0	1	1	1.20V	0	1	1	1.60V
1	0	0	1.15V	1	0	0	1.55V
1	0	1	1.10V	1	0	1	1.50V
1	1	0	1.05V	1	1	0	1.45V
1	1	1	1.00V	1	1	1	1.40V
VID2	**VID1**	**VID0**	**APW7035-C**	**VID2**	**VID1**	**VID0**	**APW7035-D**
0	0	0	2.40V	0	0	0	3.20V
0	0	1	2.30V	0	0	1	3.10V
0	1	0	2.20V	0	1	0	3.00V
0	1	1	2.10V	0	1	1	2.90V
1	0	0	2.00V	1	0	0	2.80V
1	0	1	1.90V	1	0	1	2.70V
1	1	0	1.80V	1	1	0	2.60V
1	1	1	0	1	1	1	2.50V

Simplified Power System Diagram

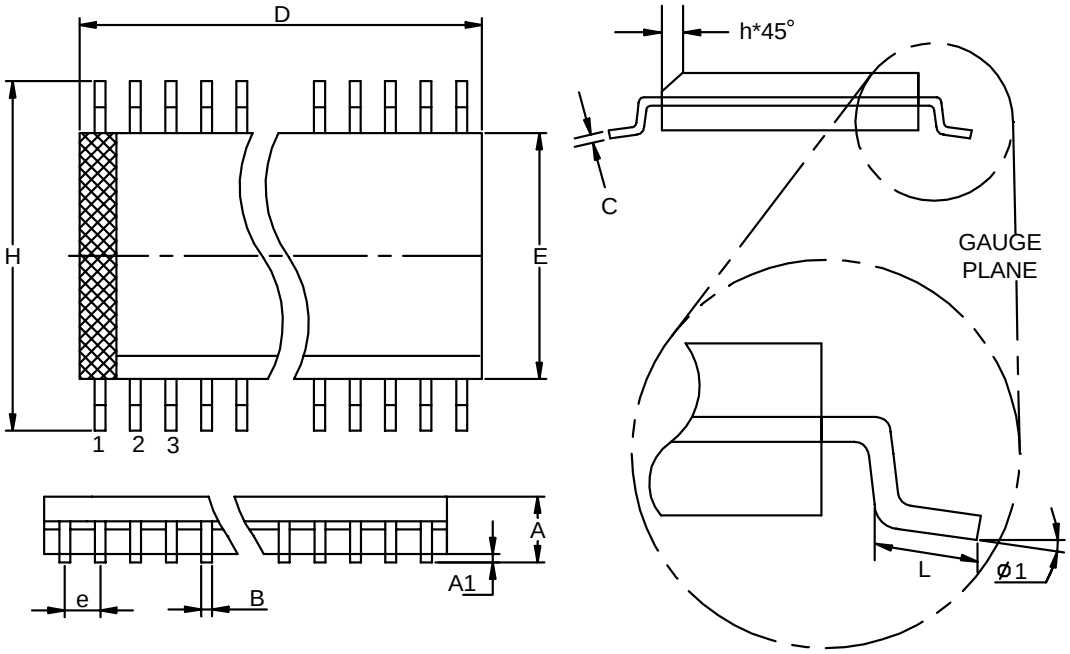


Typical Application Circuit



Package Information

SO – 300mil (Reference JEDEC Registration MS-013)



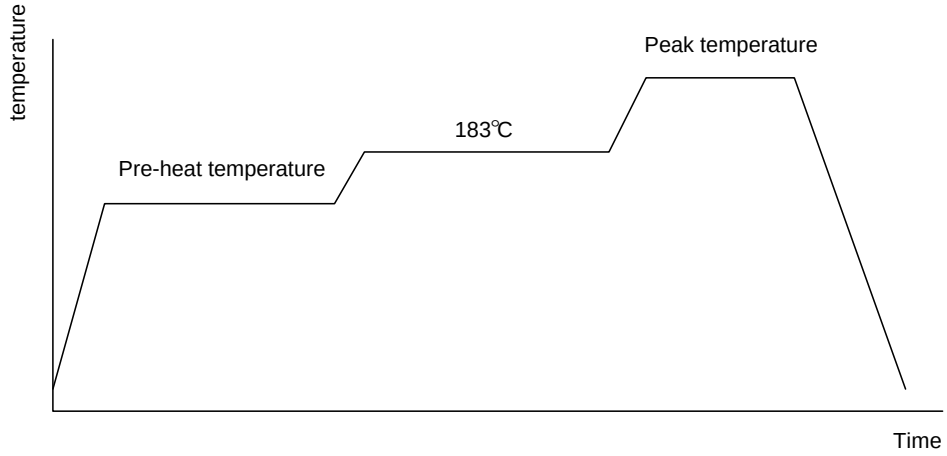
Dim	Millimeters		Variations			Dim	Inches		Variations		
	Min.	Max.	Variations	Min.	Max.		Min.	Max.	Variations	Min.	Max.
A	2.35	2.65	SO-20	12.60	13.0	A	0.093	0.1043	SO-20	0.496	0.512
A1	0.10	0.30	SO-24	15.20	15.60	A1	0.004	0.0120	SO-24	0.599	0.614
B	0.33	0.51	SO-28	17.70	18.11	B	0.013	0.020	SO-28	0.697	0.713
C	0.23	0.32				C	0.0091	0.0125			
D	See variations					D	See variations				
E	7.40	7.60				E	0.2914	0.299			
e	1.27BSC					e	0.050BSC				
H	10	10.65				H	0.394	0.419			
h	0.25	0.75				h	0.010	0.029			
L	0.40	1.27				L	0.016	0.050			
ϕ 1	0°	8°				ϕ 1	0°	8°			

Physical Specifications

Terminal Material	Solder-Plated Copper (Solder Material : 90/10 or 63/37 SnPb)
Lead Solderability	Meets EIA Specification RSI86-91, ANSI/J-STD-002 Category 3.
Packaging	1000 devices per reel

Refolw Condition (IR/ Convection or VPR Reflow)

Reference JEDEC Standard J-STD-020A APRIL 1999



Classification Reflow Profiles

	Convection or IR/ Convection	VPR
Average ramp-up rate(183°C to Peak)	3°C/second max.	10 °C /second max.
Preheat temperature 125 ± 25°C)	120 seconds max.	
Temperature maintained above 183°C	60 ~ 150 seconds	
Time within 5°C of actual peak temperature	10 ~ 20 seconds	60 seconds
Peak temperature range	220 +5/-0°C or 235 +5/-0°C	215~ 219°C or 235 +5/-0°C
Ramp-down rate	6 °C /second max.	10 °C /second max.
Time 25°C to peak temperature	6 minutes max.	

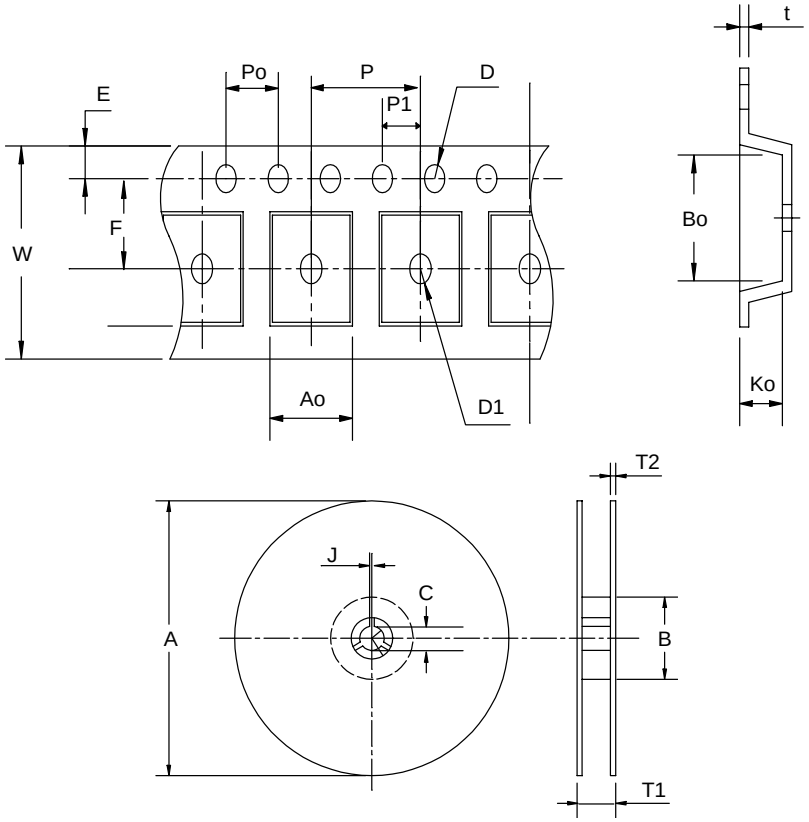
Package Reflow Conditions

pkg. thickness ≥ 2.5mm and all bags	**pkg. thickness < 2.5mm and pkg. volume ≥ 350 mm³**	**pkg. thickness < 2.5mm and pkg. volume < 350mm³**
Convection 220 +5/-0 °C		Convection 235 +5/-0 °C
VPR 215-219 °C		VPR 235 +5/-0 °C
IR/Convection 220 +5/-0 °C		IR/Convection 235 +5/-0 °C

Reliability test program

Test item	Method	Description
SOLDERABILITY	MIL-STD-883D-2003	245°C , 5 SEC
HOLT	MIL-STD-883D-1005.7	1000 Hrs Bias @ 125 °C
PCT	JESD-22-B, A102	168 Hrs, 100 % RH , 121°C
TST	MIL-STD-883D-1011.9	-65°C ~ 150°C, 200 Cycles
ESD	MIL-STD-883D-3015.7	VHBM > 2KV, VMM > 200V
Latch-Up	JESD 78	10ms , I_{tr} > 100mA

Tape & Reel Dimensions



Application	A	B	C	J	T1	T2	W	P	E
SOP-20	330±1	62 ± 1.5	12.75 ±0.15	2 + 0.6	24.4 +0.2	2± 0.2	24 + 0.3 - 0.1	12± 0.1	1.75± 0.1
Application	F	D	D1	Po	P1	Ao	Bo	Ko	t
SOP-20	11.5 ± 0.1	1.5+0.1	1.5+0.25	4.0 ± 0.1	2.0 ± 0.1	8.2 ± 0.1	13± 0.1	2.5± 0.1	0.35±0.013

(mm)

Cover Tape Dimensions

Carrier Width	24
Cover Tape Width	21.3

(mm)

Customer Service

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