Advanced PWM and Dual Linear Power Control

Features

- 3 Regulated Voltage are provided
  - Switching Power for VTT(1.25V)
  - Linear1 Regulator for FBVDDQ(2.5V)
  - Linear2 Regulator for NVVDD(2.05V)
- Simple Single-Loop Control Design
  - Voltage-Mode PWM Control
- Excellent Output Voltage Regulation
  - PWM Output: ±2% Full Temperature
  - Linear Output: ±3% Full Temperature
- Fast Transient Response
  - High-Bandwidth Error Amplifier
  - Full 0% to 100% Duty Ratio
- TTL-Compatible 3-Bit Digital-to-Analog Output Voltage Selection
  - 0.05V Steps from $1.3V_{DC}$ to $1.65V_{DC}$
- Power-Good Output Voltage Monitor
- Over-Voltage and Over-Current Fault
- Monitors Small Converter Size
  - Constant Frequency Operation(200kHz)
  - Programmable Oscillator from 50kHz to 1MHz
  - Reduce External Component Count

Applications

- Motherboard Power Regulation for Computers
  - Low-Voltage Distributed Power Supplies
  - VGA Card Power Regulation

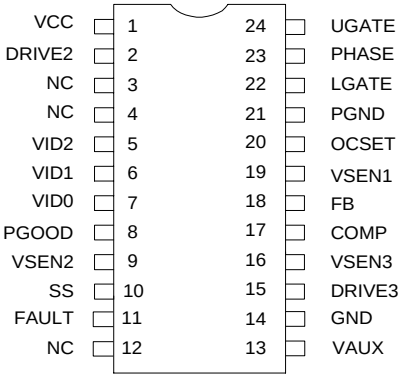
General Description

The APW7015 integrates a PWM controller and Dual linear controller, as well as the monitoring and protection functions into a single package, which provides three controlled power outputs with over-voltage and over-current protections. The PWM controller regulates the DDR reference voltage with a synchronous-rectified buck converter. The linear controller regulates power for microprocessor core voltage and Memory Voltage.

TTL Compatible 3-bit digital-to-analog converter (DAC) that adjusts the output voltage from $1.3V_{DC}$ to $1.65V_{DC}$ in 0.05V steps is included in APW7015. The precision reference and voltage-mode PWM control provide ±2% static regulation. The linear controller drives an external N-channel MOSFET to provide adjustable voltage.

The APW7015 monitors all the output voltages, and a single Power Good signal is issued when the PWM Voltage is within 10% of the DAC setting and the other output levels are above their under-voltage thresholds. Additional built-in over-voltage protection for the PWM output uses the lower MOSFET to prevent output voltages above 115% of the DAC setting. The PWM over-current function monitors the output current by using the voltage drop across the upper MOSFET's $R_{DS(ON)}$,eliminating the need for a current sensing resistor.

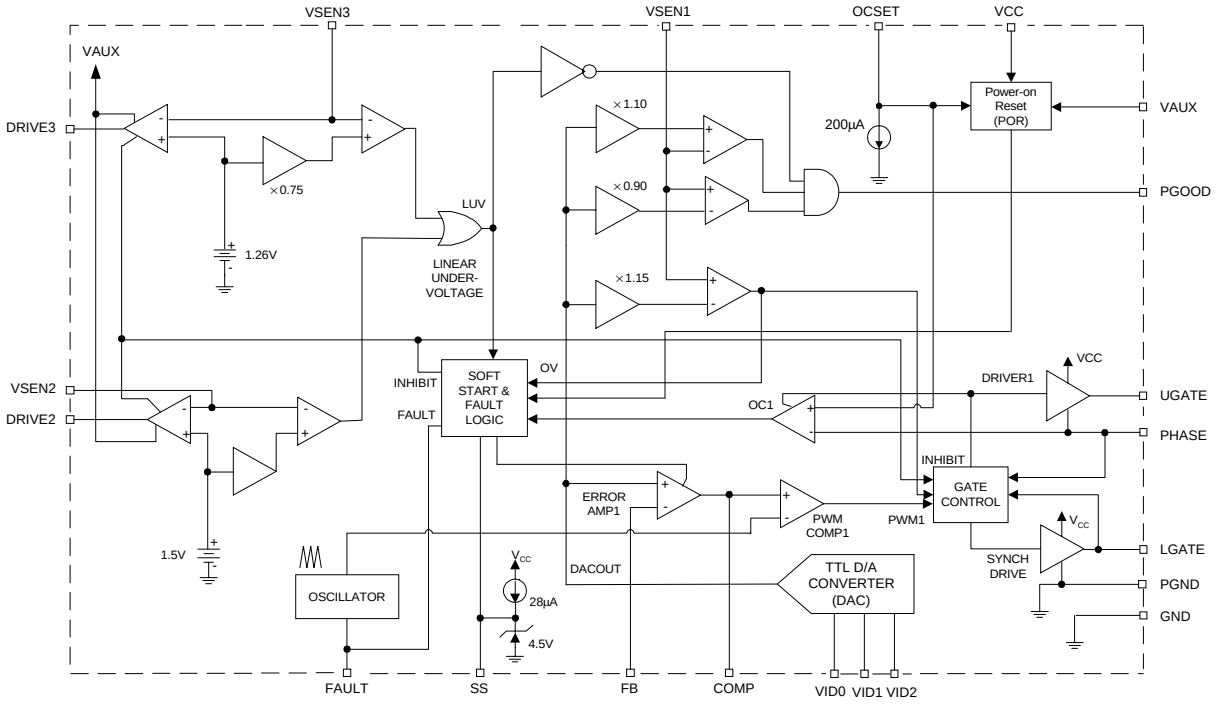
Pin Description



Ordering Information

APW7015 □□-□□ Handling Code Temp. Range Package Code	Package Code K : SOP - 24 Temp. Range C : 0 to 70℃ Handling Code TU : Tube TR : Tape & Reel

Block Diagram



Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{CC}	Supply Voltage	15	V
V_I, V_O	Input , Output or I/O Voltage	GND -0.3 V to V_{CC} +0.3	V
T_A	Operating Ambient Temperature Range	0 to 70	°C
T_J	Junction Temperature Range	0 to 125	°C
T_{STG}	Storage Temperature Range	-65 to +150	°C
T_S	Soldering Temperature	300 ,10 seconds	°C

Thermal Characteristics

Symbol	Parameter	Value	Unit
$R_{\theta JA}$	Thermal Resistance in Free Air SOIC SOIC (with 3in^2 of Copper)	 75 65	°C/W

Electrical Characteristics

(Recommended operating conditions, Unless otherwise noted) Refer to Block and Simplified Power System Diagrams, and Typical Application Schematic

Symbol	Parameter	Test Conditions	APW7015			Unit
			Min.	Typ.	Max.	
V_{CC} Supply Current						
I_{CC}	Nominal Supply Current	UGATE, LGATE, DRIVE2, DRIVE3 open		9		mA
Power-on Reset						
	Rising VCC Threshold	Vocset=4.5V			10.4	V
	Falling VCC Threshold	Vocset=4.5V	8.2			V
	Rising VAUX Threshold	Vocset=4.5V		2.5		V
	VAUX Threshold Hysteresis	Vocset=4.5V		0.5		V
	Rising V_{OCSET} Threshold			1.26		V
Oscillator						
F_{OCS}	Free Running Frequency	RT= Open	185	200	215	kHz
ΔV_{OSC}	Ramp Amplitude	RT= Open		1.9		V_{P-P}
DAC and Bandgap Reference						
	DAC(VID0-VID2) Input Low Voltage				0.8	V
	DAC(VID0-VID2) Input High Voltage		2.0			V
	DACOUT Voltage accuracy		-2.0		+2.0	%
V_{BG}	Bandgap Reference Voltage			1.265		V
	Bandgap Reference Tolerance		-2.5		+2.5	%
Linear Regulators (OUT2, OUT3)						
	Regulation (All Linears)			3		%
	Output Drive Current (All Liners)	VAUX-V_{DRIVE} >0.6V	20	40		mA
Synchronous PWM Controller Error Amplifier						
	DC Gain			88		dB
GBWP	Gain-Bandwidth Product			15		MHz
SR	Slew Rate	COMP=10pF		6		V/μs

Electrical Characteristics Cont.

Symbol	Parameter	Test Conditions	APW7015			Unit
			Min.	Typ.	Max.	
PWM Controller Gate Driver						
I_{UGATE}	UGATE Source	V_{CC}=12V, V_{UGATE} =6V		1		A
R_{UGATE}	UGATE Sink	$V_{UGATE1-PHASE}$ =1V			3.5	Ω
I_{LGATE}	LGATE Source	V_{CC}=12V, V_{LGATE} =1V		1		A
R_{LGATE}	LGATE Sink	V_{LGATE}= 1V			3	Ω
Protection						
	VSEN1 Over-Voltage (VSEN1/DACOUT)	VSEN1 Rising		115	120	%
I_{OVP}	FAULT Souring Current	$V_{FAULT/RT}$=2.0V		8.5		mA
I_{OCSET}	OCSET Current Source	V_{OCSET}= 4.5V_{DC}	170	200	230	µA
I_{SS}	Soft Start Current			28		µA
Power Good						
	VSEN1 Upper Threshold (VSEN1/DACOUT)	VSEN1 Rising	108		110	%
	VSEN1 Under Voltage (VSEN1/DACOUT)	VSEN1 Rising	92		94	%
	VSEN1 Hysteresis (VSEN1 /DACOUT)	Upper /Lower Threshold		2		%
V_{PGOOD}	PGOOD Voltage Low	I_{PGOOD}= -4mA			0.8	V

Functional Pin Description

VCC (Pin 1)

Provide a 12V bias supply for the IC to this pin. This pin also provides the gate bias charge for all the MOSFETs controlled by the IC. The voltage at this pin is monitored for Power-On Reset (POR) purposes.

DRIVE2 (Pin 2)

Connect this pin to the gate of an external MOSFET. This pin provides the drive for the NVVDD regulator's pass transistor.

VID2, VID1, VID0 (Pins 5, 6 and 7)

VID0-2 are the TTL-compatible input pins to the 3-bit DAC. The logic states of these three pins program the internal voltage reference (DACOUT). The level of DACOUT sets the VTT converter output voltage, as well as the corresponding PGOOD and OVP thresholds.

PGOOD (Pin 8)

PGOOD is an open collector output used to indicate the status of the output voltages. This pin is pulled low when the synchronous regulator output is not within ±10% of the DACOUT reference voltage or when any of the other outputs are below their under-voltage thresholds.

VSEN2 (Pin 9)

Connect this pin to a resistor divider to set the linear regulator (NVVDD) output voltage.

Functional Pin Description (Cont.)

SS (Pin 10)

Connect a capacitor from this pin to ground. This capacitor, along with an internal 28mA current source, sets the soft-start interval of the converter.

FAULT (Pin 11)

This pin provides oscillator switching frequency adjustment. By placing a resistor (R_T) from this pin to GND, the nominal 200kHz switching frequency is increased according to the following equation:

$Fs = 200kHz + 5 \times 10^6 / R_T (kW)$ (R_T to GND)

Conversely, connecting a resistor from this pin to VCC reduces the switching frequency according to the following equation:

$Fs = 200kHz + 4 \times 10^7 / R_T (kW)$ (R_T to 12V)

Nominally, the voltage at this pin is 1.26V. In the event of an over-voltage or over-current condition, this pin is internally pulled to VCC.

VAUX (Pin 13)

This pin provides boost current for the linear regulator's output drives in the event bipolar NPN transistors (instead of N-channel MOSFETs) are employed as pass elements. The voltage at this pin is monitored for power-on reset purposes.

GND (Pin 14)

Signal ground for the IC. All voltage levels are measured with respect to this pin.

DRIVE3 (Pin 15)

Connect this pin to the gate of an external MOSFET. This pin provides the drive for the FBVDDQ regulator's pass transistor.

VSEN3 (Pin 16)

Connect this pin to a resistor divider to set the linear regulator (FBVDDQ) output voltage.

COMP and FB (Pin 17, and 18)

COMP and FB are the available external pins of the PWM converter error amplifier. The FB pin is the inverting input of the error amplifier. Similarly, the COMP pin is the error amplifier output. These pins are used to compensate the voltage-mode control feedback loop of the synchronous PWM converter.

VSEN1 (Pin 19)

This pin is connected to the PWM converter's output voltage. The PGOOD and OVP comparator circuits use this signal to report output voltage status and for over- voltage protection.

OCSET (Pin 20)

Connect a resistor from this pin to the drain of the respective upper MOSFET. This resistor, an internal 200μA current source, and the upper MOSFET's on-resistance set the converter over-current trip point. An over-current trip cycles the soft-start function. The voltage at this pin is monitored for power-on reset (POR) purposes and pulling this pin low with an open drain device will shutdown the IC.

PGND (Pin 21)

This is the power ground connection. Tie the synchronous PWM converter's lower MOSFET source to this pin.

LGATE (Pin 22)

Connect LGATE to the PWM converter's lower MOSFET gate. This pin provides the gate drive for the lower MOSFET.

PHASE (Pin 23)

Connect the PHASE pin to the PWM converter's upper MOSFET source. This pin represents the gate drive return current path and is used to monitor the voltage drop across the upper MOSFET for over-current protection.

Functional Pin Description (Cont.)

UGATE (Pin 24)

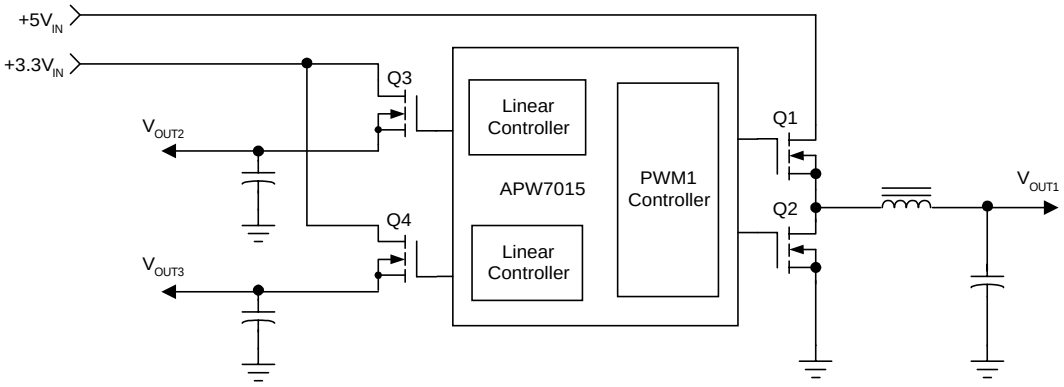
Connect UGATE pin to the PWM converter's upper MOSFET gate. This pin provides the gate drive for the upper MOSFET.

Table 1 Output Voltage Program

Pin Name			Nominal OUT1 Voltage DACOUT
VID2	VID1	VID0	
1	1	1	1.3
1	1	0	1.35
1	0	1	1.4
1	0	0	1.45
0	1	1	1.5
0	1	0	1.55
0	0	1	1.6
0	0	0	1.65

Note : 0 = connected to GND or Vss, 1 = open or connected to 5V through pull-high resistors.

Typical Characteristics



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