

FEATURES

Display driving bias ; static-1/5

- Power supply voltage ; +5V \pm 10%
+3V \pm 10%
- Supply voltage range for display : $\leq 10V$
- Negative display voltage :
 $0 \geq V_{EE} \geq V_{DD} - 10V$
- CMOS Process
- Interface

Driver (cascade connection)	Controller
Other APU0065	APU0066

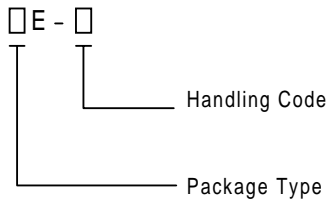
GENERAL DESCRIPTION

The APU0063 is a LCD driver LSI that is fabricated by low power CMOS technology. Basically this LSI consists of 40×2 bit bi-directional shift register, 40×2 bit data latch and 40×2 bit driver.

APPLICATIONS

- Dot matrix LCD driver with 80-channel output.
- Input / Output signal
- Output ; 40×2 channel waveform for LCD driving
- Input ; - Serial display data and control pulse from controller LSI .

ORDERING INFORMATION

<p>APU0063 □ E - □</p> 	<p>Package Type Q : QFP Y : Chip</p> <p>Handling Code TY : Tray</p>
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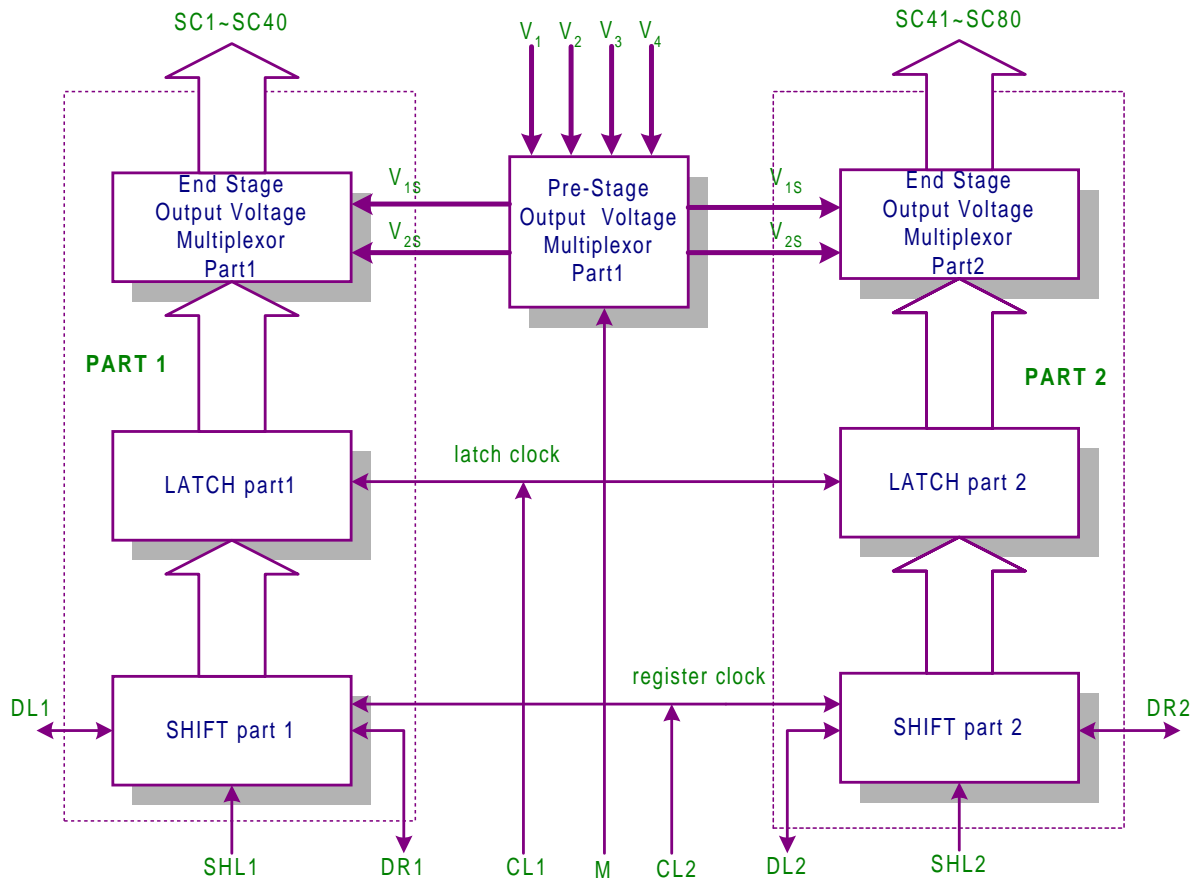


Figure 1. Block diagram of APU0063

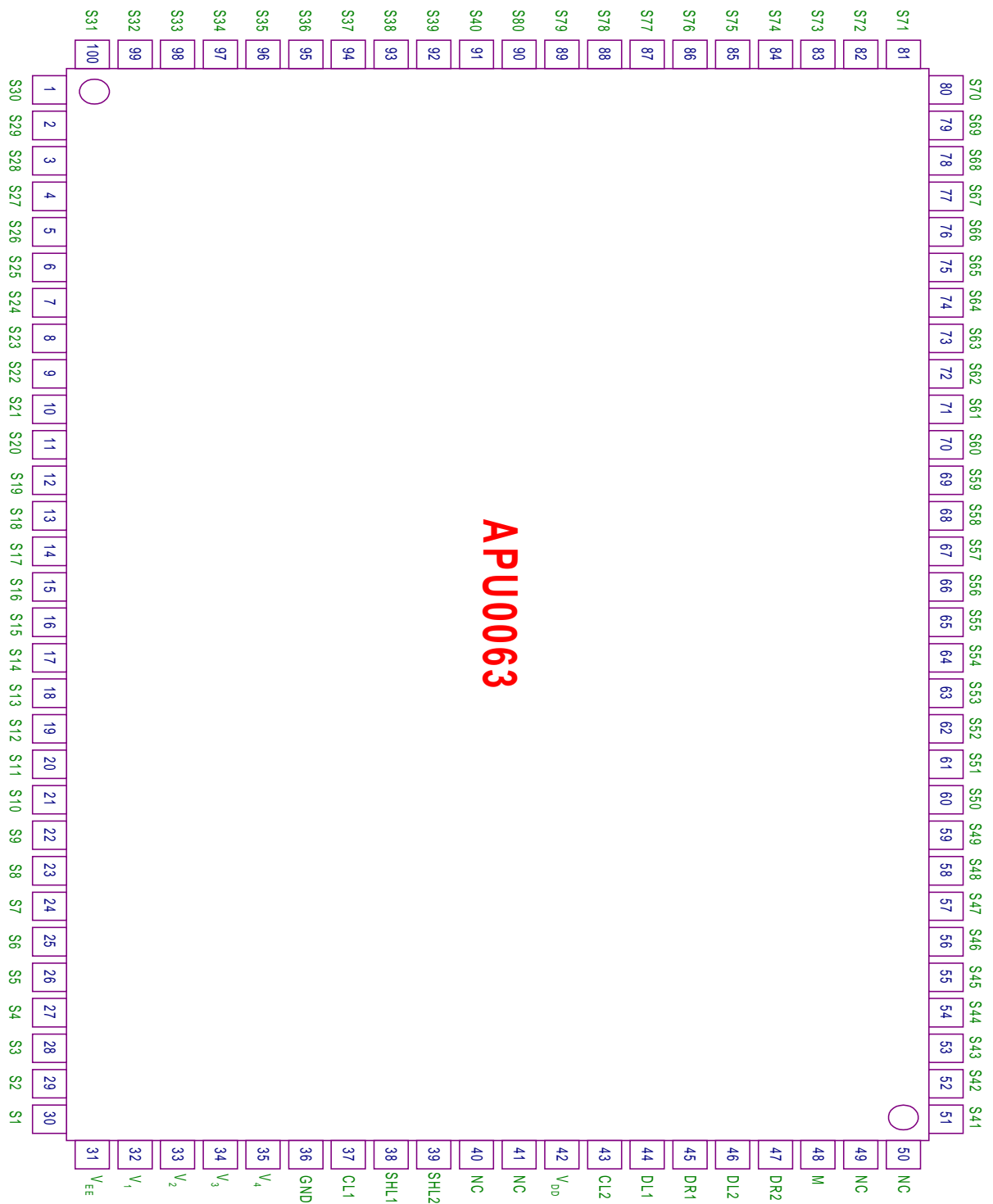




Figure 2. QFP100 Top View

PIN DESCRIPTION-QFP100

PIN(NO.)	INPUT OUTPUT	NAME	DESCRIPTION	INTERFACE									
V _{EE} (31)	Power	Negative Supply Voltage	For LCD driver circuit (0 ≥ V _{EE} ≥ V _{DD} -10V)	Power Supply									
V _{DD} (42)	Power	Operating Voltage	For logic circuit (+5V ± 10% , +3V ± 10%)	Power Supply									
V _{SS} (36)	Power	Operating Voltage	0V(GND)	Power Supply									
V ₁ ~ V ₄ (32 ~ 35)	Input	Bias Voltage	Bias Voltage level for LCD drive	Power Supply									
M(48)	Input	Altemated Signal for LCD Driver Output	This is the signal for LCD twisting	Controller									
CL1(37)	Input	Data Latch Clock	The signal enable the latch, it is negative sensitive latched. 	Controller									
CL2(43)	Input	Data Shift Clock	The signal enable the shift register, it is negative edge-trigger. 	Controller									
SHL1(38)	Input	Shifting Direction Control Signal of Part1	Selection of the shift directon of Part1 shift register <table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <td>SHL1</td> <td>DL1</td> <td>DR1</td> </tr> <tr> <td>V_{DD}</td> <td>Output</td> <td>Input</td> </tr> <tr> <td>V_{SS}</td> <td>Input</td> <td>Output</td> </tr> </table>	SHL1	DL1	DR1	V _{DD}	Output	Input	V _{SS}	Input	Output	Controller
SHL1	DL1	DR1											
V _{DD}	Output	Input											
V _{SS}	Input	Output											
DL1, DR1 (44, 45)	Input Output	Data Interface	Data input / output pf Part1 shift register	Controller or APU0066									
SC ₁ ~ SC ₄₀	Output	LCD Driver	LCD driver output of Part1	LCD									
SHL2(39)	Input	Shifting Direction Control Signal of Part2	Selection of the shift directon of Part2 shift register <table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <td>SHL2</td> <td>DL2</td> <td>DR2</td> </tr> <tr> <td>V_{DD}</td> <td>Output</td> <td>Input</td> </tr> <tr> <td>V_{SS}</td> <td>Input</td> <td>Output</td> </tr> </table>	SHL2	DL2	DR2	V _{DD}	Output	Input	V _{SS}	Input	Output	Controller
SHL2	DL2	DR2											
V _{DD}	Output	Input											
V _{SS}	Input	Output											
DL2, DR2 (46, 47)	Input Output	Data Interface	Data input / output pf Part2 shift register	Controller or APU0066									
SC ₄₁ ~ SC ₈₀	Output	LCD Driver	LCD driver output of Part2	LCD									

NOTE : Input pin can not be floated,or it will cause large leakage current.

DRIVER OUTPUT VOLTAGE

A signal of driving pin is the one of V_1, V_2, V_3 or V_4 . These selecting are following.

Data of latch	M	Output voltage
High	High	V_1
High	Low	V_2
Low	High	V_3
Low	Low	V_4

SHIFT DIRECTION SPECIFICATION

Part1

When Part1 shift direction control signal ,
 SHL1, is set to V_{SS} .
 Now the Part1 register shift direction is
 $DL1 \rightarrow SC1 \rightarrow SC2 \rightarrow \dots \rightarrow SC39 \rightarrow SC40$
 $\rightarrow DR1$
 Otherwise, when SHL1 is set to V_{DD} . Its
 direction is
 $DL1 \leftarrow SC1 \leftarrow SC2 \leftarrow \dots \leftarrow SC39 \leftarrow SC40$
 $\leftarrow DR1$

Part2

When Part2 shift direction control signal,
 SHL2, is set to V_{SS} .
 Now the Part2 register shift direction is
 $DL2 \rightarrow SC41 \rightarrow SC42 \rightarrow \dots \rightarrow SC79 \rightarrow$
 $SC80 \rightarrow DR2$
 Otherwise, when SHL2 is set to V_{DD} . Its
 direction is
 $DL2 \leftarrow SC41 \leftarrow SC42 \leftarrow \dots \leftarrow SC79 \leftarrow$
 $SC80 \leftarrow DR2$

MAXIMUM ABSOLUTE LIMIT (Ta = 25 °C)

Characteristic	Symbol	Value	Unit
Operating Voltage	V_{DD}	- 0.3 ~ + 7.0	V
Driver Supply Voltage	V_{LCD}	$V_{DD} - 13.5 \sim V_{DD} + 0.3$	V
Input Voltage 1	V_{IN1}	- 0.3 ~ $V_{DD} + 0.3$	V
Input Voltage 2 ($V_1 \sim V_4$)	V_{IN2}	$V_{DD} + 0.3 \sim V_{EE} - 0.3$	V
Operating Temperature	T_{OPR}	- 30 ~ + 85	°C
Storage Temperature	T_{STG}	- 55 ~ + 125	°C

* Voltage greater than above may damage to the circuit

ELECTRICAL CHARACTERISTICS

 DC characteristics ($V_{DD} = 2.7 \sim 5.5V, 0 \geq V_{EE} \geq V_{DD} - 10V, V_{SS} = 0V, Ta = - 30 \sim + 85 \text{ °C}$)

Characteristic	Symbol	Test condition	Min	Max	Unit	Applicable pin
Operating Current*	I_{DD}	$f_{CL2} = 400 \text{ KHz}$	-	1	mA	-
Supply Current*	I_{EE}	$f_{CL1} = 1 \text{ KHz}$	-	10	μA	
Input High Voltage	V_{IH}	-	0.7 V_{DD}	V_{DD}	V	CL1, CL2, DR1, DR2, DR1, DR2, SHL1, SHL2, M, FCS
Input Low Voltage	V_{IL}		0	0.3 V_{DD}		
Input Leakage Current	I_{LKC}	$V_{IN} = 0 - V_{DD}$	-5	5	μA	
Output High Voltage	V_{OH}	$I_{OH} = -0.4 \text{ mA}$	$V_{DD} - 0.4$	-	V	
Output Low Voltage	V_{OL}	$I_{OL} = +0.4 \text{ mA}$	-	0.4		
Voltage Descending	V_{D1}	$I_{ON} = 0.1\text{mA}$ for one of SC1-SC80	-	1.1	V	V ($V_1 \sim V_4$) - SC (SC1 ~ SC80)
	V_{D2}	$I_{ON} = 0.05\text{mA}$ for each SC1-SC80	-	1.5		
Leakage Current	I_V	$V_{IN} = V_{DD} \sim V_{EE}$ (Output SC1 ~ SC80 : floating)	-10	10	μA	$V_1 \sim V_4$

 AC CHARACTERISTICS ($V_{DD} = 2.7 \sim 5.5V, 0 \geq V_{EE} \geq V_{DD} - 10V, V_{SS} = 0V, Ta = - 30 \sim + 85 \text{ °C}$)

Characteristic	Symbol	Test condition	Min	Max	Unit	Applicable pin
Data shift Frequency	f_{CL}	-	-	400	KHz	CL2
Clock High Level Width	t_{WCKH}	-	800	-	ns	CL1, CL2
Clock Low Level Width	t_{WCKL}	-	800	-		CL2
Clock Set-up Time	t_{SL}	from CL2 to CL1	500	-		CL1, CL2
	t_{LS}	from CL1 to CL2	500	-		
Clock Rise/Fall Time	t_R / t_F	-	-	200		
Data Set-up Time	t_{SU}	-	300	-		DL1, DL2, DR1, DR2, FLM
Data Hold Time	t_{DH}	-	300	-		
Data Delay Time	t_D	CL1=15pF	-	500		DL1, DL2, DR1, DR2

TIMING CHARACTERISTICS

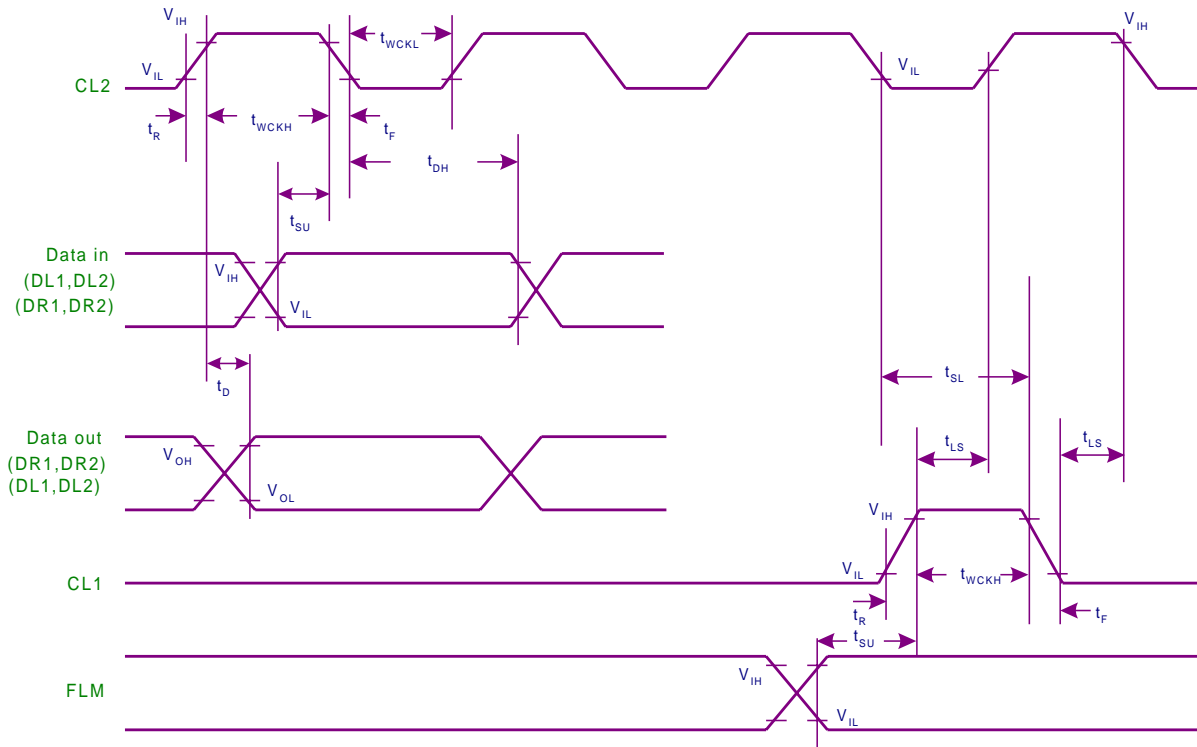


Figure 3. Timing diagram of signals

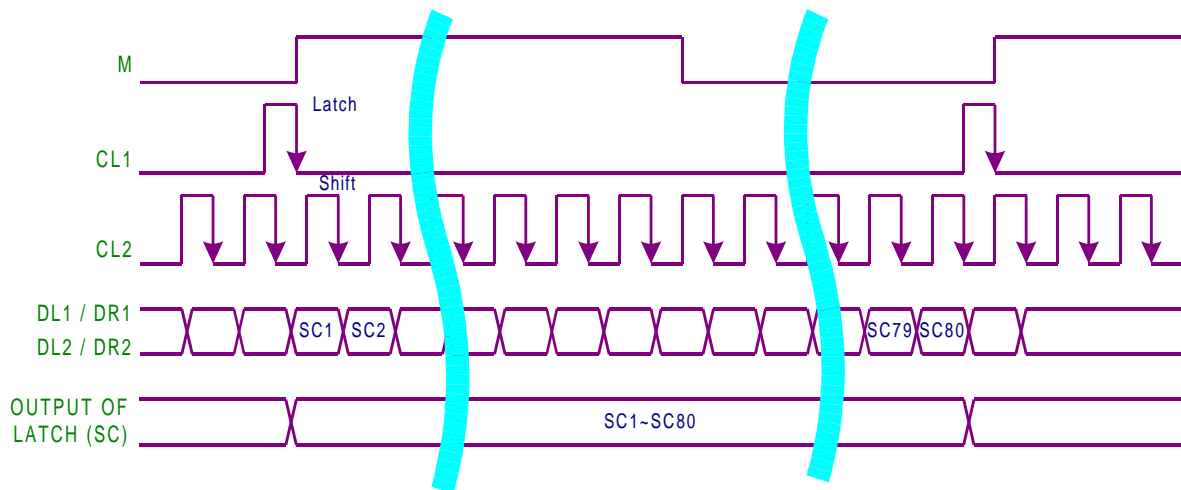


Figure 4. timing diagram

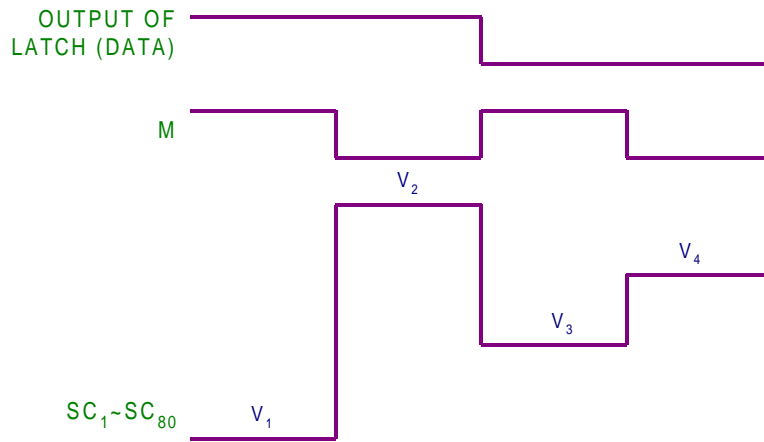


Figure 5. SC₁~SC₈₀ output waveform

APPLICATION CIRCUIT

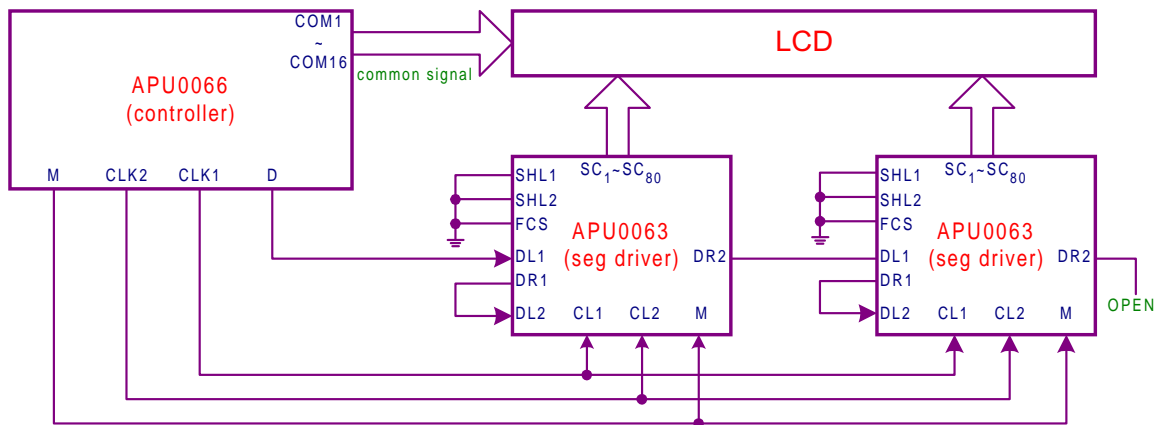
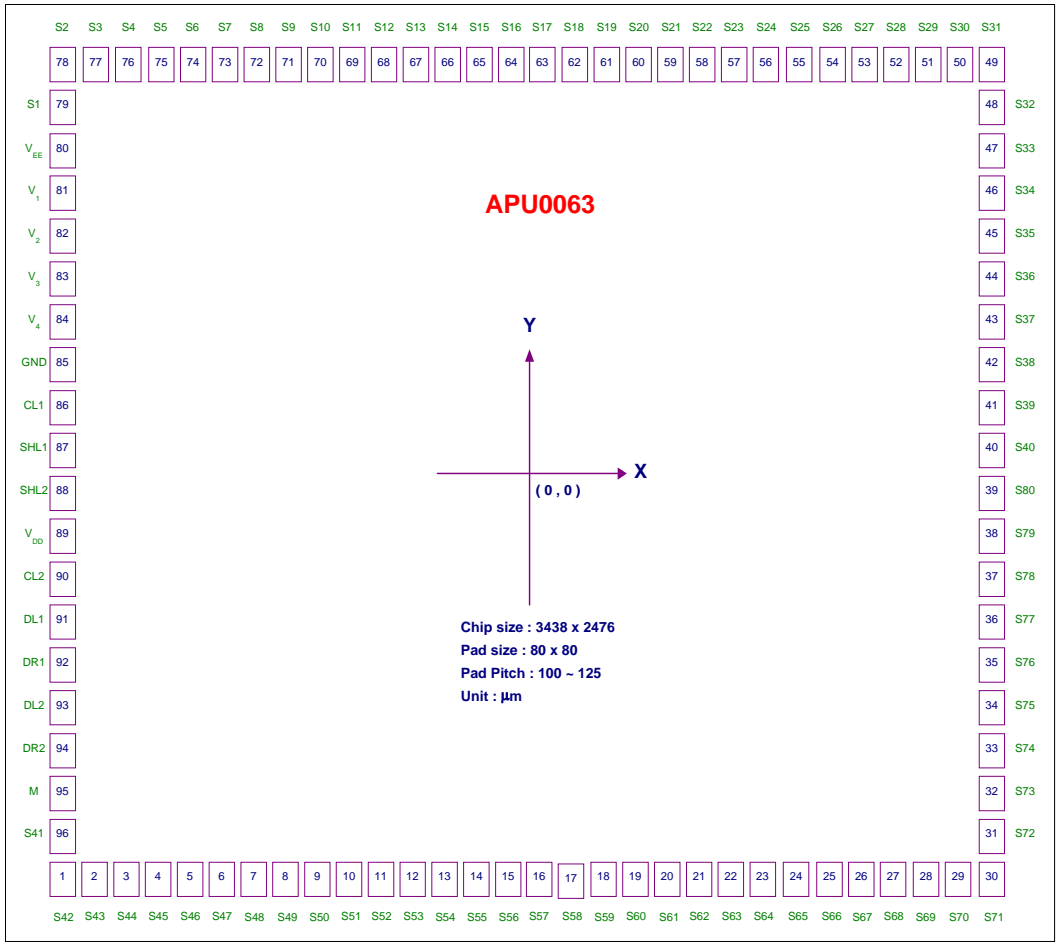


Figure 6. Connection between APU0063 and Controller



Note : (0 , 0) is center in the chip
 Bottom left corner coordination is (-1719 , -1238)
 Top right corner coordination is (1719 , 1238)

Figure 7. Chip pad arrangement

PAD LOCATION (1/2)

PAD NUMBER	PAD NAME	COORDINATE		PAD NUMBER	PAD NAME	COORDINATE	
		X	Y			X	Y
1	SC42	-1645	-1132	33	SC74	1609	-680
2	SC43	-1520	-1132	34	SC75	1609	-560
3	SC44	-1395	-1132	35	SC76	1609	-450
4	SC45	-1270	-1132	36	SC77	1609	-350
5	SC46	-1145	-1132	37	SC78	1609	-250
6	SC47	-1020	-1132	38	SC79	1609	-150
7	SC48	-900	-1132	39	SC80	1609	-50
8	SC49	-780	-1132	40	SC40	1609	50
9	SC50	-660	-1132	41	SC39	1609	150
10	SC51	-550	-1132	42	SC38	1609	250
11	SC52	-450	-1132	43	SC37	1609	350
12	SC53	-350	-1132	44	SC36	1609	450
13	SC54	-250	-1132	45	SC35	1609	560
14	SC55	-150	-1132	46	SC34	1609	680
15	SC56	-50	-1132	47	SC33	1609	800
16	SC57	50	-1132	48	SC32	1609	920
17	SC58	150	-1132	49	SC31	1645	1132
18	SC59	250	-1132	50	SC30	1520	1132
19	SC60	350	-1132	51	SC29	1395	1132
20	SC61	450	-1132	52	SC28	1270	1132
21	SC62	550	-1132	53	SC27	1145	1132
22	SC63	660	-1132	54	SC26	1020	1132
23	SC64	780	-1132	55	SC25	900	1132
24	SC65	900	-1132	56	SC24	780	1132
25	SC66	1020	-1132	57	SC23	660	1132
26	SC67	1145	-1132	58	SC22	550	1132
27	SC68	1270	-1132	59	SC21	450	1132
28	SC69	1395	-1132	60	SC20	350	1132
29	SC70	1520	-1132	61	SC19	250	1132
30	SC71	1645	-1132	62	SC18	150	1132
31	SC72	1609	-920	63	SC17	50	1132
32	SC73	1609	-800	64	SC16	-50	1132

PAD LOCATION (2/2)

PAD NUMBER	PAD NAME	COORDINATE		PAD NUMBER	PAD NAME	COORDINATE	
		X	Y			X	Y
65	SC15	-150	1132	81	V ₁	-1609	680
66	SC14	-250	1132	82	V ₂	-1609	560
67	SC13	-350	1132	83	V ₃	-1609	450
68	SC12	-450	1132	84	V ₄	-1609	350
69	SC11	-550	1132	85	GND	-1609	250
70	SC10	-660	1132	86	CL1	-1609	150
71	SC9	-780	1132	87	SHL1	-1609	50
72	SC8	-900	1132	88	SHL2	-1609	-50
73	SC7	-1020	1132	89	V _{DD}	-1609	-150
74	SC6	-1145	1132	90	CL2	-1609	-250
75	SC5	-1270	1132	91	DL1	-1609	-350
76	SC4	-1395	1132	92	DR1	-1609	-450
77	SC3	-1520	1132	93	DL2	-1609	-560
78	SC2	-1645	1132	94	DR2	-1609	-680
79	SC1	-1609	920	95	M	-1609	-800
80	V _{EE}	-1609	800	96	S41	-1609	-920

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