

16 COM / 40 SEG Driver & Controller for Dot Matrix LCD

**FEATURES**

- Internal Memory
  - Character Generator ROM : 8320 bits
  - Character Generator RAM : 512 bit
  - Display Data RAM : 80 × 8 bits for 80 digits
- Power Supply Voltage : 3V/5V ± 10%
- Supply Voltage for Display : 0 ~ -5V (V<sub>s</sub>)
- CMOS Process
- 1/8 duty, 1/11 duty or 1/16 duty : Selectable
  - 1/8 duty : 5 × 7dots format 1 line
  - 1/11 duty: 5 × 10 dots format 1 line
  - 1/16 duty : 5 × 7dots format 2 line
- 80 QFP or Bare Chip Available
- Display Character Pattern :
  - 5 × 7dots format : 192 kinds
  - 5 × 10 dots format : 32 kinds
 (The special character pattern can be programmable by Character Generator RAM directly.)
- A Customer Character Pattern Can be Programmable by Mask Option
- Automatic Power on Reset Function
- It is Possible to Read Both Character Generator and Display Data RAM from MPU

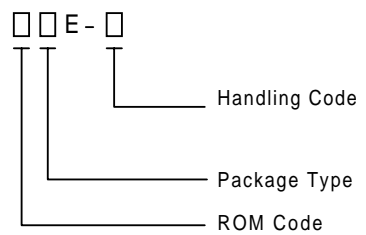
**APPLICATIONS**

- Character Type Dot Matrix LCD Driver & Controller
- Internal Driver :16 Common and 40 Segment Signal Output
- Display Character Format : 5 × 7 dots + Cursor, 5 × 10 dots + Cursor
- Easy Interface with a 4-bit or 8-bit MPU

**GENERAL DESCRIPTION**

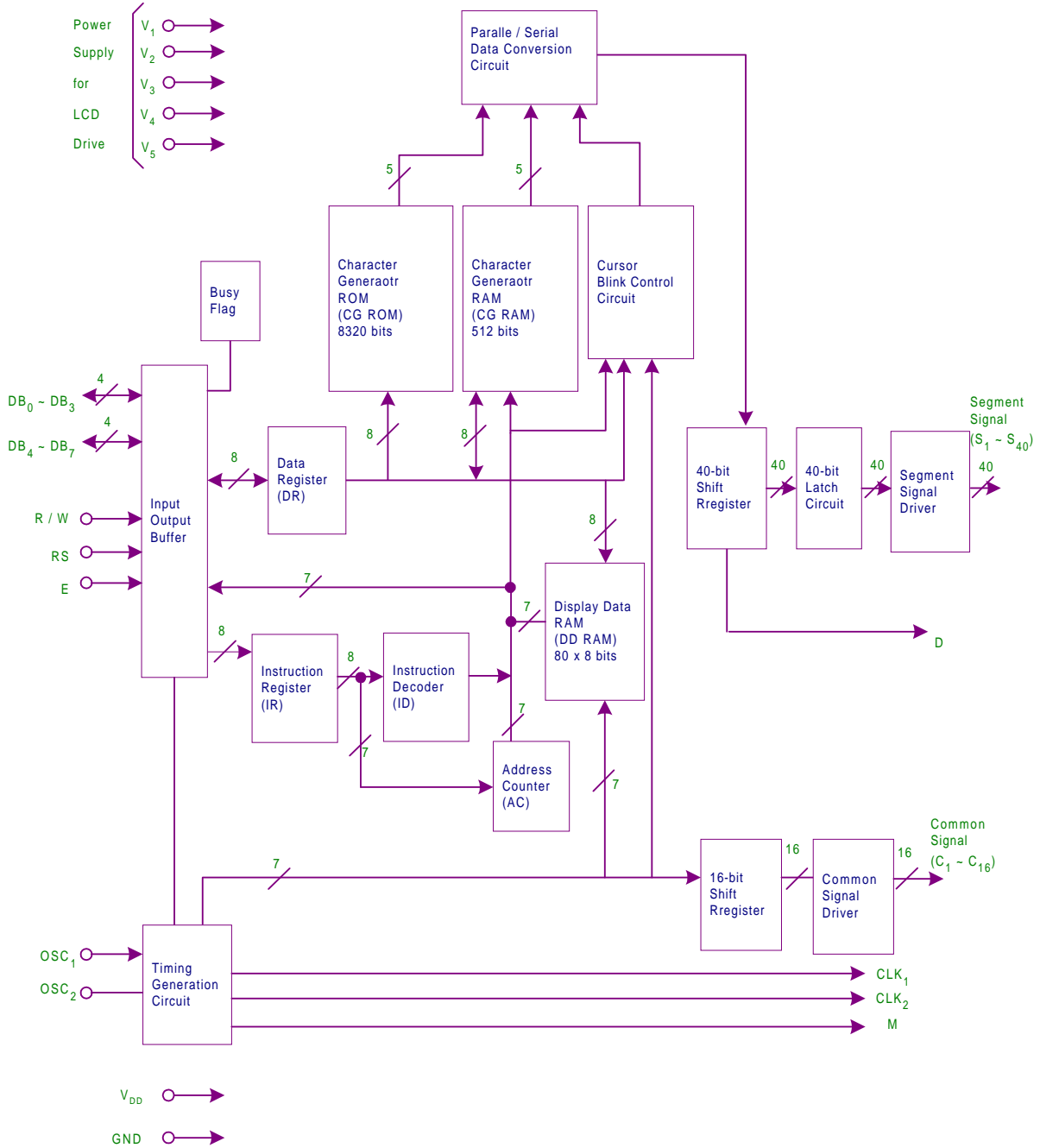
The APU0066 is a dot matrix LCD driver & controller LSI that is fabricated by low power CMOS technology.

**ORDERING INFORMATION**

<p>APU0066 □ □ E - □</p> 	<p>ROM Code 001 : Standard 002 : Customer</p> <p>Package Type Q : QFP Y : Chip</p> <p>Handling Code TY : Tray</p>
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ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

BLOCK DIAGRAM



**ABSOLUTE MAXIMUM RATINGS**  $T_A = 25^\circ\text{C}$

Symbol	Parameter	Rating	Unit
$V_{DD}$	Operating Voltage	-0.3 ~ +7	V
$V_{LCD}$	Driver Supply Voltage	$V_{DD} - 13.5 \sim V_{DD} + 0.3$	V
$V_{IN}$	Input Voltage	-0.3 ~ $V_{DD} + 0.3$	V
$P_D$	Power Dissipation	500	mW
$T_{OPR}$	Operating Temperature	-20 to +75	$^\circ\text{C}$
$T_{STG}$	Storage Temperature Range	-30 to +85	$^\circ\text{C}$

\* Voltage greater than above may damage to the circuit ( $V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$ )

**ELECTRICAL CHARACTERISTICS**

DC Characteristics ( $V_{DD} = 3V \pm 10\%$ ,  $V_{SS} = 0V$ ,  $T_A = -30 \sim 85^\circ\text{C}$ )

Symbol	Parameter	Test Conditions	APU0066			Unit	Applicable Pin		
			Min.	Typ.	Max.				
$V_{DD}$	Operating Voltage	—	2.7	3	3.3	V			
$I_{DD1}$	Operating Current (*1)	Ceramic Resonator $F_{OSC} = 250\text{KHz}$	—	0.3	0.5	mA			
$I_{DD2}$		Resistor Oscillation External Clock Operation $F_{OSC} = 270\text{KHz}$	—	0.17	0.3				
$V_{IH1}$	Input Voltage 1	—	High	1.9	—	V	E, DB <sub>0</sub> - DB <sub>7</sub> R/W, RS		
$V_{IL1}$			Low	-0.3	—			0.4	
$V_{IH2}$	Input Voltage 2	—	High	$0.7V_{DD}$	—	V	OSC <sub>1</sub>		
$V_{IL2}$			Low	—	—			$0.2V_{DD}$	
$V_{OH1}$	Output Voltage 1	$I_{OH} = -0.1\text{mA}$	High	2.0	—	V	DB <sub>0</sub> - DB <sub>7</sub>		
$V_{LH1}$			Low	—	—			0.4	
$V_{OH2}$	Output Voltage 2	$I_O = -40\mu\text{A}$	High	$0.8V_{DD}$	—	V	CLK1, CLK2. M, D		
$V_{LH2}$			Low	—	—			$0.2V_{DD}$	
$VD_{COM}$	Voltage Drop (*2)	$I_O = \pm 0.05\text{mA}$	COM	—	1	V	C <sub>1</sub> ~ C <sub>16</sub> S <sub>1</sub> ~ S <sub>40</sub>		
$VD_{SEG}$			SEG	—	—			1.5	
$I_{LKG}$	Input Leakage Current	$V_{IN} = 0$ or $V_{DD}$	-1	—	1	$\mu\text{A}$	E		
$I_{IL}$	Input Low Current	$V_{DD} = 3V$ (test pull up R)	-10	-50	-120	$\mu\text{A}$	RS, R/W, DB <sub>0</sub> - DB <sub>7</sub>		
$F_{EC}$	External Clock		Frequency(*3)	125	250	350	KHz	OSC <sub>1</sub>	
Duty			Duty	45	50	55			%
$T_R$			Rise Time	—	—	0.2			$\mu\text{s}$
$T_F$			Fall Time	—	—	0.2			$\mu\text{s}$
$F_{OSC}$	Internal Clock Frequency (*3)	$R_f = 75\text{K} \Omega \pm 2\%$	190	270	350	KHz	OSC <sub>1</sub> , OSC <sub>2</sub>		
$V_{LCD1}$	LCD Driving Voltage (*4)	$V_{DD} - V_5$	1/5 bias	3	—	10	V	$V_1 - V_5$	
$V_{LCD2}$			1/4 bias	3	—	10			

Note: \*1 : The supply current value from  $V_{DD}$  when the power condition is as follows

$$V_{DD} = 5V, V_{SS} = 0V, V_5 = -2V \text{ (when } V_{DD} = 5V)$$

$$V_{DD} = 3V, V_{SS} = 0V, V_5 = -2V \text{ (when } V_{DD} = 3V)$$

\*2 : The voltage drop from LCD bias terminals  $V_{DD}$ ,  $V_1$ ,  $V_4$  and  $V_5$  to each common terminal (C<sub>1</sub> ~ C<sub>16</sub>). And also the voltage drop from LCD bias terminals  $V_{DD}$ ,  $V_2$ ,  $V_3$  and  $V_5$  to each segment terminal (S<sub>1</sub> ~ S<sub>80</sub>).

\*3 and \*4 : Refer to oscillator circuit and input the voltage listed in the table below to  $V_1 \sim V_5$ .

DC Characteristics ( $V_{DD} = 5V \pm 10\%$ ,  $V_{SS} = 0V$ ,  $T_A = -20 \sim 75^\circ C$ )

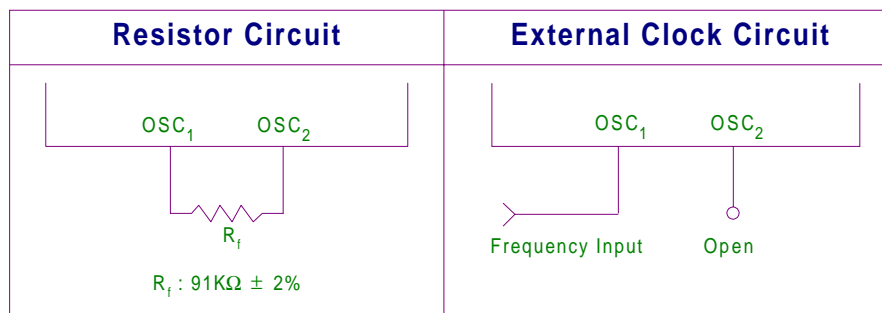
Symbol	Parameter	Test Conditions	APU0066			Unit	Applicable Pin		
			Min.	Typ.	Max.				
$V_{DD}$	Operating Voltage	—	4.5	—	5.5	V	—		
$I_{DD1}$	Operating Current (*1)	Ceramic Resonator $F_{OSC} = 250KHz$	—	0.55	0.8	mA	—		
$I_{DD2}$		Resistor Oscillation External Clock Operation $F_{OSC} = 270KHz$	—	0.35	0.6				
$V_{IH1}$ $V_{IL1}$	Input Voltage 1	—	High	2.2	—	V	E, DB <sub>0</sub> - DB <sub>7</sub> R/W, RS		
			Low	-0.3	—			0.6	
$V_{IH2}$ $V_{IL2}$	Input Voltage 2	—	High	$V_{DD} - 1$	—	V	OSC <sub>1</sub>		
			Low	-0.2	—			1	
$V_{OH1}$ $V_{LH1}$	Output Voltage 1	$I_{OH} = -0.205mA$	High	2.4	—	V	DB <sub>0</sub> - DB <sub>7</sub>		
		$I_{OL} = 1.2mA$	Low	—	—			0.4	
$V_{OH2}$ $V_{LH2}$	Output Voltage 2	$I_O = -40\mu A$	High	$0.9V_{DD}$	—	V	CLK1, CLK2. M, D		
		$I_O = 40\mu A$	Low	—	—			$0.1V_{DD}$	
$VD_{COM}$ $VD_{SEG}$	Voltage Drop (*2)	$I_O = \pm 0.1mA$	COM	—	—	V	C <sub>1</sub> ~ C <sub>16</sub> S <sub>1</sub> ~ S <sub>40</sub>		
			SEG	—	—			1	
$I_{LKG}$	Input Leakage Current	$V_{IN} = 0$ or $V_{DD}$	-1	—	1	$\mu A$	E		
$I_{IL}$	Input Low Current	$V_{DD} = 5V$ (test pull up R)	-50	-125	-250	$\mu A$	RS, R/W, DB <sub>0</sub> - DB <sub>7</sub>		
$F_{EC}$	External Clock	Frequency (*3)	125	250	350	KHz	OSC <sub>1</sub>		
Duty			Duty	45	50			55	%
$T_R$			Rise Time	—	—			0.2	$\mu s$
$T_F$			Fall Time	—	—			0.2	$\mu s$
$F_{OSC1}$	Internal Clock Frequency (*3)	$R_f = 91K\Omega \pm 2\%$	190	270	350	KHz	OSC <sub>1</sub> , OSC <sub>2</sub>		
$V_{LCD1}$ $V_{LCD2}$	LCD Driving Voltage (*4)	$V_{DD} - V_5$	1/5 bias	4.6	—	V	$V_1 - V_5$		
			1/4 bias	3	—			10	

Note : \*1 : Applies to the current value flow in terminal  $V_{DD}$  when power is input as follows;

$V_{DD} = 5V$ ,  $GND = 0V$ ,  $V_1 = 3.4V$ ,  $V_2 = 1.8V$ ,  $V_3 = 0.2V$ ,  $V_4 = 1.4V$  and  $V_5 = -3V$ .

\*2 : Applied to the voltage drop occurring from terminals  $V_{DD}$ ,  $V_1$ ,  $V_4$  and  $V_5$  to each common terminal (C<sub>1</sub> - C<sub>16</sub>) when 0.1mA is flown in or out to and from all COM and SEG terminals, and also to voltage drop occurring from terminals  $V_{DD}$ ,  $V_2$ ,  $V_3$  and  $V_5$  to each SEG terminal (S<sub>1</sub> ~ S<sub>40</sub>). When the output level is at  $V_{DD}$ ,  $V_1$ ,  $V_2$  level, 0.1mA is flown out, while 0.1mA flow in when the output level is at  $V_3$ ,  $V_4$  or  $V_5$  level. This occurs when 5V or -5V is input to  $V_{DD}$ ,  $V_1$  and  $V_3$  or to  $V_2$ ,  $V_4$ , and  $V_5$  respectively.

\*3 : Oscillator Circuit



\*4 : Input the voltage listed in the table below to  $V_1 - V_5$

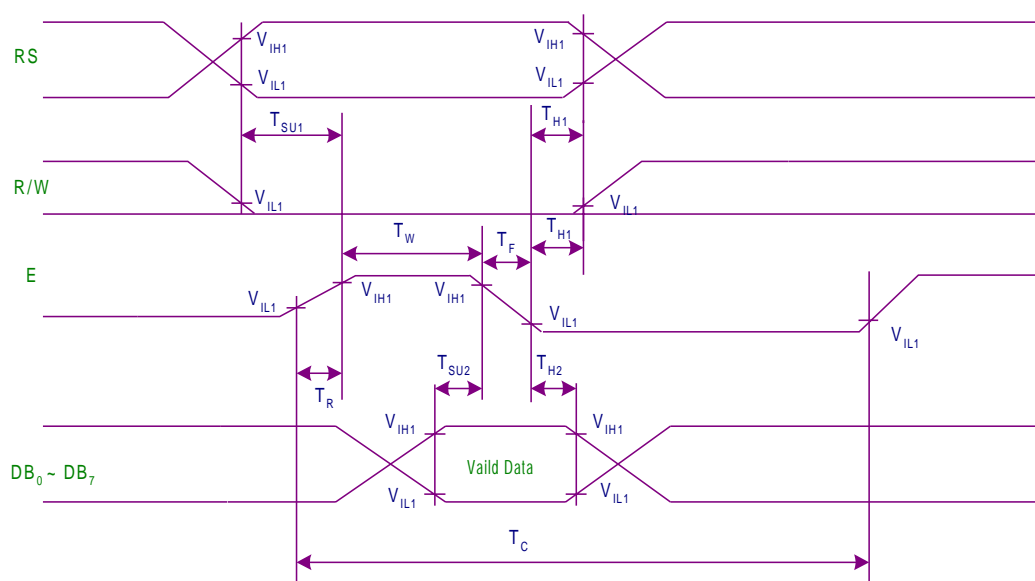
Duty	1/8, 1/11	1/16
Bias	1/4	1/5
Power Supply		
$V_1$	$V_{DD} - V_{LCD} / 4$	$V_{DD} - V_{LCD} / 5$
$V_2$	$V_{DD} - V_{LCD} / 2$	$V_{DD} - 2V_{LCD} / 5$
$V_3$	$V_{DD} - V_{LCD} / 2$	$V_{DD} - 3V_{LCD} / 5$
$V_4$	$V_{DD} - 3V_{LCD} / 4$	$V_{DD} - 4V_{LCD} / 5$
$V_5$	$V_{DD} - V_{LCD}$	$V_{DD} - V_{LCD}$

\*  $V_{LCD}$  is the LCD driving voltage, refer to the initial set of the instruction code.

AC Characteristics ( $V_{DD} = 5V \pm 10\%$ ,  $V_{SS} = 0V$ ,  $T_A = -20 \sim +75^\circ C$ )

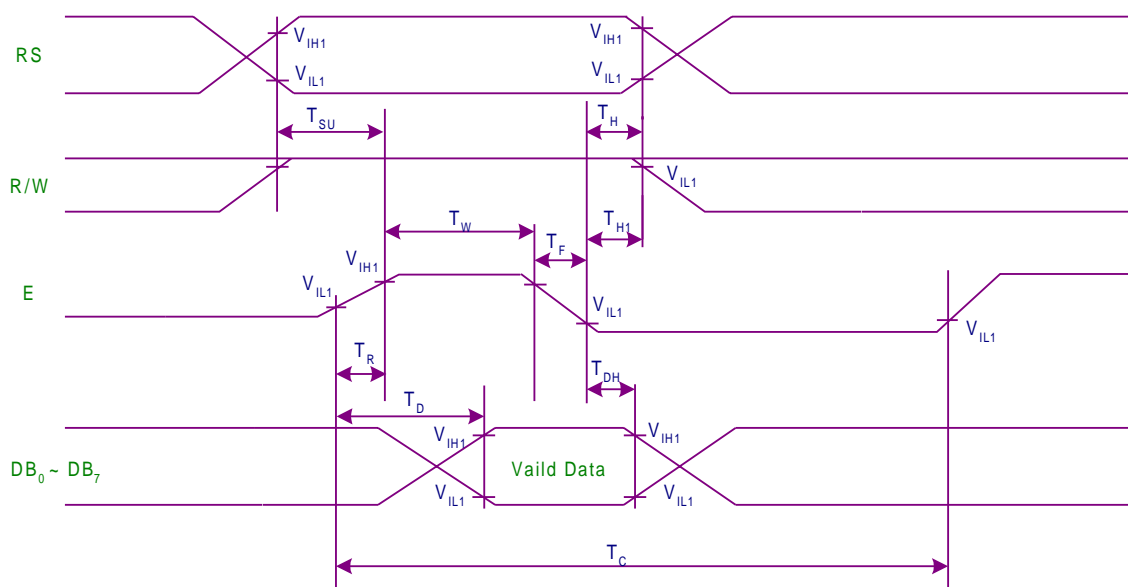
1. Write mode

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Test Pin
$T_C$	E Cycle Time	500	-	-	ns	E
$T_R$	E Rise Time	-	-	25	ns	E
$T_F$	E Fall Time	-	-	25	ns	E
$T_W$	E Pulse Width (High, Low)	220	-	-	ns	E
$T_{SU1}$	R/W and RS Set-up Time	40	-	-	ns	R/W, RS
$T_{H1}$	R/W and RS Hold Time	10	-	-	ns	R/W, RS
$T_{SU2}$	Data Set-up Time	60	-	-	ns	DB <sub>0</sub> ~ DB <sub>7</sub>
$T_{H2}$	Data Hold Time	10	-	-	ns	DB <sub>0</sub> ~ DB <sub>7</sub>



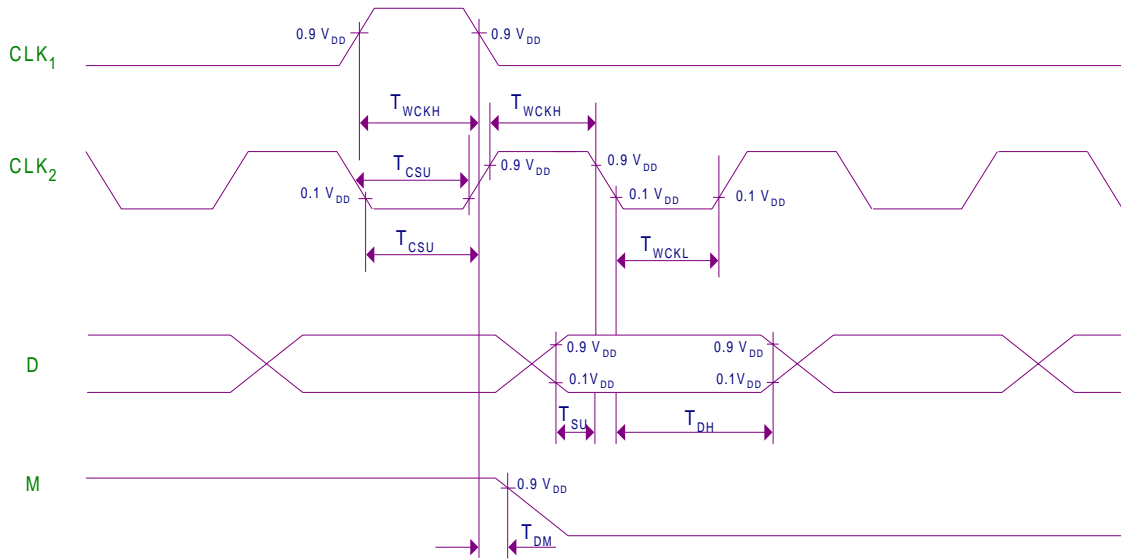
2. Read mode

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Test Pin
$T_C$	E Cycle Time	500	-	-	ns	E
$T_R$	E Rise Time	-	-	25	ns	E
$T_F$	E Fall Time	-	-	25	ns	E
$T_W$	E Pulse Width (High, Low)	220	-	-	ns	E
$T_{SU}$	R/W and RS Set-up Time	40	-	-	ns	R/W, RS
$T_H$	R/W and RS Hold Time	10	-	-	ns	R/W,RS
$T_D$	Data Output Delay Time	-	-	120	ns	DB <sub>0</sub> ~ DB <sub>7</sub>
$T_{DH}$	Data Hold Time	20	-	-	ns	DB <sub>0</sub> ~ DB <sub>7</sub>

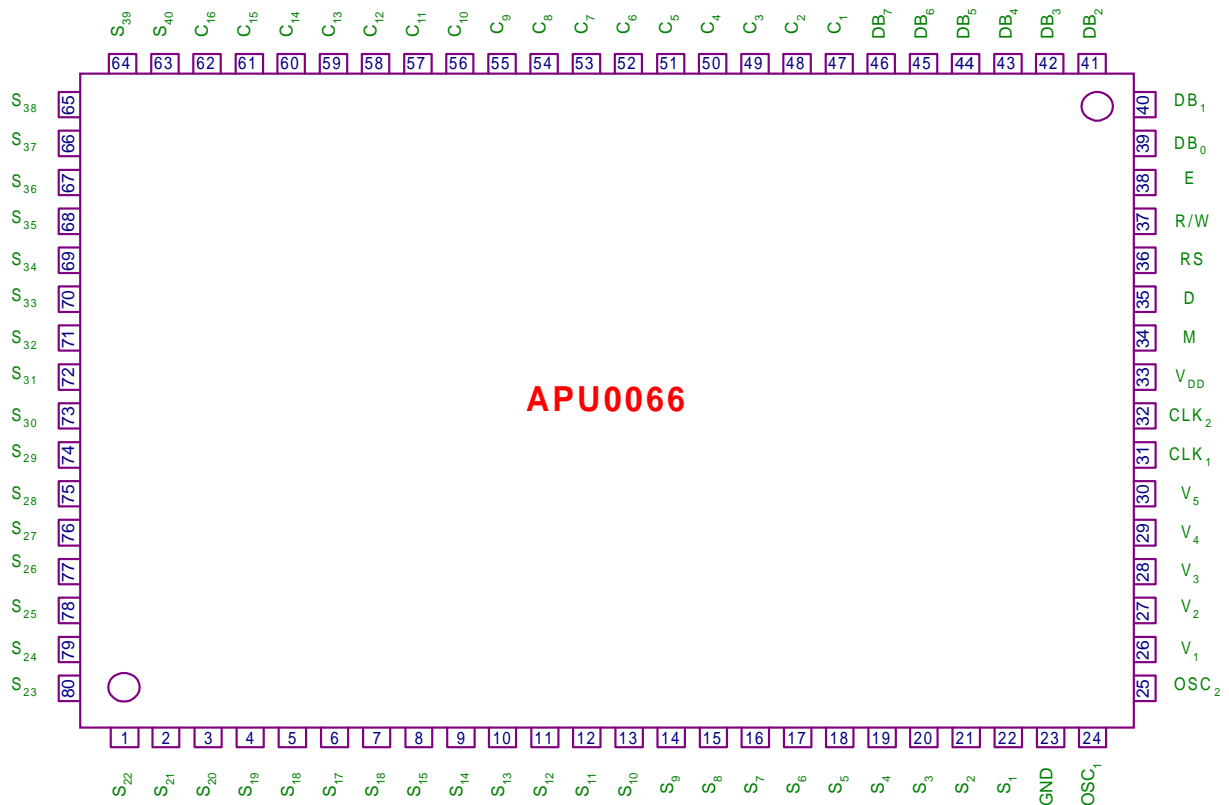


3. Interface mode with APU0065, APU0063

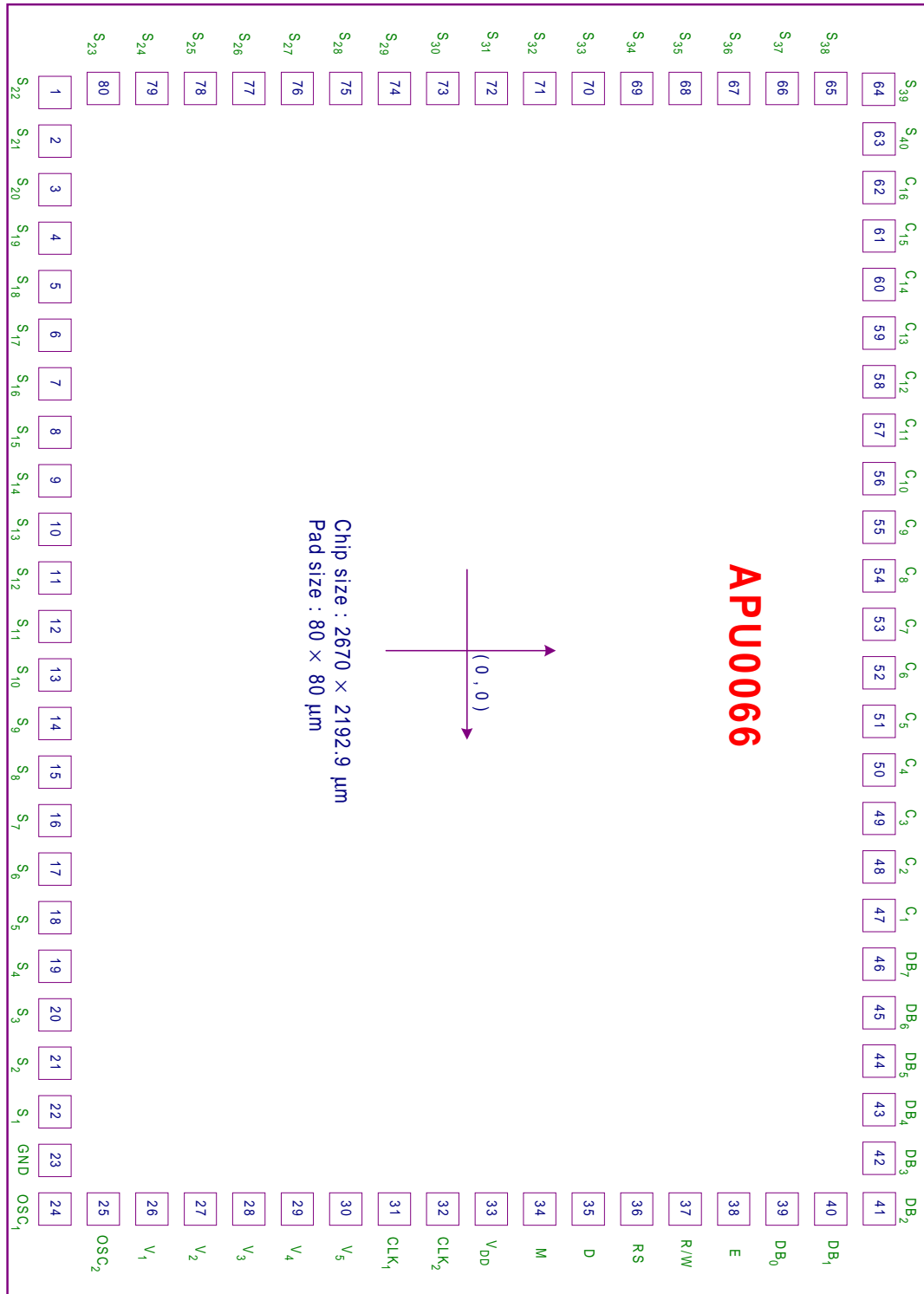
Symbol	Characteristic	Min.	Typ.	Max.	Unit	Test Pin
$T_{WCKH}$	Clock Pulse Width High	800	-	-	ns	CKL
$T_{WCKL}$	Clock Pulse Width Low	800	-	-	ns	CLK
$T_{SU}$	Data Set-up Time	300	-	-	ns	D
$T_{DH}$	Data Hold Time	300	-	-	ns	D
$T_{CSU}$	Clock Set-up Time	500	-	-	ns	CLK
$T_{DM}$	M Delay Time	-1000	-	1000	ns	M



**PIN CONFIGURATION \_80 QFP TOP VIEW**



**CHIP PAD ARRANGEMENT**





**PAD LOCATION**

PIN NO.	PIN NAME	X	Y	PIN NO.	PIN NAME	X	Y
1	S <sub>22</sub>	-1,265.00	-1,025.15	41	DB <sub>2</sub>	1,265.00	1,022.65
2	S <sub>21</sub>	-1,140.00	-1,031.45	42	DB <sub>3</sub>	1,140.00	1,031.45
3	S <sub>20</sub>	-1,015.00	-1,031.45	43	DB <sub>4</sub>	1,015.00	1,031.45
4	S <sub>19</sub>	-890.00	-1,031.45	44	DB <sub>5</sub>	890.00	1,031.45
5	S <sub>18</sub>	-770.00	-1,031.45	45	DB <sub>6</sub>	770.00	1,031.45
6	S <sub>17</sub>	-650.00	-1,031.45	46	DB <sub>7</sub>	650.00	1,031.45
7	S <sub>16</sub>	-550.00	-1,031.45	47	C <sub>1</sub>	550.00	1,031.45
8	S <sub>15</sub>	-450.00	-1,031.45	48	C <sub>2</sub>	450.00	1,031.45
9	S <sub>14</sub>	-350.00	-1,031.45	49	C <sub>3</sub>	350.00	1,031.45
10	S <sub>13</sub>	-250.00	-1,031.45	50	C <sub>4</sub>	250.00	1,031.45
11	S <sub>12</sub>	-150.00	-1,031.45	51	C <sub>5</sub>	150.00	1,031.45
12	S <sub>11</sub>	-50.00	-1,031.45	52	C <sub>6</sub>	50.00	1,031.45
13	S <sub>10</sub>	50.00	-1,031.45	53	C <sub>7</sub>	-50.00	1,031.45
14	S <sub>9</sub>	150.00	-1,031.45	54	C <sub>8</sub>	-150.00	1,031.45
15	S <sub>8</sub>	250.00	-1,031.45	55	C <sub>9</sub>	-250.00	1,031.45
16	S <sub>7</sub>	350.00	-1,031.45	56	C <sub>10</sub>	-350.00	1,031.45
17	S <sub>6</sub>	450.00	-1,031.45	57	C <sub>11</sub>	-450.00	1,031.45
18	S <sub>5</sub>	550.00	-1,031.45	58	C <sub>12</sub>	-550.00	1,031.45
19	S <sub>4</sub>	650.00	-1,031.45	59	C <sub>13</sub>	-650.00	1,031.45
20	S <sub>3</sub>	770.00	-1,031.45	60	C <sub>14</sub>	-770.00	1,031.45
21	S <sub>2</sub>	890.00	-1,031.45	61	C <sub>15</sub>	-890.00	1,031.45
22	S <sub>1</sub>	1,015.00	-1,031.45	62	C <sub>16</sub>	-1,015.00	1,031.45
23	GND	1,140.00	-1,031.45	63	S <sub>40</sub>	-1,140.00	1,031.45
24	OSC <sub>1</sub>	1,265.00	-1,024.55	64	S <sub>39</sub>	-1,265.00	1,021.20
25	OSC <sub>2</sub>	1,270.00	-811.95	65	S <sub>38</sub>	-1,270.00	808.05
26	V <sub>1</sub>	1,270.00	-691.95	66	S <sub>37</sub>	-1,270.00	688.05
27	V <sub>2</sub>	1,270.00	-571.95	67	S <sub>36</sub>	-1,270.00	568.05
28	V <sub>3</sub>	1,270.00	-451.95	68	S <sub>35</sub>	-1,270.00	448.05
29	V <sub>4</sub>	1,270.00	-351.95	69	S <sub>34</sub>	-1,270.00	348.05
30	V <sub>5</sub>	1,270.00	-251.95	70	S <sub>33</sub>	-1,270.00	248.05
31	CLK <sub>1</sub>	1,270.00	-151.95	71	S <sub>32</sub>	-1,270.00	148.05
32	CLK <sub>2</sub>	1,270.00	-51.95	72	S <sub>31</sub>	-1,270.00	48.05
33	V <sub>DD</sub>	1,270.00	48.05	73	S <sub>30</sub>	-1,270.00	-51.95
34	M	1,270.00	148.05	74	S <sub>29</sub>	-1,270.00	-151.95
35	D	1,270.00	248.05	75	S <sub>28</sub>	-1,270.00	-251.95
36	RS	1,270.00	348.05	76	S <sub>27</sub>	-1,270.00	-351.95
37	R/W	1,270.00	448.05	77	S <sub>26</sub>	-1,270.00	-451.95
38	E	1,270.00	568.05	78	S <sub>25</sub>	-1,270.00	-571.95
39	DB <sub>0</sub>	1,270.00	688.05	79	S <sub>24</sub>	-1,270.00	-691.95
40	DB <sub>1</sub>	1,270.00	808.05	80	S <sub>23</sub>	-1,270.00	-811.95

**PIN DESCRIPTION-QFP80**

Pin (No)	Input / Output	Name	Description	Interface	
V <sub>DD</sub> (33)	Power	Operating Voltage	For logical circuit (+5V ± 10%)	Power Supply	
V <sub>SS</sub> (GND) (23)			0V (GND)		
V <sub>1</sub> - V <sub>5</sub> (26 - 30)		Vegetative Supply Voltage	Bias voltage level for LCD driving		
S <sub>1</sub> - S <sub>40</sub> (22 - 1, 80 - 63)	Output	Segment Output	Segment signal output for LCD driving	LCD	
C <sub>1</sub> - C <sub>16</sub> (47 - 62)	Output	Common Output	Common signal output for LCD driving	LCD	
OSC <sub>1</sub> , OSC <sub>2</sub> (24) (25)	Input (OSC <sub>1</sub> ) Output (OSC <sub>2</sub> )	Oscillator	Both pins connected to Rf resistor or ceramic resonator for internal oscillator circuit. In case of external frequency use only, the frequency is input to (OSC <sub>1</sub> ) terminal.	Resistor or Ceramic Resonator	
CLK <sub>1</sub> (31)	Output	Data latch clock	Clock output terminal for the serially transferred data to be latched to the driver.	APU0065 or APU0063	
CLK <sub>2</sub> (32)		Data shift clock	Clock output terminal used when D terminal data output shifts the inside of the driver.		
M (34)		Alternated signal for LCD driver output	The alternating signal to convert LCD drive waveform to AC		
D (35)		Display data interface	Character pattern data, which is corresponding, to each common signal, is supplied to driver serially.		
E (38)	Input	Enable	Start enable signal to read or write the data	MPU	
R / W (37)		Read / Write	R/W signal input is used to select the read/write mode		
					High      Read mode Low      Write mode
RS (36)		Register select	Register selection input		
					High      Data register (for read and write) Low      Instruction register (for write), Busy flag, address counter (for read)
DB <sub>0</sub> - DB <sub>7</sub> (39 - 46)		Input / Output	Data interface		Used for data transfer between the MPU and APU0066. These terminals are for data bus with bi-directional three-state. Initial 4 bit (DB <sub>0</sub> - DB <sub>3</sub> ) are not used during 4 bit operation (DB <sub>7</sub> can be used as a busy flag)

**Customer Service**
**Anpec Electronics Corp.**

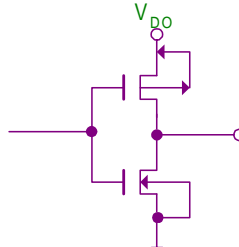
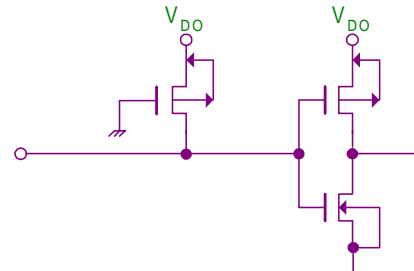
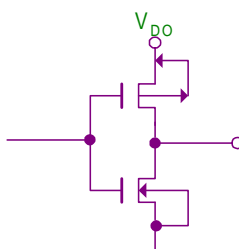
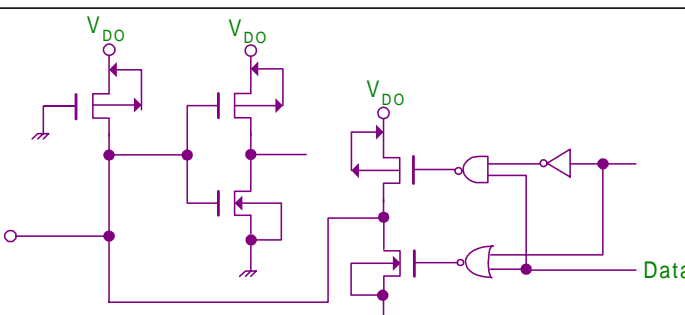
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 Fax : 886-2-89191369

**INTERNAL LOGIC of INPUT / OUTPUT TERMINAL**

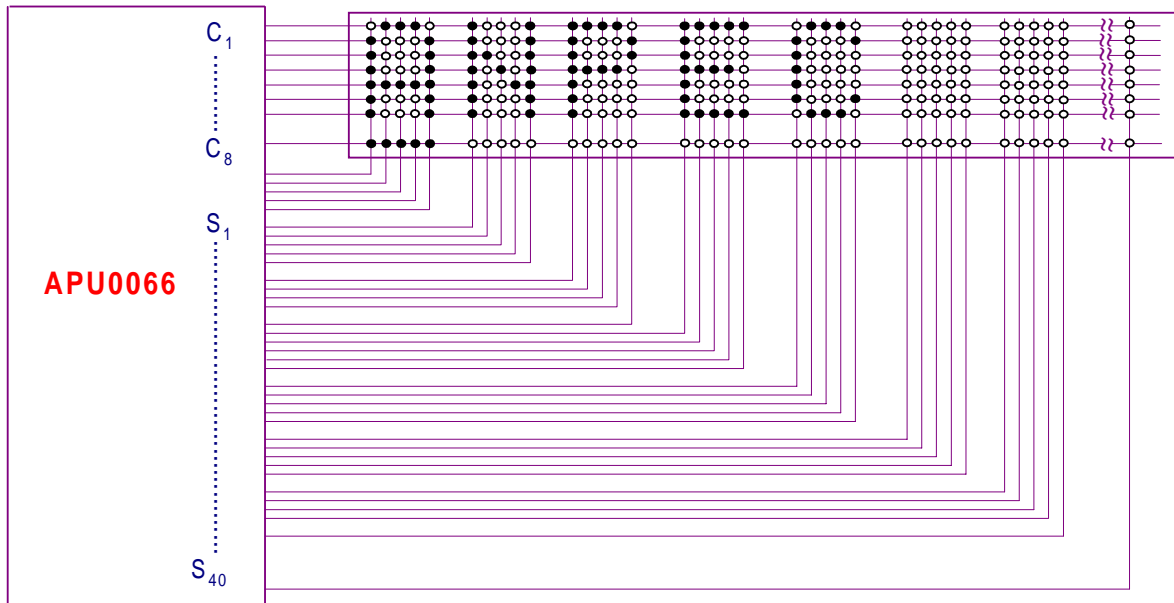
Input / Output		Logic Diagram	Applicable Pin
Input	No Pull Up		E
	With Pull Up		RS, R / W
Input			CLK <sub>1</sub> , CLK <sub>2</sub> , M, D
Input / Output			DB <sub>0</sub> ~ DB <sub>7</sub>

## CONTROL and DISPLAY COMMAND

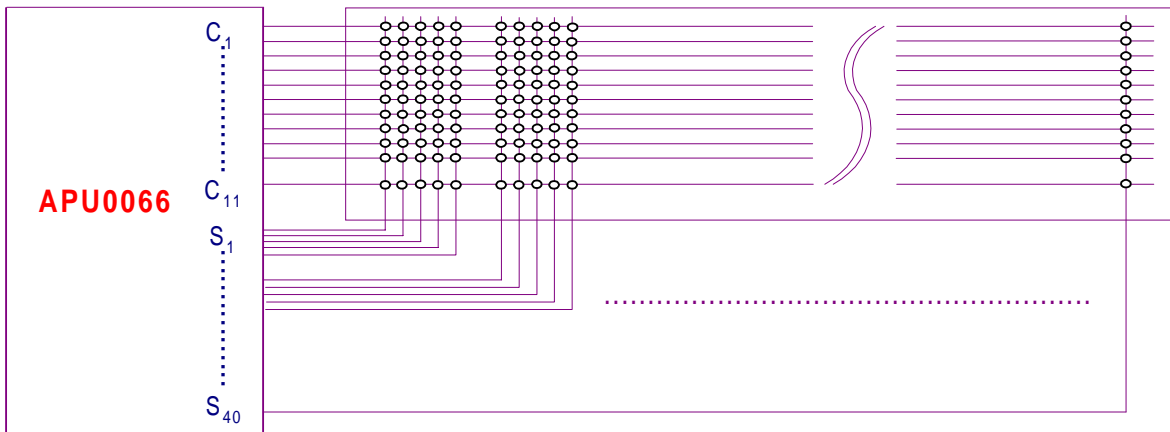
Command	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Execution Time (fosc=250KHz)	Remark
Display Clear	L	L	L	L	L	L	L	L	L	H	1.64ms	
Return Home	L	L	L	L	L	L	L	L	H	X	1.64ms	Cursor move to first digit
Entry Mode Set	L	L	L	L	L	L	L	H	I/D	SH	40μs	I/D : set cursor Move direction H : Increase L : Decrease SH : Specifies shift of display H : display is Shifted L : display is not Shifted
Display ON / OFF	L	L	L	L	L	L	H	D	C	B	40μs	Display H : Display on L : display off Cursor H : Cursor on L : Cursor off Blinking H : Blinking on L : Blinking off
Shift	L	L	L	L	L	H	S/C	R/L	X	X	40μs	SC : H : Display shift L : Cursor move R/L : H : Right shift L : Left shift
Set Function	L	L	L	L	H	DL	N	F	X	X	40μs	DL : H : 8 bits interface L : 4 bits interface N : H : 2 line display L : 1 line display F : H : 5 × 10 dots L : 5 × 7 dots
Set CG RAM Address	L	L	L	H	CG RAM address (corresponds to cursor address)						40μs	CG RAM data is sent and received after this setting
Set DD RAM Address	L	L	H	DD RAM address						40μs	DD RAM data is sent and received after this setting	
Write data	H	L	Writ Data								46μs	Write data into DD or CG RAM
Read data	H	H	Read Data								46μs	Read data from DD or CG RAM
Read Busy Flag & Address	L	H	BF	Address counter used for both DD & CG RAM address						0μs	BF : H : Busy L : Ready * Reads BF indication internal operating is being performed. * Reads address counter contents	

**APPLICATION INFORMATION ACCORDING to LCD PANEL**

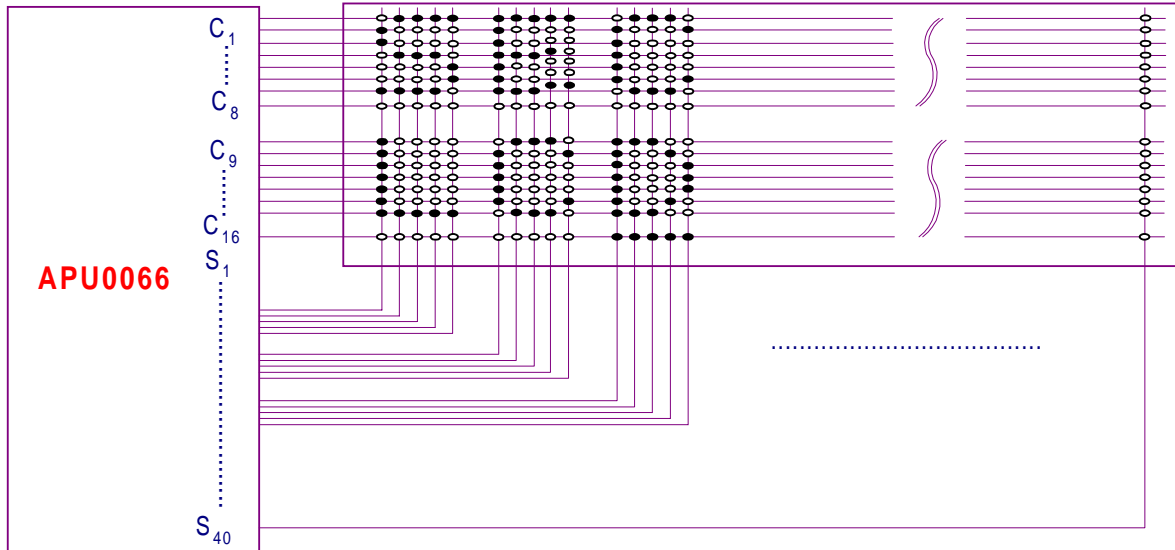
1. LCD Panel : 8 character  $\times$  1 line character format ; 5  $\times$  7 dots + 1 cursor line (1/4 bias, 1/8 duty)



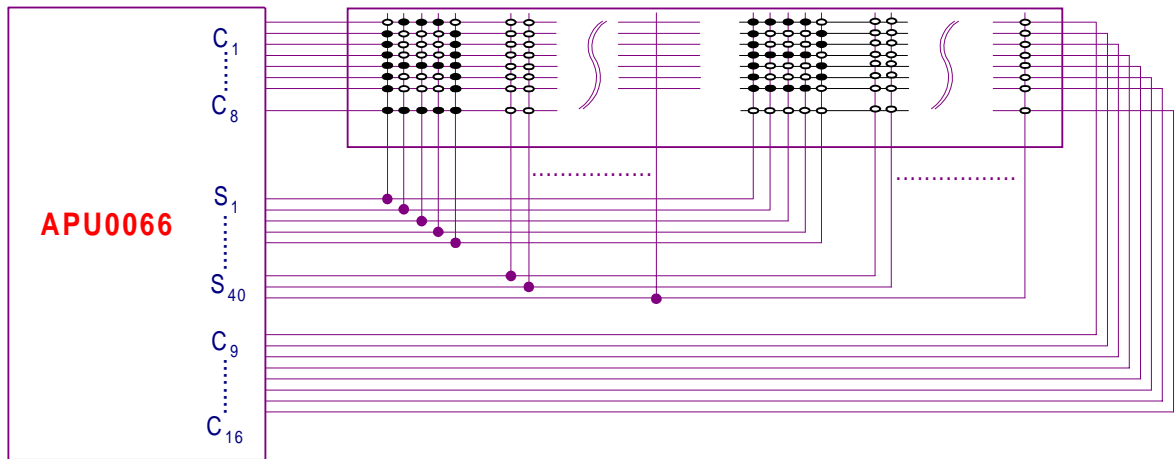
2. LCD Panel : 8 character  $\times$  1 line character format ; 5  $\times$  10 dots + 1 cursor line (1/4 bias, 1/8 duty)



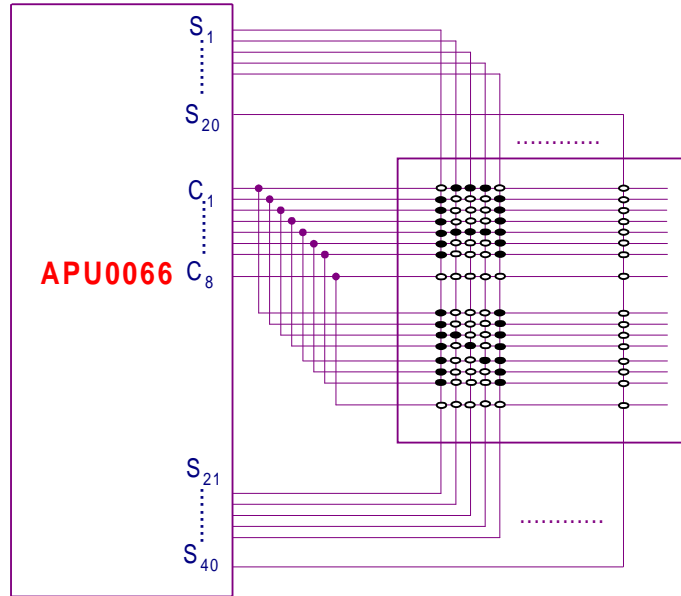
3. LCD Panel : 8 character  $\times$  2 line character format ; 5  $\times$  7 dots + 1 cursor line (1/5 bias, 1/16 duty)



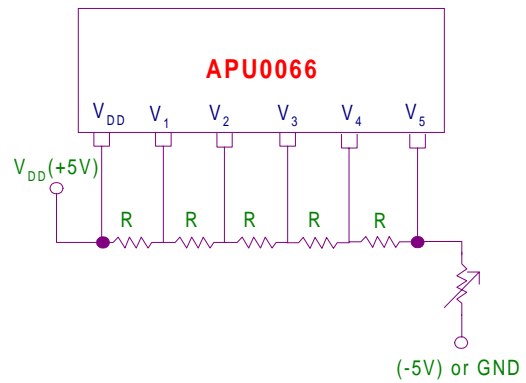
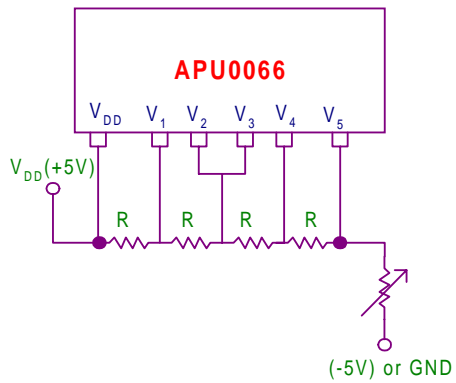
4. LCD Panel : 16 character  $\times$  1 line character format ; 5  $\times$  7 dots + 1 cursor line (1/5 bias, 1/16 duty)



5. LCD Panel : 4 character  $\times$  2 line character format ; 5  $\times$  7 dots + 1 cursor line (1/4 bias, 1/8 duty)



**BIAS VOLTAGE DIVIDE CIRCUIT**



STANDARD CHARACTER PATTERN

	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
XXXX0000	CG RAM (1)			0	1	P	Y	R					一	二	三	四
XXXX0001	CG RAM (2)		!	1	Q	a	a						。	ア	キ	ク
XXXX0010	CG RAM (3)		"	2	B	R	B	R					フ	イ	ウ	エ
XXXX0011	CG RAM (4)		#	3	C	S	C	S					レ	ウ	テ	エ
XXXX0100	CG RAM (5)		\$	4	D	T	d	t					。	工	ト	ナ
XXXX0101	CG RAM (6)		%	5	E	U	e	u					。	才	大	工
XXXX0110	CG RAM (7)		&	6	F	V	f	v					。	力	二	ヨ
XXXX0111	CG RAM (8)		*	7	G	W	g	w					。	才	大	工
XXXX1000	CG RAM (1)		(	8	H	X	h	x					。	力	二	ヨ
XXXX1001	CG RAM (2)		)	9	I	Y	i	y					。	才	大	工
XXXX1010	CG RAM (3)		*	0	J	Z	j	z					。	才	大	工
XXXX1011	CG RAM (4)		+	1	K	L	k	l					。	才	大	工
XXXX1100	CG RAM (5)		,	2	L	M	l	m					。	才	大	工
XXXX1101	CG RAM (6)		-	3	M	N	m	n					。	才	大	工
XXXX1110	CG RAM (7)		.	4	N	O	n	o					。	才	大	工
XXXX1111	CG RAM (8)		/	5	O	L	o	l					。	才	大	工