PA40

PRELIMINARY

FEATURES

- MONOLITHIC MOS TECHNOLOGY
- LOW COST
- HIGH VOLTAGE OPERATION—350V
- LOW QUIESCENT CURRENT—2mA
- NO SECOND BREAKDOWN
- HIGH OUTPUT CURRENT—120 mA PEAK

APPLICATIONS

- TELEPHONE RING GENERATOR
- PIEZO ELECTRIC POSITIONING
- ELECTROSTATIC TRANSDUCER & DEFLECTION
- DEFORMABLE MIRROR FOCUSING

DESCRIPTION

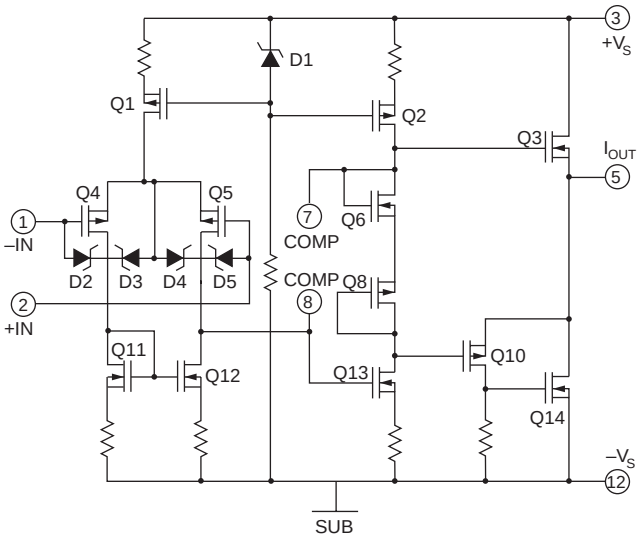
The PA40 is a high voltage monolithic MOSFET operational amplifier achieving performance features previously found only in hybrid designs while increasing reliability. Inputs are protected from excessive common mode and differential mode voltages. The safe operating area (SOA) has no second breakdown limitations. External compensation provides the user flexibility in choosing optimum gain and bandwidth for the application.

The PA40 is packaged in Apex's 7 LEAD TO220 package. The metal back of the package is tied to –Vs. The 15 mil minimum spacing of the TO220 package is adequate to stand-off the 350V rating of the PA40. The user must insure that a minimum of 11 mils spacing is maintained between pins for the circuit board artwork. If spacing is less than 11 mils, the voltage must be derated.

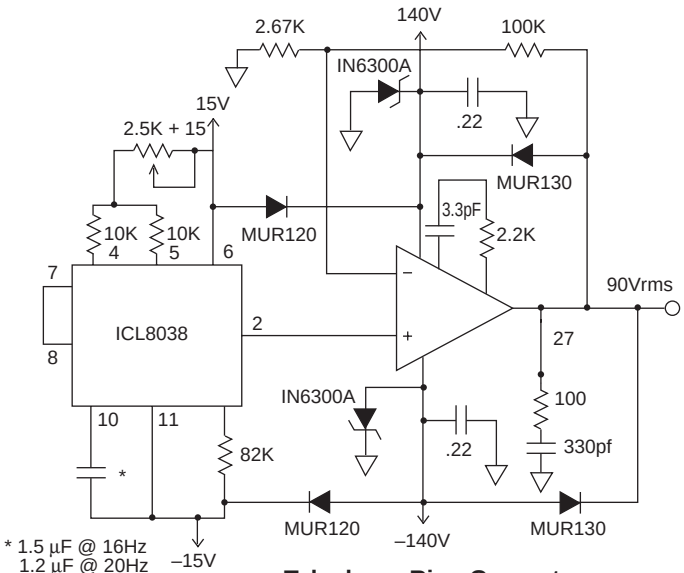
PA40 GRAPHIC HERE

The PA40 is set for a gain of 38.5 boosting the 2.33V signal to 90V. The recommended compensation for gains above 30 is used. If capacitive loading is at least 330pF at all times, the recommended snubber network may be omitted.

EQUIVALENT SCHEMATIC

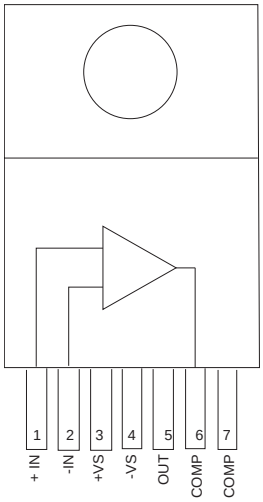


TYPICAL APPLICATION



Telephone Ring Generator

EXTERNAL CONNECTIONS



PHASE COMPENSATION

Gain	C_c	R_c
1	18pF	2.2K
10	10pF	2.2K
30	3.3pF	2.2K

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	350V
OUTPUT CURRENT, continuous within SOA	60 mA
OUTPUT CURRENT, peak	120 mA
POWER DISSIPATION, continuous @ T_C = 25°C	18W
INPUT VOLTAGE, differential	±16 V
INPUT VOLTAGE, common mode	$\pm V_S$
TEMPERATURE, pin solder – 10 sec	220°C
TEMPERATURE, junction[2]	150°C
TEMPERATURE, storage	–65 to +150°C
TEMPERATURE RANGE, powered (case)	–40 to +125°C

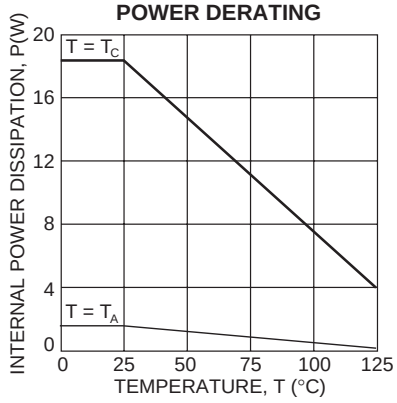
SPECIFICATIONS

		PA44			
PARAMETER	**TEST CONDITIONS[1]**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT					
OFFSET VOLTAGE, initial			15	30	mV
OFFSET VOLTAGE, vs. temperature[4]	Full temperature range		70	130	µV/°C
OFFSET VOLTAGE, vs supply			20	32	µV/V
OFFSET VOLTAGE, vs time			75		µV kh
BIAS CURRENT, initial			50	200	pA
BIAS CURRENT, vs supply			2	20	pA/V
OFFSET CURRENT, initial			50	200	pA
INPUT IMPEDANCE, DC			10^{12}		
INPUT CAPACITANCE			5		pF
COMMON MODE, voltage range		±VS–12			V
COMMON MODE REJECTION, DC	VCM = ±90V DC	84	94		dB
NOISE, broad band	10kHz BW, RS = 1K		50		µV RMS
NOISE, low frequency	1-10 Hz		10		µV p-p
GAIN					
OPEN LOOP at 15Hz	RL = 5K	94	106		dB
BANDWIDTH, open loop			1.6		MHz
POWER BANDWIDTH	CC = 10pf, 280V p-p		26		kHz
PHASE MARGIN	Full temperature range		60		°
OUTPUT					
VOLTAGE SWING	IO = 40mA	±VS–12	±VS–10		V
CURRENT, peak[5]				120	mA
CURRENT, continuous		60			mA
SETTLING TIME to .1%	CC = 10pF, 10V step, AV = –10		12		µs
SLEW RATE	CC = OPEN		40		V/µs
CAPACITIVE LOAD	AV = +1	10			nF
RESISTANCE6, no load	RCL = 0		150		
RESISTANCE6, 20 mA load	RCL = 0		25		
POWER SUPPLY					
VOLTAGE[3]	See Note 3	±50	±150	±175	V
CURRENT, quiescent			1.6	2.0	mA
THERMAL					
RESISTANCE, AC junction to case	F > 60Hz		3.7	4.3	°C/W
RESISTANCE, DC junction to case	F < 60Hz		5.6	6.8	°C/W
RESISTANCE, junction to air	Full temperature range			74	°C/W
TEMPERATURE RANGE, case	Meets full range specifications	–25		+85	°C

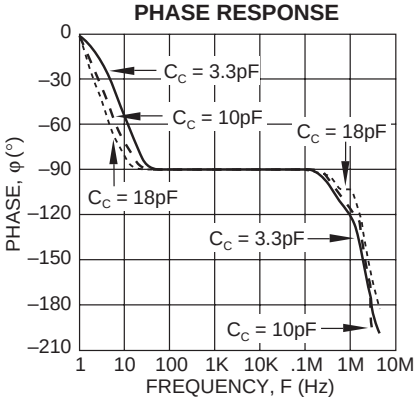
NOTES:
1. Unless otherwise noted T_C = 25°C, C_C = 18pF, R_C = 2.2K. DC input specifications are ± value given. Power supply voltage is typical rating.
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
3. Derate maximum supply voltage .5 V/°C below case temperature of 25°C. No derating is needed above TC = 25°C.
4. Sample tested by wafer to 95%.
5. Guaranteed but not tested.

CAUTION The PA40 is constructed from MOSFET transistors. ESD handling procedures must be observed.

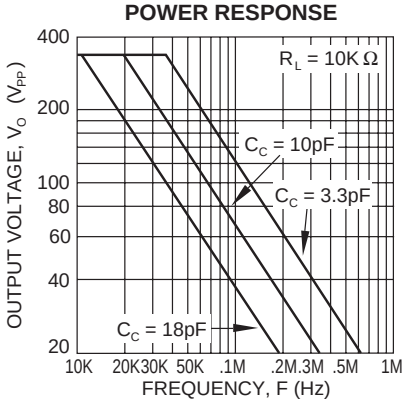
POWER DERATING



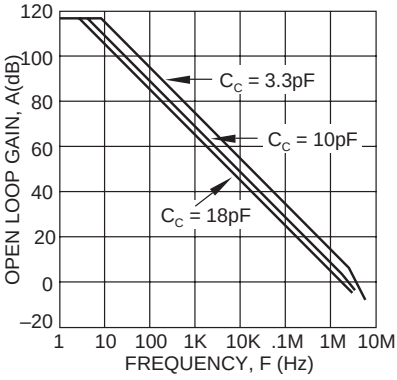
PHASE RESPONSE



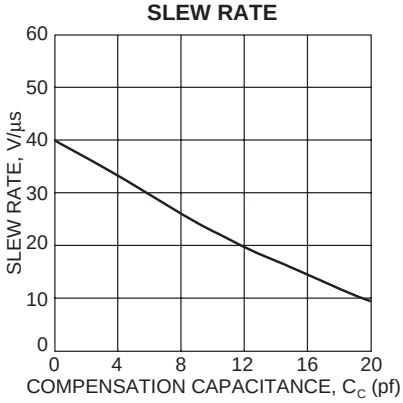
POWER RESPONSE



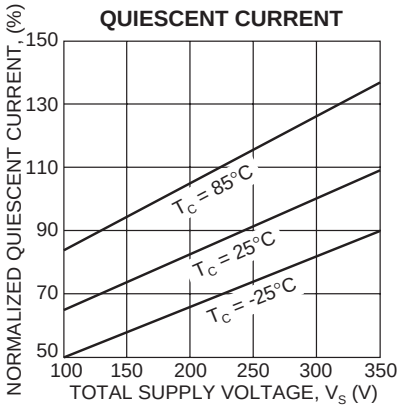
SMALL SIGNAL RESPONSE



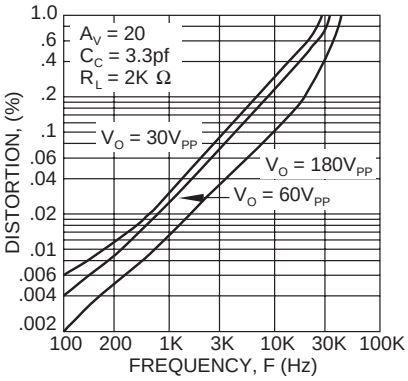
SLEW RATE



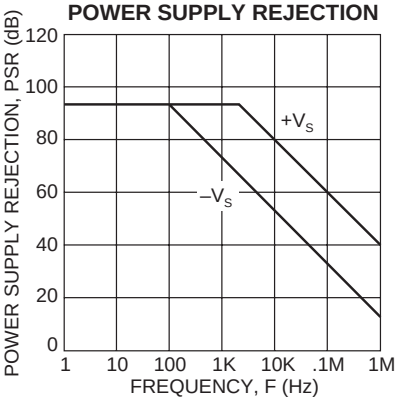
QUIESCENT CURRENT



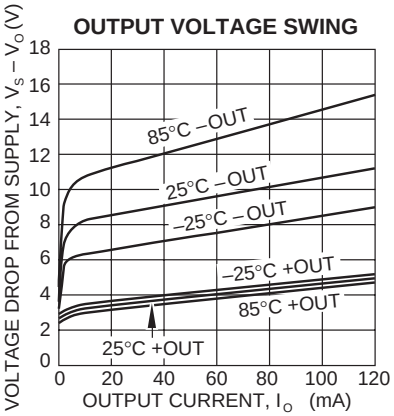
HARMONIC DISTORTION



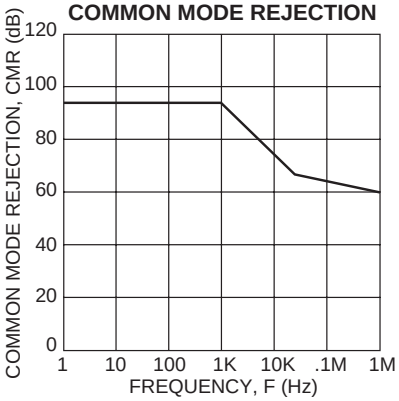
POWER SUPPLY REJECTION



OUTPUT VOLTAGE SWING



COMMON MODE REJECTION



GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.apexmicrotech.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit; heat sink selection; Apex's complete Application Notes library; Technical Seminar Workbook; and Evaluation Kits.

INPUT PROTECTION

The PA40 inputs are protected against common mode voltages up the supply rails and differential voltages up to ±16 volts as well as static discharge. Differential voltages exceeding 16 volts will be clipped by the protection circuitry. However, if more than a few milliamps of current is available from the overload source, the protection circuitry could be destroyed. The protection circuitry includes 300 ohm current limiting resistors at each input, but this may be insufficient for severe overloads. It may be necessary to add external resistors to the application circuit where severe overload conditions are expected. Limiting input current to 1mA will prevent damage.

STABILITY

The PA40 has sufficient phase margin when compensated for unity gain to be stable with capacitive loads of at least 10 nF. However, the low pass circuit created by the sumpoint (–in) capacitance and the feedback network may add phase shift and cause instabilities. As a general rule, the sumpoint load resistance (input and feedback resistors in parallel) should be 1K ohm or less at low gain settings (up to 10). Alternatively, use a bypass capacitor across the feedback resistor. The time constant of the feedback resistor and bypass capacitor combination should match the time constant of the sumpoint resistance and sumpoint capacitance.

The PA40 is externally compensated and performance can be tailored to the application. Use the graphs of small signal gain and phase response as well as the graphs for slew rate and power response as a guide. The compensation capacitor C_C must be rated at 350V working voltage. The compensation capacitor and associated resistor R_C must be mounted closely to the amplifier pins to avoid spurious oscillation. An NPO capacitor is recommended for compensation.

SAFE OPERATING AREA (SOA)

The MOSFET output stage of this power operational amplifier has two distinct limitations:

1. The current handling capability of the die metallization.
2. The temperature of the output MOSFETs.

NOTE: The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.