SA16

FEATURES

- HALF BRIDGE OUTPUT
- WIDE SUPPLY RANGE—16-500V
- 10A CONTINUOUS TO 75° C CASE
- 3 PROTECTION CIRCUITS
- ANALOG OR DIGITAL INPUTS
- SYNCHRONIZED OR EXTERNAL OSCILLATOR
- FLEXIBLE FREQUENCY CONTROL

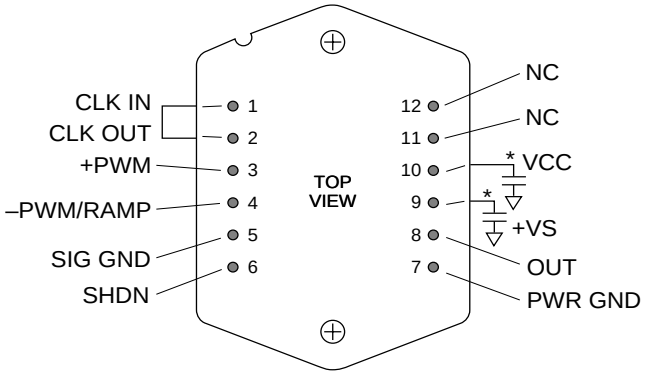
APPLICATIONS

- MOTORS
- REACTIVE LOADS
- LOW FREQUENCY SONAR
- LARGE PIEZO ELEMENTS
- OFF-LINE DRIVERS
- C-D WELD CONTROLLER

DESCRIPTION

The SA16 is a half bridge pulse width modulation amplifier that can supply 5000W to the load. Flexible frequency control is provided. An internal 45kHz oscillator requires no external components and can be used to synchronize multiple amplifiers. The oscillator output may be divided down and connected to the clock input to lower the switching frequency . The clock input stage divides by two and determines the output switching rate (normally 22.5 kHz). A shutdown input turns off both output drivers. High side current sensing protects the amplifier from shorts to ground. In addition, the half bridge output MOSFETs are protected from thermal overloads by directly sensing the temperature of the die. The 12-pin hermetic MO-127/40S power package occupies only 3 square inches of board space.

EXTERNAL CONNECTIONS

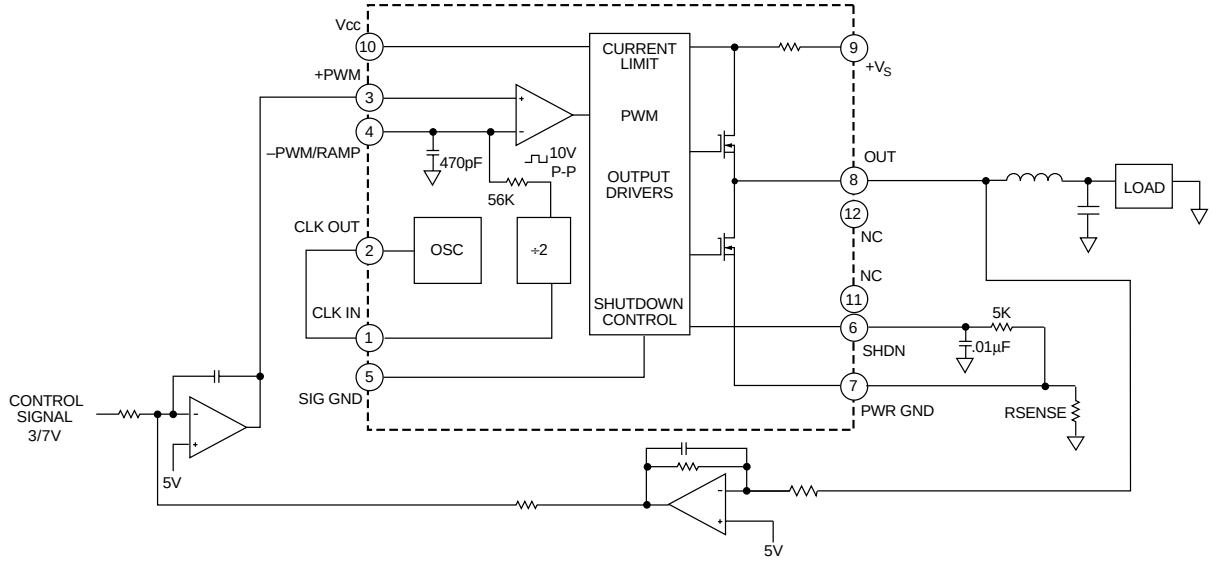


Case tied to pin 5. Allow no current in case. Bypassing of supplies is required. Package is Apex MO-127/40S. See Outline Dimensions/Packages in Apex data book.

If +PWM < RAMP/–PWM then OUT = HIGH.

*See text.

BLOCK DIAGRAM AND TYPICAL APPLICATION
PROGRAMMABLE POWER SUPPLY



ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$	500V
SUPPLY VOLTAGE, V_{CC}	16V
POWER DISSIPATION, internal	150W
TEMPERATURE, pin solder - 10s	300°C
TEMPERATURE, junction[2]	150°C
TEMPERATURE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C
INPUT VOLTAGE, +PWM	0 to +11V
INPUT VOLTAGE, –PWM	0 to +11V
INPUT VOLTAGE, I_{LIM}	0 to +10V

SPECIFICATIONS

PARAMETER	TEST CONDITIONS[2]	MIN	TYP	MAX	UNITS
CLOCK (CLK)					
CLK OUT, high level[4]	$I_{OUT} \leq 1$mA	4.8		5.3	V
CLK OUT, low level[4]	$I_{OUT} \leq 1$mA	0		.4	V
FREQUENCY		44	45	46	kHz
RAMP, center voltage			5		V
RAMP, P-P voltage			4		V
CLK IN, low level[4]		0		.9	V
CLK IN, high level[4]		3.7		5.4	V
OUTPUT					
R_{ON}	Each output driver			.48	Ω
EFFICIENCY, 10A output	V_S = 500V		97		%
SWITCHING FREQUENCY	OSC in ÷ 2	22.05	22.5	22.95	kHz
CURRENT, continuous[4]	75°C case	10			A
CURRENT, peak[4]		14			A
POWER SUPPLY					
VOLTAGE, V_S	Full temperature range	16[5]	240	500	V
VOLTAGE, V_{CC}	Full temperature range	14	15	16	V
CURRENT, V_{CC}	I_{OUT} = 0			80	mA
CURRENT, V_{CC}, shutdown				50	mA
CURRENT, V_S	No Load			90	mA
I_{LIM}/SHUTDOWN					
TRIP POINT		90		110	mV
INPUT CURRENT				100	nA
THERMAL[3]					
RESISTANCE, junction to case	Full temperature range, for each die			.83	°C/W
RESISTANCE, junction to air	Full temperature range		12		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	–25		+85	°C

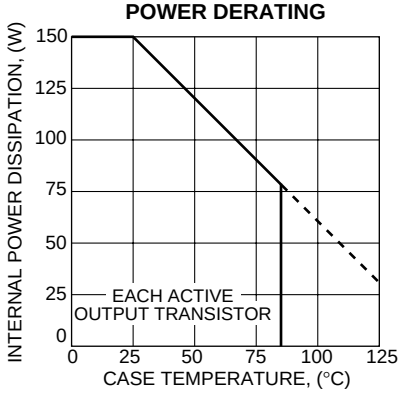
NOTES:
1. Each of the two output transistors can dissipate 150W.
2. Unless otherwise noted: T_C = 25°C, V_S, V_{CC} at typical specification.
3. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF. For guidance, refer to the heatsink data sheet.
4. Guaranteed but not tested.
5. If 100% duty cycle is not required $V_{S(MIN)}$ = 0V.

CAUTION

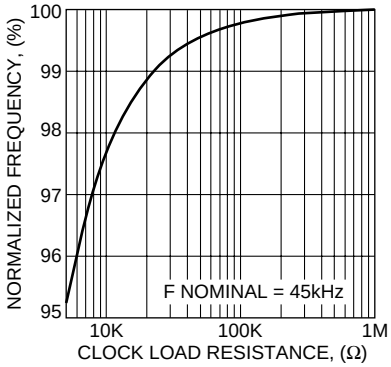
The SA16 is constructed from MOSFET transistors. ESD handling procedures must be observed.

The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

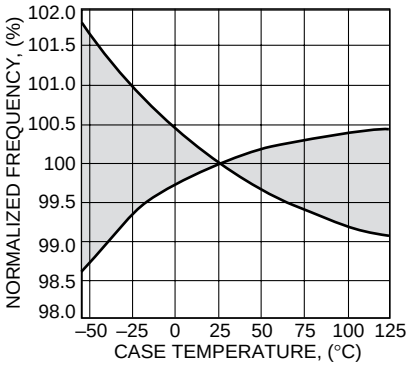
POWER DERATING



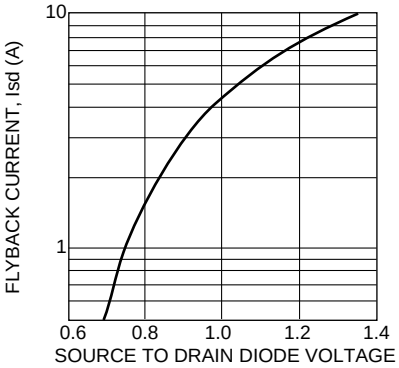
CLOCK LOADING



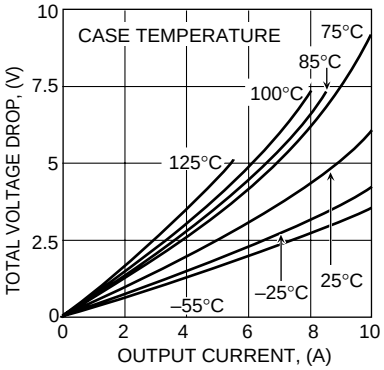
CLOCK FREQUENCY OVER TEMP



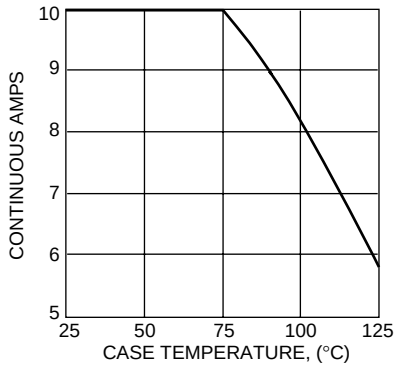
REVERSE DIODE



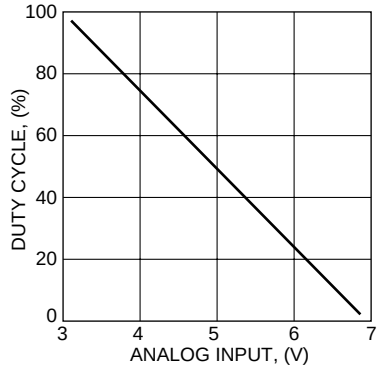
TOTAL VOLTAGE DROP



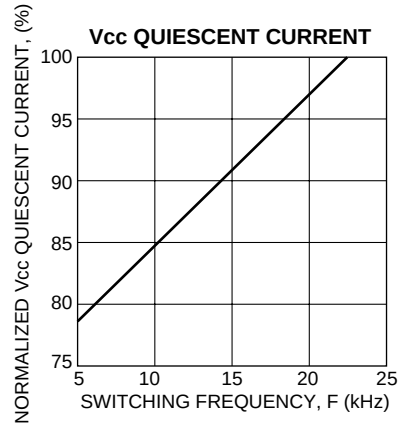
CONTINUOUS OUTPUT



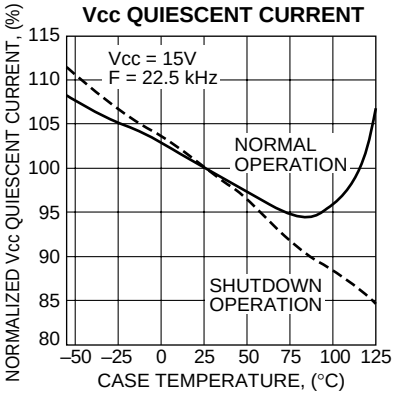
DUTY CYCLE VS ANALOG INPUT



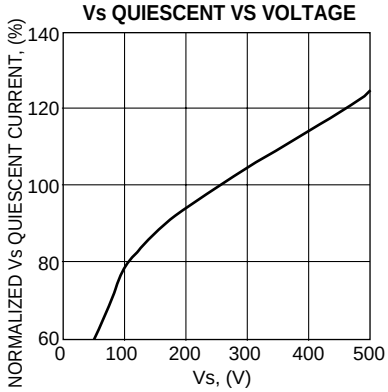
Vcc QUIESCENT CURRENT



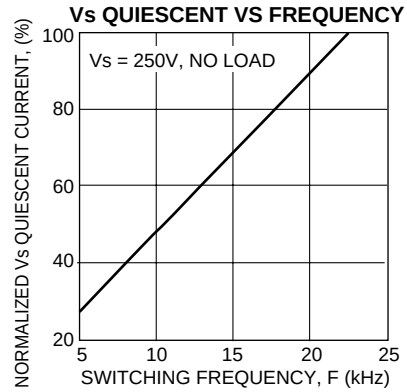
Vcc QUIESCENT CURRENT



Vs QUIESCENT VS VOLTAGE



Vs QUIESCENT VS FREQUENCY



GENERAL

Helpful information about power supplies, heatsinking and mounting can be found in the "General Operating Considerations" section of the Apex data book. For information on the package outline, heatsinks, and mounting hardware see the "Package Outlines" and "Accessories" section of the data book. Also see Application Note 30 on "PWM Basics."

CLOCK CIRCUIT AND RAMP GENERATOR

The clock frequency is internally set to a frequency of approximately 45kHz. The CLK OUT pin will normally be tied to the CLK IN pin. The clock is divided by two and applied to an RC network which produces a ramp signal at the –PWM/ RAMP pin. An external clock signal can be applied to the CLK IN pin for synchronization purposes. If a clock frequency lower than 45kHz is chosen an external capacitor must be tied to the –PWM/RAMP pin. This capacitor, which parallels an internal capacitor, must be selected so that the ramp oscillates 4 volts p-p with the lower peak 3 volts above ground.

PWM INPUTS

The half bridge driver may be accessed via the pwm input comparator. When +PWM < -PWM then OUT is HIGH. A motion control processor which generates the pwm signal can drive these pins with signals referenced to SIG GND.

PROTECTION CIRCUITS

A high side current monitor will latch off the output transistors when the high side current rises to approximately 150% of rated output. The temperature of the output transistors is also monitored. When either of the output transistors reaches approximately 165°C both are latched off. In either case, it will be necessary to remove the fault condition and recycle power to Vcc to restart the circuit. A short to +Vs can be protected against by inserting a sensing resistor into the PWR GND circuit as shown in Figure A.

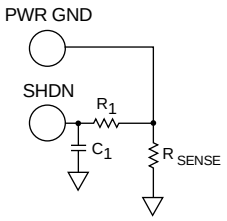


FIGURE A. PROTECTING AGAINST SHORTS TO +Vs.

In Figure A, the sense resistor inserted into the PWR GND connection is tied to the SHDN pin. When the current from a short to +Vs develops 100 mV across the sense resistor the shutdown circuit will shut off the output transistors for the remainder of the switching cycle. The SA16 will restart at the beginning of a new cycle and retest for this condition. This circuit does not test for shorts to ground. The RC circuit R_1, C_1 filters out any switching spikes and may need to be adjusted to ignore normal current spikes in the application circuit.

An external shutdown command can be mixed with the protection circuit of Figure A. In figure B a 5V shutdown command signal is divided down by R_2, R_1 to the 100 mV threshold level of the SHDN pin of the SA16. As long as the shutdown command remains high both output transistors will remain off.

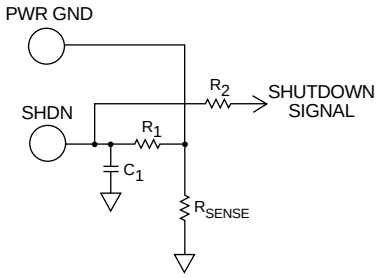


FIGURE B. ADDING SHUTDOWN CONTROL.

BYPASSING

Adequate bypassing of the power supplies is required for proper operation. Failure to do so can cause erratic and low efficiency operation as well as excessive ringing at the outputs. The Vs supply should be bypassed with at least a 1μF ceramic capacitor in parallel with another low ESR capacitor of at least 10μF per amp of output current. Capacitor types rated for switching applications are the only types that should be considered. The bypass capacitors must be physically connected directly to the power supply pins. Even one inch of lead length will cause excessive ringing at the outputs. This is due to the very fast switching times and the inductance of the lead connection. The bypassing requirements of the Vcc supply are less stringent, but still necessary. A .1μF to .47μF ceramic capacitor connected directly to the Vcc pin will suffice.

STARTUP CONDITIONS

The high side of the all N channel output half bridge circuit is driven by a bootstrap circuit and charge pump arrangement. In order for the circuit to produce a 100% duty cycle indefinitely the low side transistor must have previously been in the ON condition. This means, in turn, that if the input signal to the SA16 at startup is demanding a 100% duty cycle, the output may not follow the command and may be in a tri-state condition. The ramp signal must cross the input signal at some point to correctly determine the output state. After the ramp crosses the input signal level one time, the output state will be correct thereafter.

