4-Bit Micro-controller With LCD Driver

Features

- Low power and low voltage operation
- Powerful instruction set (150 instructions)
- Memory capacity
  - Instruction ROM capacity 4096 x 16 bits
  - Index ROM capacity 256 x 8 bits
  - Internal RAM capacity 384 or 256 x 4 bits
- Input/Output ports of up to 20 pins
- 8-level subroutine nesting
- Built-in LCD driver, 8 x 42 = 336 segments
- Built-in EL driver, frequency or melody generator
- Built-in Resistance-to-Frequency Converter
- Built-in 2-channel 6/8-bit PWM output
- Built-in key strobe function (Shared with segment pin)
- Built-in voltage doubler, halver, tripler quadrupler charge pump circuit
- Two 6-bit programmable timers with programmable clock source
- Watchdog timer
- 4 external & 3 internal interrupt resources
  - External: INT, RFC, IOA/IOC/S port, keystrobe
  - Internal: TM1, TM2, Predivider
- Dual clock operation
- HALT and STOP function

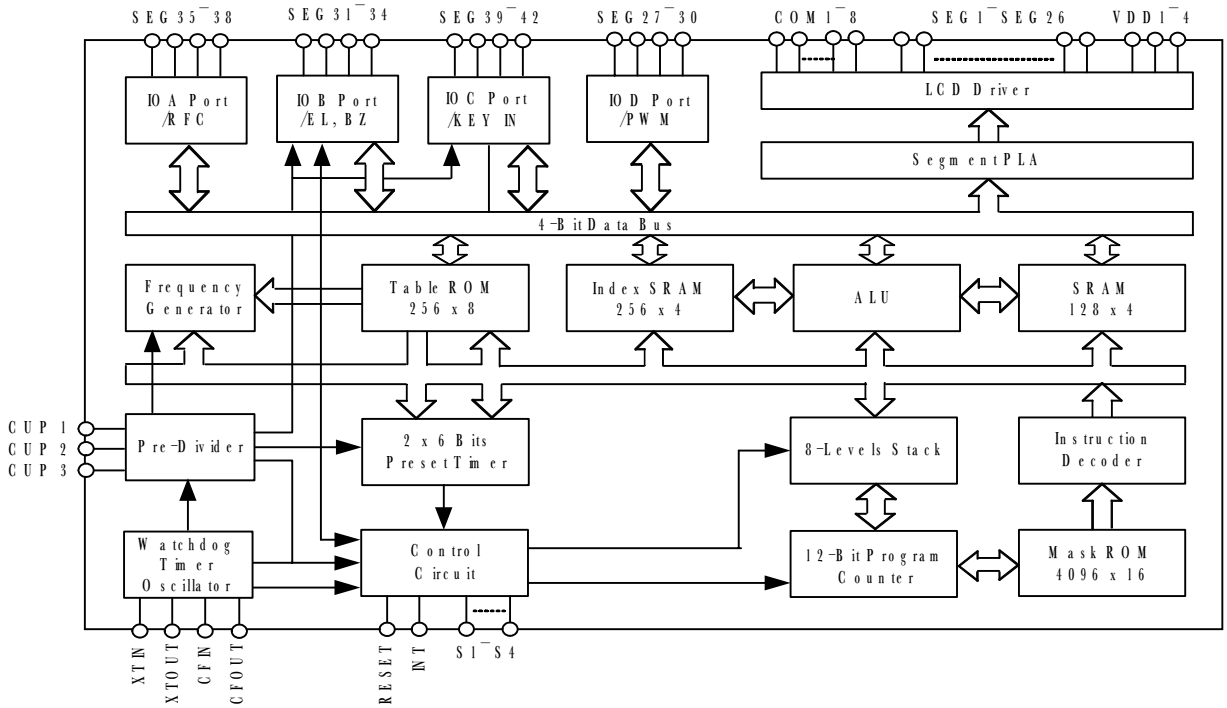
General Description

The APU429 is an embedded high performance 4-bit micro-computer with an on-chip LCD driver. It contains all the necessary functions in a single chip: 4-bit parallel processing ALU, ROM, RAM, I/O ports, timer, clock generator, dual clock, RFC, EL-light, LCD driver, look-up table, watchdog timer and keyboard scanning. The instruction set includes not only 4-bit operation and manipulation instructions but also various conditional branch instructions and LCD driver data transfer instructions which are powerful and easy to use.

The HALT function stops any internal operations other than the oscillator, divider and LCD driver in order to minimize the power dissipation.

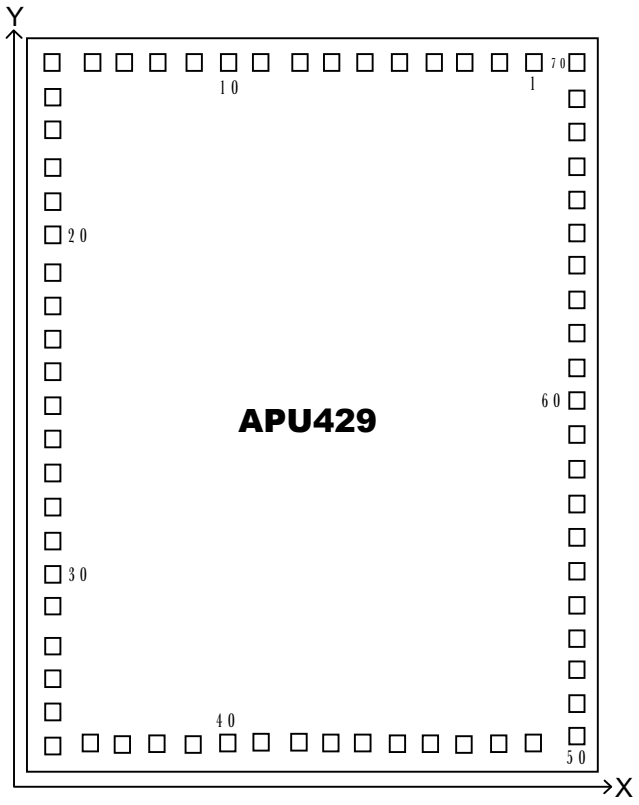
The STOP function stops all the clocks in the chip.

Block Diagram



Pad Assignment

Chip size : 2620 x 2050 μm
Pad size : 100 x 100 μm
Pad window : 90 x 90 μm
Pad pitch : min. 120 μm



Note: The substrate of die must connect to GND.

Pad Coordinates

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
1	CFIN	1971.50	2544.50	36	SEG13/KO3	75.25	75.25
2	CFOUT	1785.25	2544.50	37	SEG14/KO4	225.25	75.25
3	XTIN	1665.25	2544.50	38	SEG15/KO5	345.25	75.25
4	XTOUT	1545.25	2544.50	39	SEG16/KO6	465.25	75.25
5	BAK	1425.25	2544.50	40	SEG17/KO7	585.25	75.25
6	TESTA	1305.25	2544.50	41	SEG18/KO8	705.25	75.25
7	RESET	1185.25	2544.50	42	SEG19/KO9	825.25	75.25
8	INT	1065.25	2544.50	43	SEG20/KO10	945.25	75.25
9	S1	945.25	2544.50	44	SEG21/KO11	1065.25	75.25
10	S2	825.25	2544.50	45	SEG22/KO12	1185.25	75.25
11	S3	705.25	2544.50	46	SEG23/KO13	1305.25	75.25

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
12	S4	585.25	2544.50	47	SEG24/KO14	1425.25	75.25
13	VDD1	465.25	2544.50	48	SEG25/KO15	1545.25	75.25
14	VDD2	345.25	2544.50	49	SEG26/KO16	1665.25	75.25
15	VDD3	225.25	2544.50	50	SEG27/IOD1	1785.25	75.25
16	VDD4	75.25	2544.50	51	SEG28/IOD2	1971.50	75.25
17	CUP1	75.25	2394.50	52	SEH29/IOD3/PWM1	1971.50	225.25
18	CUP2	75.25	2274.50	53	SEH30/IOD4/PWM2	1971.50	345.25
19	CUP3	75.25	2154.50	54	SEG31/IOB1/ELC	1971.50	465.25
20	COM1	75.25	2034.50	55	SEG32/IOB2/ELP	1971.50	585.25
21	COM2	75.25	1914.50	56	SEG33/IOB3/BZB	1971.50	705.25
22	COM3	75.25	1785.25	57	SEG34/IOB4/BZ	1971.50	825.25
23	COM4	75.25	1665.25	58	SEG35/IOA1/CX	1971.50	945.25
24	SEG1	75.25	1545.25	59	SEG36/IOA2/RR	1971.50	1065.25
25	SEG2	75.25	1425.25	60	SEG37/IOA3/RT	1971.50	1185.25
26	SEG3	75.25	1305.25	61	SEG38/IOA4/RH	1971.50	1305.25
27	SEG4	75.25	1185.25	62	SEG39/IOC1/KI1	1971.50	1425.25
28	SEG5	75.25	1065.25	63	SEG40/IOC2/KI2	1971.50	1545.25
29	SEG6	75.25	945.25	64	SEG41/IOC3/KI3	1971.50	1665.25
30	SEG7	75.25	825.25	65	SEG42/IOC4/KI4	1971.50	1785.25
31	SEG8	75.25	705.25	66	COM5	1971.50	1905.25
32	SEG9	75.25	585.25	67	COM6	1971.50	2034.50
33	SEG10	75.25	465.25	68	COM7	1971.50	2154.50
34	SEG11/KO1	75.25	345.25	69	COM8	1971.50	2274.50
35	SEG12/KO2	75.25	225.25	70	GND	1971.50	2394.50
Chip size : 2620 x 2050 μm							

Pad Descriptions

Pad Name	I/O	Description
BAK		Positive back-up voltage. In Li mode, connects a 0.1μ capacitance to GND.
VDD1 VDD2 VDD3 VDD4		LCD drive voltage and positive supply voltage. While in Ag mode, connects +1.5V to VDD1. While in Li/ExtV mode, connects +3.0V to VDD2.
RESET	I	Input pin for LSI reset signal. With Internal pull-down resistor.
INT	I	Input pin for external INT request signal. Falling edge or rising edge triggered by mask option. Internal pull-down or pull-up resistor or floatting to be selected by mask option. TESTA I Test signal input pin, internal pull-down resistor.
TESTA	I	Test signal input pin.
CUP1 CUP2 CUP3	O	Switching pins for supplying the LCD driving voltage to the VDD1, 2, 3, 4 pins. Connects the CUP1, CUP2 and CUP3 pins with a nonpolarized electronic capacitor if 1/2, 1/3 or 1/4 bias mode has been selected. In the STATIC mode, these pins should be open.

Pad Name	I/O	Description
XTIN XTOUT	I O	Time based counter frequency (Clock specified. LCD alternating frequency. Alarm signal frequency.) or system clock oscillation. 32KHz crystal oscillator. Oscillation stops at the execution of STOP instruction.
CFIN CFOUT	I O	System clock oscillation. Connected with ceramic resonator. Connected with RC oscillation circuit. Oscillation stops at the execution of STOP or SLOW instruction.
COM1~8	O	Output pins for supplying voltage to drive the common pins of the LCD panel.
SEG1~10	O	Output pins for LCD panel segment.
SEG11~26/KO1~16	O	Output pins for LCD panel segment. Key strobe function, share pins as key scan output.
SEG27~42	O	Output pins for LCD panel segment.
IOA1~4	I/O	Input/Output port A, can use software to define the internal pull-low resistor and chattering clock in order to reduce input bounce and generate an interrupt. This port shares pins with SEG35~38 and is set by mask option. This port also shares pins with CC, RR, RT and RH, and is set by mask option.
IOB1~4	I/O	Input/Output port B. IOB port shares pins with SEG31~34, and is set by mask option. This port also shares pins with ELC, ELP, BZB and BZ, and is set by mask option.
IOC1~4	I/O	Input/Output port C, can use software to define internal pull-low/low-level hold resistor and chattering clock in order to reduce input bounce and generate an interrupt or keyboard scanning function with ELC, ELP, BZB and BZ, and is set by mask option.
IOD1~4	I/O	Input/Output port D. This port shares pins with SEG27~30 and is set by mask option. IOD3, 4 shares pins with PWM1, 2 and is set by mask option.
S1~4	I	Input ports by mask option to internal pull-low/low-level hold resistor and chattering clock in order to reduce input bounce and generate an interrupt or HALT or STOP release.
KI1~4	I	Key scan input, this port shares pins with IOC1~4 and is set by mask option.
RFC CC RR RT RH	I O O O	1 input pin and 3 output pins for RFC application. This port shares pins with SEG35~38 and is set by mask option. This port shares pins with IOA1~4 and is set by mask option.
EL ELC ELP	O O	Output port for EL-light. This port shares pins with SEG31, 32 and is set by mask option. This port shares pins with IOB1, 2 and is set by mask option.
ALM BZB BZ	O	Output port for alarm, frequency or melody generator. This port shares pins with IOB3, 4 and is set by mask option.
PWM1, 2	O	6/8-Bit PWM output; set by mask option.
GND		Negative supply voltage.

Absolute Maximum Rating

Ta = 0 to 70℃ GND=0V

Name	Symbol	Rating	Unit
Maximum Supply Voltage	V_{DD1}	-0.3 ~ +5.5	V
	V_{DD2}	-0.3 ~ +5.5	V
	V_{DD3}	-0.3 ~ +8.5	V
	V_{DD4}	-0.3 ~ +8.5	V
Maximum Input Voltage	V_{IN}	-0.3 to $V_{DD1/2}$+0.3	V
Maximum Output Voltage	V_{OUT1}	-0.3 to $V_{DD1/2}$+0.3	V
	V_{OUT2}	-0.3 to V_{DD3}+0.3	V
Maximum Operating Temperature	t_{OPG}	0 to +70	℃
Maximum Storage Temperature	t_{STG}	-25 to +125	℃

Allowable operating conditions

Ta = 0 to 70℃ GND=0V

Name	Symbol	Condition	Min.	Max.	Unit
Supply Voltage	V_{DD1}		1.2	5.25	V
	V_{DD2}		2.4	5.25	V
	V_{DD3}		2.4	8.0	V
	V_{DD4}		2.4	8.0	V
Oscillator Start-up Voltage	V_{DDB}	Crystal Mode	1.3		V
Oscillator Sustain Voltage	V_{DDB}	Crystal Mode	1.2		V
Supply Voltage	V_{DD1}	Ag Mode	1.2	1.65	V
Supply Voltage	V_{DD2}	EXT-V, Li Mode	2.4	5.25	V
Input ″H″ Voltage	V_{IH1}	Ag Battery Mode	$V_{DD1-0.7}$	$V_{DD1+0.7}$	V
Input ″L″ Voltage	V_{IL1}	Li Battery Mode	-0.7	0.7	V
Input ″H″ Voltage	V_{IH2}		$V_{DD2-0.7}$	$V_{DD2+0.7}$	V
Input ″L″ Voltage	V_{IL2}		-0.7	0.7	V
Input ″H″ Voltage	V_{IH3}	OSCIN at Ag Battery Mode	$0.8V_{DD1}$	V_{DD1}	V
Input ″L″ Voltage	V_{IL3}		0	$0.2V_{DD1}$	V
Input ″H″ Voltage	V_{IH4}	OSCIN at Li Battery Mode	$0.8V_{DD2}$	V_{DD2}	V
Input ″L″ Voltage	V_{IL4}		0	$0.2V_{DD2}$	V
Input ″H″ Voltage	V_{IH5}	CFIN at Li Battery or EXT-V Mode	$0.8V_{DD2}$	V_{DD2}	V
Input ″L″ Voltage	V_{IL5}		0	$0.2V_{DD2}$	V
Input ″H″ Voltage	V_{IH6}	RC Mode	$0.8V_{DDO}$	V_{DDO}	V
Input ″L″ Voltage	V_{IL6}		0	$0.2V_{DDO}$	V
Operating Freq.	f_{OPG1}	Crystal Mode	32	3580	kHz
	f_{OPG2}	External RC Mode	32	1000	kHz
	f_{OPG3}	CF Mode	1000	3580	kHz

Electrical Characteristics

Input resistance

Name	Symbol	Condition	Min.	Typ.	Max.	Unit
″L″-Level Hold t_R (IOC)	R_{IIH1}	V_I=0.2V_{DD1}, #1	10	40	100	kΩ
	R_{IIH2}	V_I=0.2V_{DD2}, #2	10	40	100	kΩ
	R_{IIH3}	V_I=0.2V_{DD2}, #3	5	20	50	kΩ
IOC/IOA Pull-Down t_R	R_{MSD1}	V_I=V_{DD1}, #1	200	500	1000	kΩ
	R_{MSD2}	V_I=V_{DD2}, #2	200	500	1000	kΩ
	R_{MSD3}	V_I=V_{DD3}, #3	100	250	500	kΩ
INT Pull-Up t_R	R_{INTU1}	V_I=V_{DD1}, #1	200	500	1000	kΩ
	R_{INTU2}	V_I=V_{DD2}, #2	200	500	1000	kΩ
	R_{INTU3}	V_I=V_{DD3}, #3	100	250	500	kΩ
INT Pull-Down t_R	R_{INTD1}	V_I=GND, #1	200	500	1000	kΩ
	R_{INTD2}	V_I=GND, #2	200	500	1000	kΩ
	R_{INTD3}	V_I=GND, #3	100	250	500	kΩ
RES Pull-Down t_R	R_{RES1}	V_I=GND or V_{DD1}, #1	5	20	50	kΩ
	R_{RES2}	V_I=GND or V_{DD2}, #2	5	20	50	kΩ
	R_{RES3}	V_I=GND or V_{DD2}, #3	5	20	50	kΩ

Note: #1: V_{DD1}= 1.2V (Ag), #2: V_{DD2}= 2.4V (Li), #3: V_{DD2}= 4V (Ext-V).

DC output characteristics

Name	Symbol	Condition	For	Min.	Typ.	Max.	Unit
Output ″H″ Voltage	V_{OH1a}	I_{OH}=-10μA, #1	SEG1~26	0.8	0.9	1.0	V
	$V_{OH2\ a}$	I_{OH}=-50μA, #2		1.5	1.8	2.1	V
	$V_{OH3\ a}$	I_{OH}=-200μA, #3		2.5	3	3.5	V
Output ″L″ Voltage	$V_{OL1\ a}$	I_{OL}=20μA, #1		0.2	0.3	0.4	V
	$V_{OL2\ a}$	I_{OL}=100μA, #2		0.3	0.6	0.9	V
	$V_{OL3\ a}$	I_{OL}=400μA, #3		0.5	1	1.5	V
Output ″H″ Voltage	V_{OH1c}	I_{OH}=-200μA, #1	SEG27~42 IOA, B, C, D	0.8	0.9	1.0	V
	V_{OH2c}	I_{OH}=-1mA, #2		1.5	1.8	2.1	V
	V_{OH3c}	I_{OH}=-3mA, #3		2.5	3	3.5	V
Output ″L″ Voltage	V_{OL1c}	I_{OL}=400μA, #1		0.2	0.3	0.4	V
	V_{OL2c}	I_{OL}=2mA, #2		0.3	0.6	0.9	V
	V_{OL3C}	I_{OL}=6mA, #3		0.5	1	1.5	V

Note: #1: V_{DD1}= 1.2V (Ag), #2: V_{DD2}= 2.4V (Li), #3: V_{DD2}= 4V (Ext-V).

Segment driver output characteristics

Name	Symbol	Condition	For	Min.	Typ.	Max.	Unit
Static display mode							
Output ″H″ Voltage	V_{OH1d}	I_{OH}=-1μA, #1	SEG-n	1.0			V
	V_{OH2d}	I_{OH}=-1μA, #2		2.2			V
	V_{OH3d}	I_{OH}=-1μA, #3		3.8			V
Output ″L″ Voltage	V_{OL1d}	I_{OL}=1μA, #1				0.2	V
	V_{OL2d}	I_{OL}=1μA, #2				0.2	V
	V_{OL3d}	I_{OL}=1μA, #1				0.2	V
Output ″H″ Voltage	V_{OH1e}	I_{OH}=-10μA, #1	COM-n	1.0			V
	V_{OH2e}	I_{OH}=-10μA, #2		2.2			V
	V_{OH3e}	I_{OH}=-10μA, #3		3.8			V
Output ″L″ Voltage	V_{OL1e}	I_{OL}=10μA, #1				0.2	V
	V_{OL2e}	I_{OL}=10μA, #2				0.2	V
	V_{OL3e}	I_{OL}=10μA, #3				0.2	V
1/2 bias display mode							
Output ″H″ Voltage	V_{OH12f}	I_{OH}=-1μA, #1, #2	SEG-n	2.2			V
	V_{OH3f}	I_{OH}=-1μA, #3		3.8			V
Output ″L″ Voltage	V_{OL12f}	I_{OL}=1μA, #1, #2				0.2	V
	V_{OL3f}	I_{OL}=1μA, #3				0.2	V
Output ″H″ Voltage	V_{OH12g}	I_{OH}=-10μA, #1, #2	COM-n	2.2			V
	V_{OH3g}	I_{OH}=-10μA, #3		3.8			V
Output ″M″ Voltage	V_{OM12g}	$I_{OI/H}$=±10μA, #1, #2		1.0		1.4	V
	V_{OM3g}	$I_{OI/H}$=±10μA, #3		1.8		2.2	V
Output ″L″ Voltage	V_{OL12g}	I_{OL}=10μA, #1, #2				0.2	V
	V_{OL3g}	I_{OL}=10μA, #3				0.2	V
1/3 bias display mode							
Output ″H″ Voltage	V_{OH12i}	I_{OH}=-1μA, #1, #2	SEG-n	3.4			V
	V_{OH3i}	I_{OH}=-1μA, #3		5.8			V
Output ″M1″ Voltage	V_{OM12i}	$I_{OI/H}$=±10μA, #1, #2		1.0		1.4	V
	V_{OM13i}	$I_{OI/H}$=±10μA, #3		1.8		2.2	V
Output ″M2″ Voltage	V_{OM22i}	$I_{OI/H}$=±10μA, #1, #2		2.2		2.6	V
	V_{OM23i}	$I_{OI/H}$=±10μA, #13		3.8		4.2	V
Output ″L″ Voltage	V_{OL12i}	I_{OL}=1μA, #1, #2				0.2	V
	V_{OL3i}	I_{OL}=1μA, #3				0.2	V
Output ″H″ Voltage	V_{OH12j}	I_{OH}=-10μA, #1, #2	COM-n	3.4			V
	V_{OH3j}	I_{OH}=-10μA, #3		5.8			V
Output ″M1″ Voltage	V_{OM12j}	$I_{OI/H}$=±10μA, #1, #2		1.0		1.4	V
	V_{OM13j}	$I_{OI/H}$=±10μA, #3		1.8		2.2	V
Output ″M2″ Voltage	V_{OM22j}	$I_{OI/H}$=±10μA, #1, #2		2.2		2.6	V
	V_{OM23j}	$I_{OI/H}$=±10μA, #3		3.8		4.2	V
Output ″L″ Voltage	V_{OL12j}	I_{OL}=10μA, #1, #2				0.2	V
	V_{OL3j}	I_{OL}=10μA, #3				0.2	V

Note: #1: V_{DD1}= 1.2V (Ag), #2: V_{DD2}= 2.4V (Li), #3: V_{DD2}= 4V (Ext-V).

Functional Description

SRAM

The 256 x 4 bits index SRAM and 128 x 4 bits data SRAM are 2 separate regions.

Index ROM

The 256 x 8 bits index ROM can be used as a 4-bit mode or an 8-bit mode.

I/O ports

The IOA port can be selected by software separately as input or output, and with/without internal pull-low and different chattering clocks in order for HALT release/ interrupt trigger to reduce the bounce of key_scan:

PH6: 512Hz PH8:128Hz PH10: 32Hz

The pull-low of the IOA will be masked off for those pins defined as output pins.

The IOA port can be used as a pseudo serial output port.

The IOB port can be selected by software separately as input or output.

The IOC port can be selected by software separately as input or output, and with/without internal pull-low and different chattering clocks in order for HALT release/ interrupt trigger to reduce the bounce of key_scan.

The IOD port can be selected by software separately as input or output.

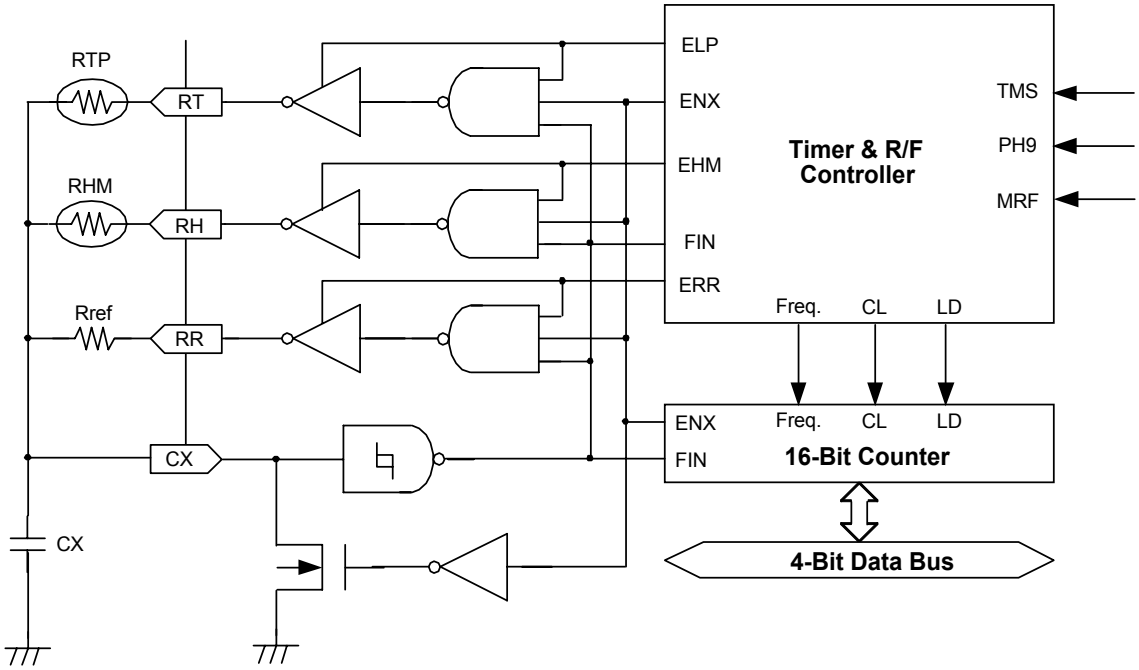
The IOD port can be used as a pseudo serial output port.

The initial state of all I/O ports is standard input state and IOA, C have pull-low device.

Before setting some pins from input to output, you can execute the output function to ensure their output value. The S ports are input pins that contain pull-low. The L_L_H resistor can be selected by mask option and different chattering clocks in the same manner as the IOA, C ports.

Resistor to frequency converter

We use an RC oscillation circuit and a 16-bit counter to calculate the relative resistance of temperature and humidity sensor. The diagram is shown below:



There are two types of methodology for measuring the input frequency: first, set FIN (i.e. CX) as the clock input, using timer 2 as interval control or using software to directly control the interval. Second, if the FIN (CX) frequency is too low, either because of a poor resolution for a fixed interval or a longer interval for better

resolution but with a longer read-out rate (for example: 10 seconds per read-out), you can switch the measure mode in order to set FIN (CX) as interval control (it will enable the counter from first FIN rising edge to the next rising edge, then will generate an interrupt) and use FREQ (internal frequency generator output) as clock input, hence you can count the interval of CX.

To measure the resistor value of the temperature and humidity sensor, we must first measure the frequency of Rref, then the frequency of sensor.

Fref= K/Rref CX and
Fsensor= K/Rsensor CX, hence
Rsensor= Rref * Freq/Fsensor.

Where K is a coefficient for RC-oscillation and will be a constant in a short time period.

Keyboard scanning function

SEG11~26 shares the keyboard scanning output, the output of the keyboard scanning is a P open-drain to VDDO (positive power supply) and all other SEGs and COMs are in Hi-z state during this period. This will minimize the effect of the LCD output.

The segment 11-26 also could be used as keyscan output and LCD still could be displayed with only slightly affected.

SPK 00b5 b4 b3 b2 b1 b0.

b5: 1 will disable key-scan output.

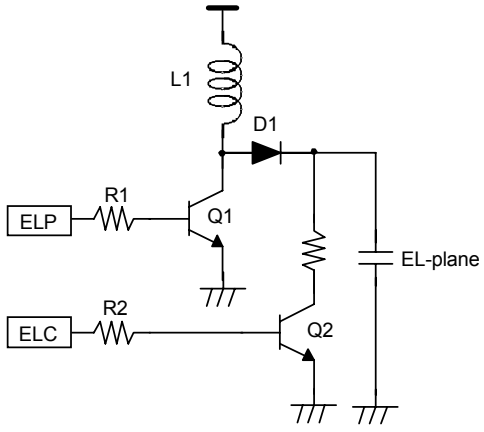
b4: 1 will set all keyscan output as high, if b5=0.

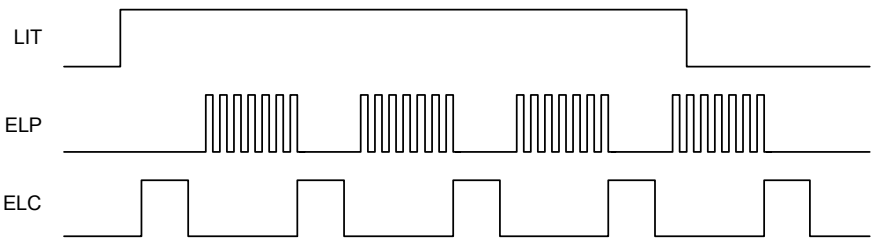
b3~b0: will set the corresponding segment output as 1, if b5=0 and b4=0.

During power on, LCD off, STOP condition. All the common & segment output will be the chips supply power.

EL-light

Set the ELC and ELP clock and duty cycle by ELC X instruction, then turn on and off the ELC and ELP output by SF X and RF X instruction. With external transistor, diode, inductor and resistor, we can pump the Elpanel to AC 100~250V.





While the light is turned on, the ELC will turn on before the ELP, but when the light is turned off, the ELP and ELC will turn off after the next falling edge of the ELC to make sure no voltage is left on the EL- panel.

Timer

The 6-bit programmable timer can select PH3/PH9/PH15/FREQ (timer 2 can also select PH5/PH7/PH11/PH13 by TM2X instruction) as the clock source. When it underflows, the HALT release signal is generated.

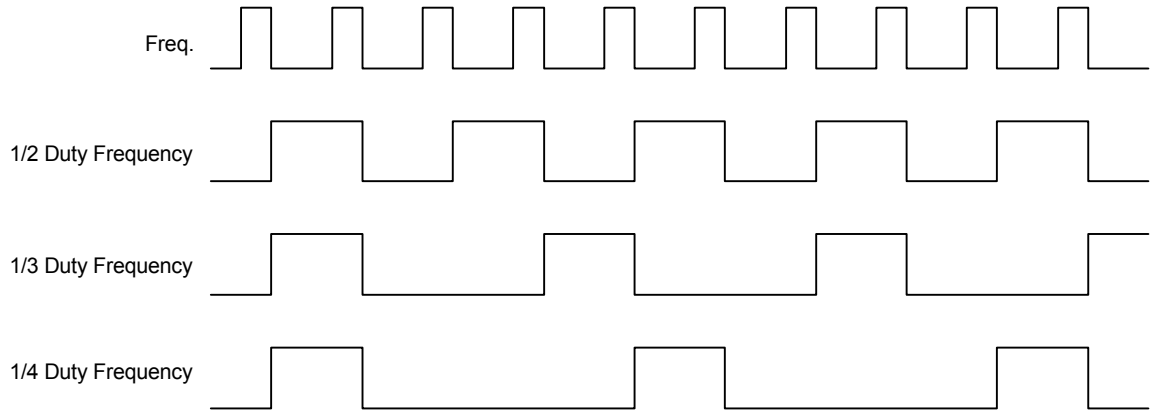
Predivider

The predivider is a 15-stage counter that uses PH0 as the clock source. The output of T-F/F is changed when the input signal is changed from H to L. PH11~15 are reset to L when PLC 100H instruction is executed, or power-on or external reset is used. When PH14 is changed from H to L, the HALT release signal is generated.

Alarm/frequency/melody

There is an 8-bit programmable counter and an 8-bit envelope control for alarm, frequency or melody output from BZ/BZB.

The frequency counter can use software to select 1/2 duty, 1/3 duty or 1/4 duty drive mode.



INT function

The INT pin can be selected by mask option as pull-high/pull-low or none, and rising edge/falling edge trigger.

Watchdog timer

The watchdog timer automatically generates a device reset when it overflows. The interval of overflow is 8/64/512 x PH10 (set by mask option). You can use software to enable and disable this function. The watchdog enable flag will be disabled by power-on reset or reset-pin reset condition, but cannot be disabled by watchdog reset itself.

HALT function

The HALT instruction will disable all clocks except the predivider, timer, frequency counter, PWM, EL-light generator and chattering clock to minimize the operating current.

STOP function

The STOP instruction will disable all clocks to minimize the standby current, so only two external factors (INT, IOA/IOC/S port, keyscan) can release the STOP condition.

Instruction Table (Total 150 instructions)

Instruction	Machine Code	Function	Flag/Remark
NOP	0000 0000 0000 0000	No Operation	
LCT Lz, Ry	0000 001Z ZZZZ YYYY	Lz ← { 7SEG ← Ry}	
LCB Lz, Ry	0000 010Z ZZZZ YYYY	Lz ← { 7SEG ← Ry}	
LCP Lz, Ry	0000 011Z ZZZZ YYYY	Lz ← Ry , AC	
LCD Lz, @HL	0000 100Z ZZZZ 0000	Lz ← T@HL	
LCT Lz, @HL	0000 100Z ZZZZ Z-01	Lz {7SEG @HL	

Instruction	Machine Code	Function	Flag/Remark
LCB Lz, @HL	0000 100Z ZZZZ Z-10	Lz {7SEG @HL	
LCP Lz, @HL	0000 100Z ZZZZ Z-11	Lz @HL, AC	
OPA Rx	0000 1010 0XXX XXXX	Port(A) ← Rx	
OPAS Rx, D	0000 1011 DXXX XXXX	A1, 2, 3, 4 ← Rx0, Rx1, D, Pulse	
OPB Rx	0000 1100 0XXX XXXX	Port(B) ← Rx	
OPC Rx	0000 1101 0XXX XXXX	Port(C) ← Rx	
OPD Rx	0000 1110 0XXX XXXX	Port(D) ← Rx	
OPDS Rx	0000 1111 DXXX XXXX	D1, 2, 3, 4 ← Rx0, Rx1, D, Pulse	
FRQ Rx, D	0001 00DD 0XXX XXXX	FREQ ← Rx, AC DD=00: 1/4 Duty DD=01: 1/3 Duty DD=10: 1/2 Duty DD=11: 1/1 Duty	
FRQ D,@HL	0001 01DD 0000 0000	FREQ ← T@HL	
FRQX D,X	0001 10DD XXXX XXXX	FREQ ← X	
MVL Rx	0001 1100 0XXX XXXX	L ← Rx	
MVH Rx	0001 1101 0XXX XXXX	H ← Rx	
MPW1 Rx	0001 1110 0XXX XXXX	PWM1 ← Rx , AC	
MPW2 Rx	0001 1111 0XXX XXXX	PWM2 ← Rx , AC	
ADC Rx	0010 0000 0XXX XXXX	AC ← Rx+AC+CF	CF
ADC @HL	0010 0000 1000 0000	AC ← @HL+AC+CF	CF
ADC* Rx	0010 0001 0XXX XXXX	AC, Rx ← Rx+AC+CF	CF
ADC* @HL	0010 0001 1000 0000	AC, @HL ← @HL+AC+CF	CF
SBC Rx	0010 0010 0XXX XXXX	AC ← Rx+ACB+CF	CF
SBC @HL	0010 0010 1000 0000	AC ← @HL+ACB+CF	CF
SBC* Rx	0010 0011 0XXX XXXX	AC, Rx ← Rx+ACB+CF	CF
SBC* @HL	0010 0011 1000 0000	AC, @HL ← @HL+ACB+CF	CF
ADD Rx	0010 0100 0XXX XXXX	AC ← Rx+AC	CF
ADD @HL	0010 0100 1000 0000	AC ← @HL+AC	CF
ADD* Rx	0010 0101 0XXX XXXX	AC,Rx ← Rx+AC	CF
ADD* @HL	0010 0101 1000 0000	AC, @HL ← @HL+AC	CF
SUB Rx	0010 0110 0XXX XXXX	AC ← Rx+ACB+1	CF
SUB @HL	0010 0110 1000 0000	AC ← @HL+ACB+1	CF
SUB* Rx	0010 0111 0XXX XXXX	AC, Rx ← Rx+ACB+1	CF
SUB* @HL	0010 0111 1000 0000	AC,@HL ← @HL+ACB+1	CF
ADN Rx	0010 1000 0XXX XXXX	AC ← Rx+AC	
ADN @HL	0010 1000 1000 0000	AC ← @HL+AC	
ADN* Rx	0010 1001 0XXX XXXX	AC, Rx ← Rx+AC	
ADN* @HL	0010 1001 1000 0000	AC,@HL ← @HL+AC	
AND Rx	0010 1010 0XXX XXXX	AC ← Rx AND AC	
AND @HL	0010 1010 1000 0000	AC ← @HL AND AC	

Instruction	Machine Code	Function	Flag/Remark
AND* Rx	0010 1011 0XXX XXXX	AC, Rx ← Rx AND AC	
AND* @HL	0010 1011 1000 0000	AC,@HL ← @HL AND AC	
EOR Rx	0010 1100 0XXX XXXX	AC ← Rx EOR AC	
EOR @HL	0010 1100 1000 0000	AC ← @HL EOR AC	
EOR* Rx	0010 1101 0XXX XXXX	AC, Rx ← Rx EOR AC	
EOR* @HL	0010 1101 1000 0000	AC,@HL ← @HL EOR AC	
OR Rx	0010 1110 0XXX XXXX	AC ← Rx OR AC	
OR @HL	0010 1110 1000 0000	AC ← @HL OR AC	
OR* Rx	0010 1111 0XXX XXXX	AC, Rx ← Rx OR AC	
OR* @HL	0010 1111 1000 0000	AC,@HL ← @HL OR AC	
ADCI Ry,D	0011 0000 DDDD YYYY	AC ← Ry+D+CF CF	
ADCI* Ry,D	0011 0001 DDDD YYYY	AC, Ry ← Ry+D+CF	CF
SBCI Ry,D	0011 0010 DDDD YYYY	AC ← Ry+DB+CF	CF
SBCI* Ry,D	0011 0011 DDDD YYYY	AC, Ry ← Ry+DB+CF	CF
ADDI Ry,D	0011 0100 DDDD YYYY	AC ← Ry+D	CF
ADDI* Ry,D	0011 0101 DDDD YYYY	AC, Ry ← Ry+D	CF
SUBI Ry,D	0011 0110 DDDD YYYY	AC ← Ry+DB+1	CF
SUBI* Ry,D	0011 0111 DDDD YYYY	AC, Ry ← Ry+DB+1	CF
ADNI Ry,D	0011 1000 DDDD YYYY	AC ← Ry+D	
ADNI* Ry,D	0011 1001 DDDD YYYY	AC, Ry ← Ry+D	
ANDI Ry,D	0011 1010 DDDD YYYY	AC ← Ry AND D	
ANDI* Ry,D	0011 1011 DDDD YYYY	AC, Ry ← Ry AND D	
EORI Ry,D	0011 1100 DDDD YYYY	AC ← Ry EOR D	
EORI* Ry,D	0011 1101 DDDD YYYY	AC, Ry ← Ry EOR D	
ORI Ry,D	0011 1110 DDDD YYYY	AC ← Ry OR D	
ORI* Ry,D	0011 1111 DDDD YYYY	AC, Ry ← Ry OR D	
INC* Rx	0100 0000 0XXX XXXX	AC, Rx ← Rx+1	CF
INC* @HL	0100 0000 1000 0000	AC, @HL ← @HL+1	CF
DEC* Rx	0100 0001 0XXX XXXX	AC, Rx ← Rx-1	CF
DEC* @HL	0100 0001 1000 0000	AC, @HL ← @HL-1	CF
IPA Rx	0100 0010 0XXX XXXX	AC, Rx ← Port(A)	
IPB Rx	0100 0100 0XXX XXXX	AC, Rx ← Port(B)	
IPS Rx	0100 0110 0XXX XXXX	AC, Rx ← Port(S)	
IPC Rx	0100 0111 0XXX XXXX	AC, Rx ← Port(C)	
IPD Rx	0100 1000 0XXX XXXX	AC, Rx ← Port(D)	
MAF Rx	0100 1010 0XXX XXXX	AC,Rx ← STS1	B3: CF B2: ZERO B1: (No use) B0: (No use)

Instruction	Machine Code	Function	Flag/Remark
MSB Rx	0100 1011 0XXX XXXX	AC,Rx ← STS2	B3: (No use) B2: SCF2(HRx) B1: SCF1(CPT) B0: BCF
MSC Rx	0100 1100 0XXX XXXX	AC,Rx ← STS3	B3: SCF7(PDV) B2: PH15 B1: SCF5(TMR1) B0: SCF4(INT)
MCX Rx	0100 1101 0XXX XXXX	AC,Rx ← STS3X	B3: SCF9(RFC) B2: SCF0(APT) B1: SCF6(TMR2) B0: (No use)
MSD Rx	0100 1110 0XXX XXXX	AC,Rx ← STS4	B3: (No use) B2: RFOVF B1: WDF B0: CSF
SR0 Rx	0101 0000 0XXX XXXX	ACn, Rxn ← Rx(n+1) AC3, Rx3 ← 0	
SR1 Rx	0101 0001 0XXX XXXX	ACn, Rxn ← Rx(n+1) AC3, Rx3 ← 1	
SL0 Rx	0101 0010 0XXX XXXX	ACn, Rxn ← Rx(n-1) AC0, Rx0 ← 0	
SL1 Rx	0101 0011 0XXX XXXX	Can, Rxn ← Rx(n-1) AC0, Rx0 ← 1	
DAA	0101 0100 0000 0000	AC ← BCD(AC)	CF
DAA* Rx	0101 0101 0XXX XXXX	AC, Rx ← BCD(AC)	CF
DAA* @HL	0101 0101 1000 0000	AC, @HL ← BCD(AC)	CF
DAS	0101 0110 0000 0000	AC ← BCD(AC)	CF
DAS* Rx	0101 0111 0XXX XXXX	AC, Rx ← BCD(AC)	CF
DAS* @HL	0101 0111 1000 0000	AC, @HL ← BCD(AC)	CF
LDS Rx,D	0101 1DDD DXXX XXXX	AC, Rx ← D	
LDH Rx,@HL	0110 0000 0XXX XXXX	AC, Rx ← H(T@HL)	
LDH* Rx,@HL	0110 0001 0XXX XXXX	AC, Rx ← H(T@HL) HL ← HL + 1	
LDL Rx,@HL	0110 0010 0XXX XXXX	AC, Rx ← L(T@HL)	
LDL* Rx,@HL	0110 0011 0XXX XXXX	AC, Rx ← L(T@HL) HL ← @HL + 1	
MRF1 Rx	0110 0100 0XXX XXXX	AC,Rx ← RFC3-0	
MRF2 Rx	0110 0101 0XXX XXXX	AC,Rx ← RFC7-4	
MRF3 Rx	0110 0110 0XXX XXXX	AC,Rx ← RFC11-8	
MRF4 Rx	0110 0111 0XXX XXXX	AC,Rx ← RFC15-12	
STA Rx	0110 1000 0XXX XXXX	Rx ← AC	
STA @HL	0110 1000 1000 0000	@HL ← AC	

Instruction	Machine Code	Function	Flag/Remark
LDA Rx	0110 1100 0XXX XXXX	AC ← Rx	
LDA @HL	0100 1100 1000 0000	AC ← @HL	
MRA Rx	0110 1101 0XXX XXXX	CF ← Rx3	
MRW @HL,Rx	0110 1110 0XXX XXXX	AC,@HL ← Rx	
MWR Rx,@HL	0110 1111 0XXX XXXX	AC,Rx ← @HL	
MRW Ry,Rx	0111 0YYY YXXX XXXX	AC,Ry ← Rx	
MWR Rx,Ry	0111 1YYY YXXX XXXX	AC,Rx←Ry	
JB0 X	1000 0XXX XXXX XXXX	PC ← X	if AC0 = 1
JB1 X	1000 1XXX XXXX XXXX	PC ← X	if AC1 = 1
JB2 X	1001 0XXX XXXX XXXX	PC ← X	if AC2 = 1
JB3 X	1001 1XXX XXXX XXXX	PC ← X	if AC3 = 1
JNZ X	1010 0XXX XXXX XXXX	PC ← X	if AC ≠ 0
JNC X	1010 1XXX XXXX XXXX	PC ← X	if CF = 0
JZ X	1011 0XXX XXXX XXXX	PC ← X	if AC0 = 0
JC X	1011 1XXX XXXX XXXX	PC ← X	if CF = 1
CALL X	1100 0XXX XXXX XXXX	STACK ← PC+1 PC ← X	
JMP X	1101 0XXX XXXX XXXX	PC ← X	
RTS	1101 1000 0000 0000	PC ← STACK	CALL Return
SCC X	1101 1001 0XXX XXXX	X6 = 1: Cfq = BCLK X6 = 0: Cfq = PH0 X5 = 1: Cpw = BCLK X5 = 1: Cpw = PH0 X4, 3 = 1X: Set P(A) X4, 3 = 01: Set P(S) X4, 3 = 00 Set P (C) X2,1,0=001: Cch = PH10 X2,1,0=010: Cch = PH8 X2,1,0=1XX: Cch = PH6	
SCA X (SMS)	1101 1010 00XX XXXX	X0~3: S1~4 Enable (SEF0~3) X5: A1-4 Enable (SEF5) X4: C1-4 Enable (SEF4)	
SPA X	1101 1100 000X XXXX	X4: Set A4~1 Pull-Low X3~0: Set A4~1 I/O	
SPB X	1101 1101 0000 XXXX	X3~0: Set D4~1 I/O	
SPC X	1101 1110 000X XXXX	X4: Set C4-1 Pull-Low/ Low-Level-Hold X3~0: Set C4-1 I/O	
SPD X	1101 1111 0000 XXXX	X3-0: Set D4~1 I/O	
TMS Rx	1110 0000 0XXX XXXX	Timer1 ← Rx, AC	
TMS @HL	1110 0001 0000 0000	Timer1 ← T@HL	

Instruction	Machine Code	Function	Flag/Remark
TMSX	1110 0010 XXXX XXXX	X7,6=11: Ctm=FREQ X7,6=10: Ctm=PH15 X7,6=01: Ctm=PH3 X7,6=00: Ctm=PH9 X5~0: Set Timer1 Value	
SPK Rx	1110 0011 00XX XXXX	X5 = 1: Set all Hi-Z X4 = 1: Set all = 1 X3 = 0: Set n of 16	IOC=Normal IOC=Key_scan IOC=Key_scan
TM2 Rx	1110 0100 0XXX XXXX	Timer2 ← Rx, AC	
TM2 @HL	1110 0101 0000 0000	Timer2 ← T@HL	
TM2X X	1110 011X XXXX XXXX	X8,7,6=111 : Ctm=PH13 X8,7,6=110 : Ctm=PH11 X8,7,6=101 : Ctm=PH7 X8,7,6=000 : Ctm=PH5 X8,7,6=011 : Ctm=FREQ X8,7,6=010 : Ctm=PH15 X8,7,6=001 : Ctm=PH3 X8,7,6=000 : Ctm=PH9 X5~0: Set Timer2 Value	
SHE X	1110 1000 0XXX XXX0	X6: Enable HEF6(RFC) X4: Enable HEF4(TMR2) X3: Enable HEF3(PDV) X2: Enable HEF2(INT) X1: Enable HEF1(TMR1)	
SIE* X	1110 1001 0XXX XXXX	X6: Enable IEF6(RFC) X5: Enable IEF5(KEY_S) X4: Enable IEF4(TMR2) X3: Enable IEF3(PDV) X2: Enable IEF2(INT) X1: Enable IEF1(TMR1) X0: Enable IEF0(A,CPT)	
PLC X	1110 101X 0XXX XXXX	X8: Reset PH15~11 X6, 4~0: Reset HRF6, 4~0	
SRF X	1110 1100 00XX XXXX	X5: Enable Cx Control X4: Enable Timer2 Control X3: Enable Counter X2: Enable RH Output X1: Enable RT Output X0: Enable RR Output	 ENX EHM ETP ERR
SRE X	1110 1101 X0XX 0000	X7: Enable SRF7 X6: Enable SRF6 X5: Enable SRF5 X4: Enable SRF4 X3~0: Enable SRF3~0	SRF7 (KEY_S) SRF6 (A Port) SRF5 (INT) SRF4 (C Port) SRF3~0 (S Port)
FAST	1110 1110 0000 0000	SCLK: High Speed Clock	
SLOW	1110 1111 0000 0000	SCLK: Low Speed Clock	

Instruction	Machine Code	Function	Flag/Remark
SF X	1111 0000 X0XX XXXX	X7: Reload Set X5: S-Port Pull-low X4: WDT Enable X3: HALT after EL LIGHT X2: EL LIGHT On X1: BCF Set X0: CF Set	RL1 WDF BCF CF
RF X	1111 0100 X00X 0XXX	X7: Reload Reset X5: S-port L_L H X4: WDT Reset X2: EL LIGHT Off X1: BCF Reset X0: CF Reset	RL1 WDF BCF CF
SF2 X	1111 1000 0000 0XXX	X0: Reload Set X1: Dis-ENX Set X2: Close all segments X3: Jump to next page	RL2 DED RSOFF
RF2 X	1111 1001 0000 0XXX	X0: Reload Reset X1: Disable Dis-ENX Reset X2: Release all Segments	RL2 DED RSOFF
ALM X	1111 101X XXXX XXXX	X8,7,6=111: FREQ X8,7,6=100: DC1 X8,7,6=011: PH3 X8,7,6=010: PH4 X8,7,6=001: PH5 X8,7,6=000: DC0 X5~0 ← PH15~10	
ELC X	1111 110X XXXX XXXX	X8=1 BCLKX X8=0 PH0 X7,6=11 BCLK/8 X7,6=10 BCLK/4 X7,6=01 BCLK/2 X7,6=00 BCLK X5,4=11 1/1 X5,4=10 1/2 X5,4=01 1/3 X5,4=00 1/4 X3,2=11 PH5 X3,2=10 PH6 X3,2=01 PH7 X3,2=00 PH8 X1,0=11 1/1 X1,0=10 1/2 X1,0=01 1/3 X1,0=00 1/4	ELP – CLK BCLKX ELP – DUTY ELC – CLK ELC – DUTY
HALT	1111 1110 0000 0000	HALT operation	
STOP	1111 1111 0000 0000	STOP operation	

Symbol description

AC	: Accumulator	D	: Immediate Date
ACn	: Accumulator Bit N	PC	: Program Counter
X	: Address	CF	: Carry Flag
Rx	: Memory of Address X	ZERO	: Zero Flag
Rxn	: Memory Bit N of Address X	WDF	: Watchdog Timer Enable Flag
Ry	: Memory of Working Register Y	HL	: Index Register
BCF	: Backup Flag	BCLK	: System clock stops only in STOP condition
@HL	: Addres s of Index	IEFn	: Interrupt Enable Flag
HRFn	: HALT Release Flag	SRFn	: STOP Release Enable Flag
HEFn	: HALT Release Enable Flag	SCFn	: Start Condition Flag
Cfq	: Clock Source of Frequency Generator	Cch	: Clock Source of Chattering Detector
Ctm	: Clock Source of Timer	TMR	: Timer Overflow Release Flag
Fout	: RFC Frequency	( )	: Content of Register
PDV	: Predivider	SEFn	: Switch Enable Flag
Lz	: LCD Latch	FREQ	: Frequency Generator Setting Value
T@HL	: Address of Index ROM	ADF	: ADC Flag
CSF	: Clock Source Flag	DAC	: Digital-to-Analog Converter Output Signal
@L	: Low Address of Index	@H	: High Address of Index
RFOVF	: RFC Overflow Flag	H(T@HL)	: High Nibble of Index ROM
L(T@HL)	: Low Nibble of Index ROM		

Appendix (Important Issue for APU429/428)

Chip's internal vlotage V.S. power mode and external connection

	AG	LI		EXT-V	Note
V_{DD1}	Vsupply	1/2 × Vsupply		1/2 × Vsupply	
V_{DD2}	2 × V_{DD1}	Vsupply		Vsupply	
V_{DD3}	3 × V_{DD1}	3/2 × Vsupply		3/2 × Vsupply	*1
V_{DD4}	4 × V_{DD1}	2 × Vsupply		2 × Vsupply	*2
BAK	V_{DD1}	BCF=0	BCF=1	V_{DD2}	*3
		V_{DD1}	V_{DD2}		

Note: *1: V_{DD3} is only used for LCD operating in 1/3 bias and 1/4 bias. If 1/2 bias chosen, V_{DD3} need be connected to V_{DD2} (V_{DD3} is equal to V_{DD2}).

*2: V_{DD4} is only used for LCD operating in 1/4 bias. If 1/3 bias chosen, V_{DD4} need be connected to V_{DD3} (V_{DD4} is equal to V_{DD3}). If 1/2 bias chosen, V_{DD4} need be connected to V_{DD2} (V_{DD4} is equal to V_{DD2}).

*3: BAK is defined as chip's internal power supply node, which is used only for internal logic circuitry.

A. Whatever the power mode used, all external VDD# pins must connect a capacitor (0.05μF or 0.1μF) to GND for decoupling power noise using.

B. All VDD# pins other than Vsupply are from voltage charge pump, i.e. If no clock, then VDD# pins can not supply out.

C. Vsupply is the power supply for Chip and depends on the power mode used, all the input and output pins voltage range follow the Vsupply.

The capacitor connected between CUP2 and CUP3 is only when APU429 operating in 1/4 bias.

Some notes for BCF flag

BCF is always set to ″High″ automatically after Power on, Reset and STOP mode.

A. For power saving use, BCF may be set to ″Low″ which can reduce chip's current consumption.

B. Ag and Li battery mode applications:
After Power on, Reset or release from STOP mode. Need to wait 2 seconds long, then can set BCF to ″Low″.

C. Larger current load and fast clock:
a. BCF should be set to ″High″ for the case of fast clock or larger current load (such as RFC, ADC, DAC, EL-light and Buzzer output) use.
b. After set BCF to ″high″, need wait 2 ms long at least, then can enable larger current load. Or after disable Larger current load, need wait 2ms long at least, then can set BCF to ″Low″

D. Li battery mode applications:
Especially for Li battery mode, BCF switching will cause a temporary current surge (or power noise) on BAK. Furthermore if not necessary, don't switch BCF too often as possible.

E. Improperly use of BCF will cause malfunction to chips.

F. Lower current consumption and reliability:
The chip's reliability will greatly decrease if invalid use BCF, especially for Li-battery mode. Because the chip's internal power also switches between V_{DD1} and V_{DD2}, which also cause a temporary power noise.

Input pin

Any input pins floating will cause chips in malfunction and large current consumption.

32.768kHz X′tal oscillator

Always layout the X′tal as close the Chips as possible and don′t place any signals across the layout routing. Since X′tal oscillation circuit consumes current only 0.5μA to 1μA, any power noise will disturb the oscillation. The proper external capacitors for X_{IN} and X_{OUT} are necessary for the accuracy and stability of oscillation.

1 / (Cin+Cpcb) + 1 / (Cout+Cpcb) = 1/CL

The Chip′s X_{OUT} pin has an internal capacitor around 10~20pF connected to BAK (chip′s internal Node).

For example:

Epson′s C-001R 20ppm, CL=12.5pF

C_{IN} = 25pF

C_{OUT} = 15pF

The time accuracy will be around ± 0.5 second/day

Note: The parasitic capacitors of X′tal pins in PCB layout need be considered in above calculation.

RFC/Event counter/IOA for APU429

If anyone uses RFC / Event counter function and IOAs in the same application, make sure the pin IOA1 (which is corresponding to CX by mask option) must set as IOA′s output mode by SPA instruction. Or the signal changes on CX pin may cause HALT release or interrupt for IOA′s port. In this case the program couldn't function properly.