10/100BASE Dual Speed 8-Port Repeater

Ver. 1.1

Features

- IEEE 802.3u repeater compatible
- Supports 8 10/100Mbps RMII I/F repeater ports
- Accompany with AX88872 to build a low cost dual speed repeater solution
- Up-to 4 repeaters can be cascaded for vertical expansion
- Up-to 3 chips can be cascaded locally for horizontal expansion
- All ports can be separately isolated or partitioned in response to fault condition
- Separate jabber and partition state machines for each port
- Per-port LED display for Jabber, Partition, Activity and global collision, utilization (%) for 10/100Mbps presentation
- Power on LED diagnosis. All the LED display will follow the "ON-OFF-ON-OFF-Normal" operation procedure during/after power on reset
- 50MHz Operation, 3.3volt and 128-pin PQFP

Product description

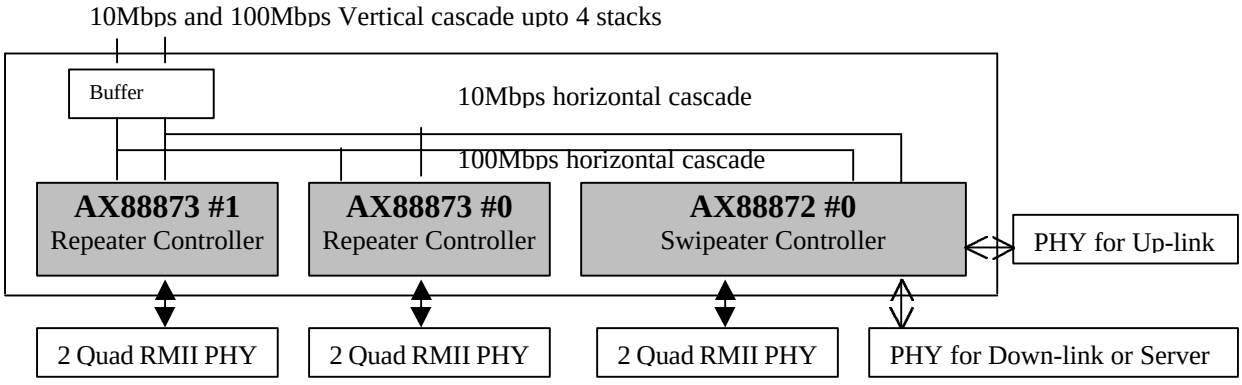
The AX88873 10/100Mbps Dual Speed repeater Controller is a counterpart of AX88872 without built in 4-ports switch. It is design for low cost dual speed dumb HUB application.

The AX88873 directly supports up-to eight 10/100Mbps automatic links RMII interfaces. Maximum up-to 96 repeater ports can be constructed by stacking 1 AX88872 and 2 AX88873 chips horizontally and then cascading 4 horizontal boards vertically.

With using 128-pin low cost package, accompany with AX88872 to build up low cost dual speed repeater application. Not only perform the repeater function but gain additional 2 switch ports. The 2 dual speed switch ports are connected to external MII or RMII interfaces PHY for various applications. For example, one port is use for down link and the other is used for up link to extend the network topology. The other case is one port for up link and the other port for server.

The AX88873 is designed base on IEEE 802.3u clause 27 " Repeater for 100Mb/s base-band networks" It is fully compatible with IEEE 802.3u standard. Please refer Ax872-11.doc to get more information about AX88872.

System Block Diagram



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FIGURES

1.0 AX88873 Overview

1.1 General Description

The AX88873 is a simple dual speed repeater that provides two expansion buses for 10M and 100M segments respectively. Accompany with AX88872 (build-in a 4-port switch) can construct high port count (16 ports or 24 ports) application and gain 2 additional switch ports. Additional two switch ports are also useful for up-link or connection of server.

The pin count of chip is reduced to 128 when design uses RMII I/F instead of MII. It is not only simplify the design but also user can choose low cost RMII Quad PHY.

1.2 AX88873 Block Diagram:

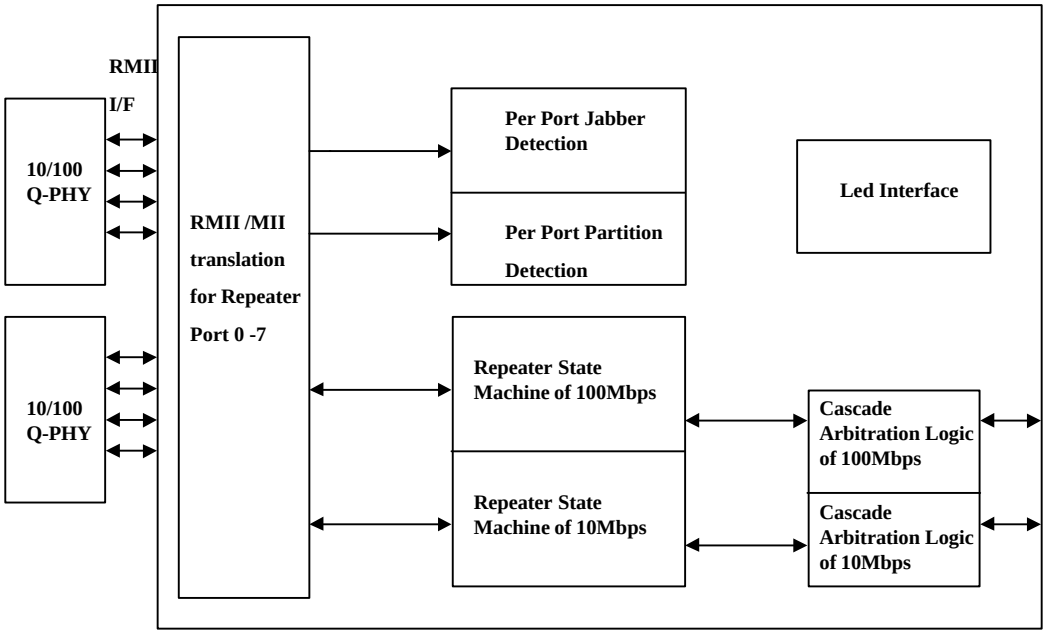


Fig - 1 AX88873 Block Diagram

1.3 Pin Connection Diagram

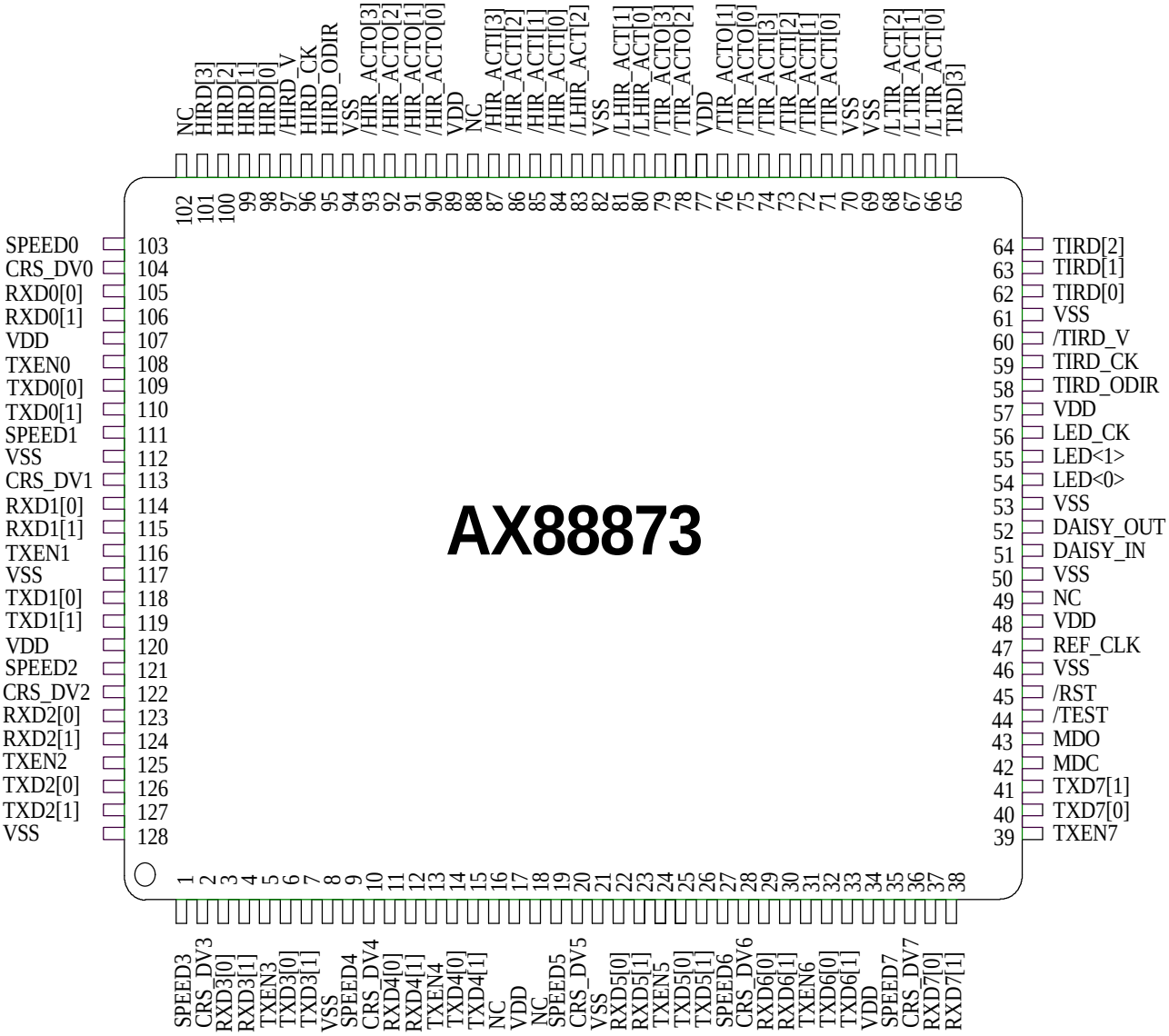


Fig - 2 Pin Connection Diagram

2.0 Pin Description

The following terms describe the AX88873 pin out:

All pin names with the "/" suffix are asserted low.

I	=	Input
O	=	Output
I/O	=	Input /Output

2.1 RMII interface for repeater ports

2.1.1 Repeater Port 0

Signal Name	Type	Pin No.	Description
SPEED0	I	103	**Speed Select :** SPEED0 is not standard RMII signal. This signal is sourced from PHY to inform repeater whether 10M or 100M speed is auto-negociated. Active for 10Mbps speed is selected depending on power on configuration.
CRS_DV0	I	104	**Carrier Sense/Receive Data Valid :** CRS_DV is asserted asynchronously on detection of carrier. CRS_DV is asserted by the PHY when receive medium is non-idle. Loss of carrier shall result in the desertion of CRS_DV synchronous to the cycle of REF_CLK, which presents the first DI-bit of a nibble on to RXD0[1:0].
RXD0[1:0]	I	106,105	**Receive Data :** RXD0[1:0] is synchronous to REF_CLK RXD0[1:0] shall be "00" to indicate idle when CRS_DV is disserted. Value other than "00" are reserved for out-of-band signaling shall be ignored by MAC Upon assertion of CRS_DV, PHY shall ensure that RXD[1:0] = "00" until proper receive decoding takes place
TXEN0	O	108	**Transmit Enable :** TXEN0 is synchronous to REF_CLK. TXEN0 indicates that MAC is presenting DI-bits on TXD[1:0] for transmission. TXEN0 shall be negated prior to the 1st REF_CLK rising edge following the final DI-bit of a frame
TXD0[1:0]	O	110,109	**Transmit Data :** TXD0[1:0] shall transition synchronously to REF_CLK. TXD0[1:0] shall be "00" to indicate idle when TX_EN is disserted. Value other than "00" are reserved for out-of-band signaling shall be ignored by PHY. When TX_EN is asserted, TXD[1:0] are accepted for transmission by PHY

2.1.2 Repeater Port 1

Signal Name	Type	Pin No.	Description
SPEED1	I	111	**Speed Select :** Please references section 2.1.1 PORT0 description.
CRS_DV1	I	113	**Carrier Sense/Receive Data Valid :** Please references section 2.1.1 PORT0 description.
RXD1[1:0]	I	115,114	**Receive Data :** Please references section 2.1.1 PORT0 description.
TXEN1	O	116	**Transmit Enable :** Please references section 2.1.1 PORT0 description.
TXD1[1:0]	O	119,118	**Transmit Data :** Please references section 2.1.1 PORT0 description.

2.1.3 Repeater Port 2

Signal Name	Type	Pin No.	Description
SPEED2	I	121	**Speed Select :** Please references section 2.1.1 PORT0 description.
CRS_DV2	I	122	**Carrier Sense/Receive Data Valid :** Please references section 2.1.1 PORT0 description.
RXD2[1:0]	I	124,123	Receive Data : Please references section 2.1.1 PORT0 description.
TXEN2	O	125	**Transmit Enable :** Please references section 2.1.1 PORT0 description.
TXD2[1:0]	O	127,126	**Transmit Data :** Please references section 2.1.1 PORT0 description.

2.1.4 Repeater Port 3

Signal Name	Type	Pin No.	Description
SPEED3	I	1	**Speed Select :** Please references section 2.1.1 PORT0 description.
CRS_DV3	I	2	**Carrier Sense/Receive Data Valid :** Please references section 2.1.1 PORT0 description.
RXD3[1:0]	I	4,3	**Receive Data :** Please references section 2.1.1 PORT0 description.
TXEN3	O	5	**Transmit Enable :** Please references section 2.1.1 PORT0 description.
TXD3[1:0]	O	7,6	**Transmit Data :** Please references section 2.1.1 PORT0 description.

2.1.5 Repeater Port 4

Signal Name	Type	Pin No.	Description
SPEED4	I	9	**Speed Select :** Please references section 2.1.1 PORT0 description.
CRS_DV4	I	10	**Carrier Sense/Receive Data Valid :** Please references section 2.1.1 PORT0 description.
RXD4[1:0]	I	12,11	**Receive Data :** Please references section 2.1.1 PORT0 description.
TXEN4	O	13	**Transmit Enable :** Please references section 2.1.1 PORT0 description.
TXD4[1:0]	O	15,14	**Transmit Data** : Please references section 2.1.1 PORT0 description.

2.1.6 Repeater Port 5

Signal Name	Type	Pin No.	Description
SPEED5	I	19	**Speed Select :** Please references section 2.1.1 PORT0 description.
CRS_DV5	I	20	**Carrier Sense/Receive Data Valid :** Please references section 2.1.1 PORT0 description.
RXD5[1:0]	I	23,22	**Receive Data :** Please references section 2.1.1 PORT0 description.
TXEN5	O	24	**Transmit Enable :** Please references section 2.1.1 PORT0 description.
TXD5[1:0]	O	26,25	**Transmit Data :** Please references section 2.1.1 PORT0 description.

2.1.7 Repeater Port 6

Signal Name	Type	Pin No.	Description
SPEED6	I	27	**Speed Select :** Please references section 2.1.1 PORT0 description.
CRS_DV6	I	28	**Carrier Sense/Receive Data Valid :** Please references section 2.1.1 PORT0 description.
RXD6[1:0]	I	30,29	**Receive Data :** Please references section 2.1.1 PORT0 description.
TXEN6	O	31	**Transmit Enable :** Please references section 2.1.1 PORT0 description.
TXD6[1:0]	O	33,32	**Transmit Data :** Please references section 2.1.1 PORT0 description.

2.1.8 Repeater Port 7

Signal Name	Type	Pin No.	Description
SPEED7	I	35	**Speed Select :** Please references section 2.1.1 PORT0 description.
CRS_DV7	I	36	**Carrier Sense/Receive Data Valid :** Please references section 2.1.1 PORT0 description.
RXD7[1:0]	I	38,37	**Receive Data :** Please references section 2.1.1 PORT0 description.
TXEN7	O	39	**Transmit Enable :** Please references section 2.1.1 PORT0 description.
TXD7[1:0]	O	41,40	**Transmit Data :** Please references section 2.1.1 PORT0 description.

2.2 Expansion Bus Interface for 100 Mbps

Signal Name	Type	Pin No.	Description
HIRD[3:0]	I/O/Z /PU	101,100 99,98	**INTER REPEATER DATA :** Nibble data input/output. Transfer data from the “active” AX88872/3 to all other “inactive” AX88872/3 chips. The bus-master of the IRD bus is determined by IR_ACT bus arbitration.
/HIRD_V	I/O/Z /PU	97	**INTER REPEATER DATA VALID :** This signal reflects the RX_DV status of the active port. Used to frame good packets.
HIRD_CK	I/O/Z /PU	96	**INTER REPEATER CLOCK VALID :** All inter repeater signals are synchronized to the rising edge of this clock.
HIRD_ODIR	O	95	**INTER REPEATER DATA IN/OUT DIRECTION :** This pin indicates the direction of IRD data . “High” = HIRD[3:0], /HIRD_V , HIRD_CK are Output. “Low” = HIRD[3:0], /HIRD_V , HIRD_CK are Input.
/LHIR_ACT[2:0]	I/O/OC	83,81,80	**LOCAL REPEATER ACTIVITY IN/OUT :** the function is the same as /HIR_ACTO[3:0] but for local repeater activity only.
/HIR_ACTI[3:0]	I/PU	87,86 85,84	**INTER REPEATER ACTIVITY IN:** These pins perform the same function as /HIR_ACTO[3:0] when they serve as input function. Then the /HIR_ACTO[3:0] insert external buffers the input function must be replaced with /HIR_ACTI [3:0].
/HIR_ACTO[3:0]	I/O/OC	93,92 91,90	**INTER REPEATER ACTIVITY IN/OUT:** The local repeater activity appearance, the signal of the related RID (Repeater ID) will be asserted and as an output pin. All other pins serve as input pins but except the collision conditions. When collision occurs , the signal of related (RID-1) pins will also serve as outputs and will active during local collision period. The exception case is when RID = 0, then (RID-1) is replaced with (RID+1).

2.3 Expansion Bus Interface for 10 Mbps

Signal Name	Type	Pin No.	Description
TIRD[3:0]	I/O/Z /PU	65,64 63,62	**INTER REPEATER DATA :** Nibble data input/output. Transfer data from the "active" AX88872/3 to all other "inactive" AX88872/3 chips. The bus-master of the IRD bus is determined by IR_ACT bus arbitration.
/TIRD_V	I/O/Z /PU	60	**INTER REPEATER DATA VALID :** This signal reflects the RX_DV status of the active port. Used to frame good packets.
TIRD_CK	I/O/Z /PU	59	**INTER REPEATER CLOCK VALID :** All inter repeater signals are synchronized to the rising edge of this clock.
TIRD_ODIR	O	58	**INTER REPEATER DATA IN/OUT DIRECTION :** This pin indicates the direction of data for external transceiver. "High" = TIRD[3:0], /TIRD_V , TIRD_CK are Output. "Low" = TIRD[3:0], /TIRD_V , TIRD_CK are Input.
/LTIR_ACT[2:0]	I/O/OC	68,67,66	**LOCAL REPEATER ACTIVITY IN/OUT :** the function is the same as /TIR_ACTO[3:0] but for local repeater activity only.
/TIR_ACTI[3:0]	I/PU	74,73, 72,71	**INTER REPEATER ACTIVITY IN:** These pins perform the same function as /HIR_ACTO[3:0] when they serve as input function. Then the /HIR_ACTO[3:0] insert external buffers the input function must be replaced with /HIR_ACTI [3:0].
/TIR_ACTO[3:0]	I/O/OC	79,78 76,75	**INTER REPEATER ACTIVITY IN/OUT:** The local repeater activity appearance, the signal of the related RID (Repeater ID) will be asserted and as an output pin. All other pins serve as input pins but except the collision conditions. When collision occurs , the signal of related (RID-1) pins will also serve as outputs and will active during local collision period. The exception case is when RID = 0, then (RID-1) is replaced with (RID+1).

2.4 LED Display

<table>
<tr><th>Signal Name</th><th>Type</th><th>Pin No.</th><th>Description</th></tr>
<tr><td>LED[1:0]</td><td>O</td><td>55, 54</td><td>Those signals indicate each port‘s statuses (such as activity, jabber and partition) and global information(such as Collision , Repeater ID, Utilization) in sequence. For detail , see the LED timing specification
The utilization of 100M segment and 10M segment are using the same scale.
The Utilization % display define as following : (See Note 1 also)
1: Led off
0: Led on
<table>
<tr><th>Utilization %</th><th>UTI0</th><th>UTI1</th><th>UTI2</th><th>UTI3</th><th>UTI4</th><th>UTI5</th></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>5</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>10</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>15</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>30</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>60</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
</table>
LED[0] : This signal also indicates 100M repeater collision (Blinking) during the interval of sequence shift
data.

LED[1] : This signal also indicates 10 M repeater collision (Blinking) during the interval of sequence shift data.</td></tr>
<tr><td>LED_CK</td><td>O</td><td>56</td><td>LED Clock : The signal is a discontinue clock for LED signals serial shift out. The clock period width is 400nS and last 32 cycle with every 52.4ms repeated.</td></tr>
</table>

2.5 Miscellaneous

Signal Name	Type	Pin No.	Description
/RST	I	45	**Reset :** Active Low The chip is reset when this signal is asserted Low
REF_CLK	I	47	**Reference clock :** The input is a continuous clock at 50Mhz for timing reference with RMII interface.
DAISY_IN	I/PU	51	**Repeater Identification Number Daisy-Chain In :** When MODE=”1” , This pin is a daisy chain serial input for Repeater ID. A state machine always monitors the input if a correct data (RID) present at the pin, the (RID+1) will be written to RID register and override the power on setup RID for the chip.
DAISY_OUT	O/ML	52	**Repeater Identification Number Daisy-Chain Out :** When MODE=”1” , This pin is periodically shift out the RID of itself to the next chained chip to inform that this ID has already been occupied. The RID is shift out periodically every about 200us.
MDO	O	43	**Station Management Data Out :** For setup PHY auto-negotiation registers. A burst write commands are issue to setup PHY register after reset. The PHY address 4h, 5h, 6h, 7h, 8h, 9h,Ah and Bh will be written as register 4h to value 00A1h (Advertise register set to 10/100 half-duplex mode)and register 0h to value 1000h(Enable auto-negotiation).
MDC	O	42	**Station Management Data Clock Out :** For MDO reference clock.
/TEST	I/PD	44	**Test Pin :** Active LOW

			The pin is just for test mode setting purpose only. Must be pull high when normal operation.
NC	O	16, 18 49,88 102	**NC :** Keep no connection
VDD	I	17, 34 48, 57 77, 89 107, 120	**POWER :** +3.3V +/-5%
VSS	I	8, 21 46, 50 53,61 69, 70 82, 94, 112, 117 128	**POWER:** 0V

2.6 Power on configuration setup signals cross reference table

Signal Name	Share with	Description
Speed_Define	TXD7[1]	**Speed Setting for Repeater Port 0 to Port 7 :** 0 : SPEED0~7 pin is Low for 10M,high for 100M 1 : SPEED0~7 pin is Low for 100M,high for 10M
LRID_S1 LRID_S0	TXD5[1] TXD5[0]	**Local Repeater ID Selection :** **LRID_S1 LRID_S0 LRID No.** 1 1 0 1 0 1 0 1 2 0 0 reserved

All of the above signals are pull-up for default values.

Note 1 :

The calculation formulae of Traffic Utilization between ASIX and NetCom is difference, so you will get different results when using SmartBit (SB) testing this item.

We found the SmartBit calculate the Utilization without include 96 Bit time inter frame gap (IFG). So the utilization value can be 100%. As well as we found SB used min packet size (64 byte) and min IFG (96 bit-time) as 100% utilization. In theory, when max packet size (1518 byte) and min IFG the utilization will be more than 100%, but SB also treat it as 100%.

In our AX88873 design, we use real cable bandwidth as calculation base. We calculate the bit counts of carrier within a unit time. Because of the existence of inter frame gap, In our calculation 100% utilization is impossible. So the above two cases (64 byte packet size and 1518 byte packet size with min. IFG), we will count as 85.7% and 99.2%.

If using SB test result to indicate utilization LED the value must be modified. See the following reference table.

ASIX's Utilization%	1	5	10	15	30	60
SmartBit's Utilization%	2	7	12	17	34	68

3.0 Functional Description

3.1 Repeater State Machine

The repeater state machine is in idle state when there is no carrier presented on any ports **.** When there is only one port has receive activity, the repeater state machine will enter data -forwarding state to ensure correct data forwarding to other connected ports. If collision happens anytime, The repeater state machine detects collision then send jam pattern to all ports until collision ceases.

3.2 RXE /TXE Control

Idle state

CRS_DV(ALL) = 0, the repeater sends no data to any port.

RXE(ALL) = 0.
TXE(ALL) = 0.

Data Forwarding state

If CRS_DV(ALL) = 1, N is the only one port that has incoming packet.

RXE(N) = 1, RXE(ALLXN) = 0.
TXE(N) = 0, TXE(ALLXN) = 1.

Collision state

If CRS_DV(ALL) > 1, the repeater sends jam pattern to all ports.

RXE(ALL) = 0.
TXE(ALL) = 1.

One Port Left state

When all packets are back off except only one port still has activity, that is CRS_DV(ALL) = 1 again . N is the only one left port that has incoming packet. The repeater sends jam pattern to all other port except for the still activity ports.

RXE(ALL) = 0.
TXE(ALLXN) = 1.

3.3 Jabber State Machine

To prevent an illegally long reception of data from reaching the repeater unit, each port has its own jabber timer. If a reception exceeds this duration (64K bit times for AX88872A), the jabber condition will be detected. In this condition, repeater unit will disable receive and transmit packets for the jabbered port and the other ports remain the normal operation.

When the carrier is no longer detected for the jabbered port or reset the repeater, the jabber state will be existed and the port will receive and transmit packets normally.

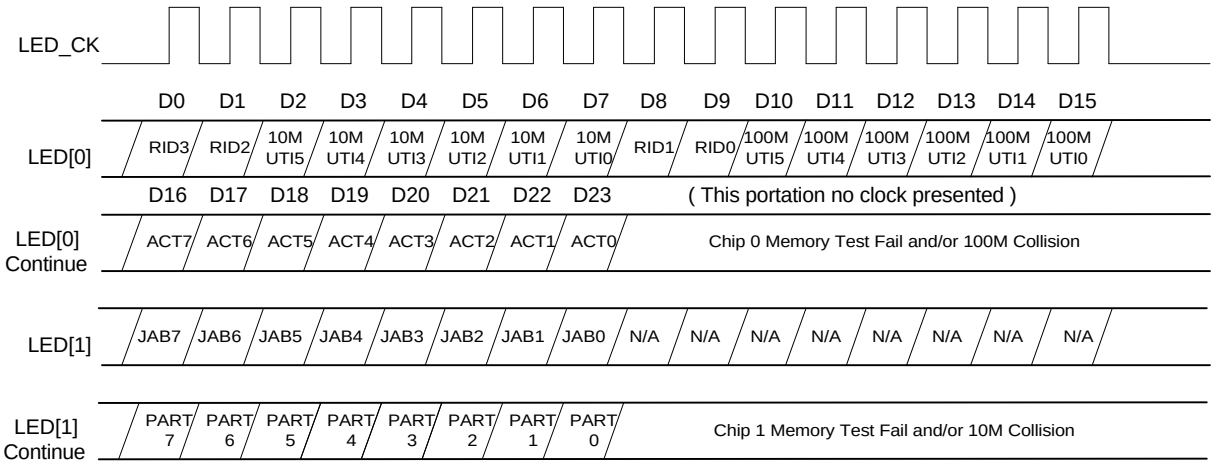
3.4 Partition State Machine

The partition state machine is used to protect network from being upset when a port suffer continuous collision, each port uses a partition state machine to detect and prevent this condition. When a port suffers from continuous 64 times of collision events, then it goes to Partition State. The partitioned port will be not released until a packet without collision be transmitted(more than 512 bit times for AX88872A) or reset the repeater.

3.5 LED Display Interface

AX88873 provides per-port LED status indication for partition, jabber, activity and support rate - based LED for 10 and 100Mbps segments utilization (%) . All LED[1:0] perform active low.

LED[1:0] Status Driver Wave-form as follows :



Notes:

a. PART7~0indicates partition status for each port
b. JAB7~0 indicates jabber status for each port
c. ACT7~0 indicates activity status for each port
d. RID3~0 is the ID of repeater chip
e. 10M UTI5~0 indicate global utilization rate of 10Mbps for each 104.8ms sampling period.
f. 100M UTI5~0 indicate global utilization rate of 100Mbps for each 104.8ms sampling period.

It must use external shift register to decode data on LED[1:0]. The application shows as follows:

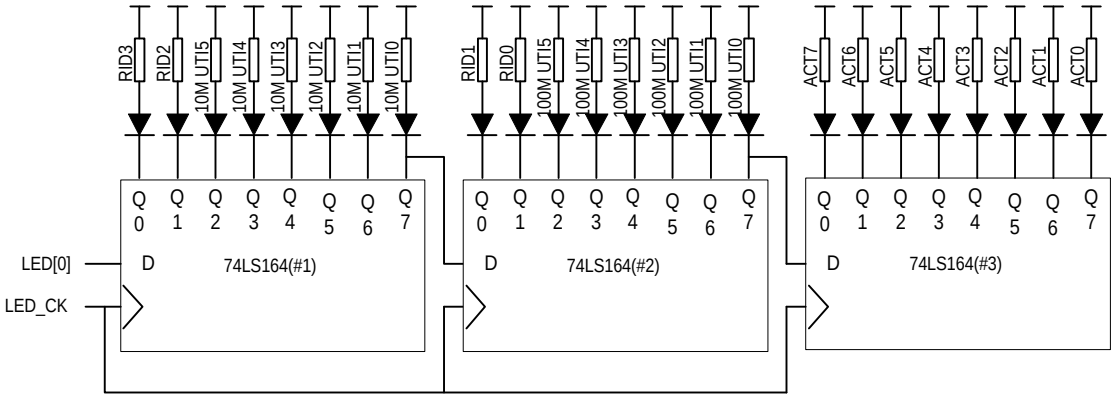


Fig - 3 Application for LED display

If the user don‘t want to show jabber status, take away the latter 74LS164(#2). The application is the same for LED[1].

4.0 INTERNAL REGISTERS

The information reserve for intelligent function.

5.0 ELECTRICAL SPECIFICATION AND TIMING

5.1 Absolute Maximum Ratings

Description	SYM	Min	Max	Units
Operating Temperature	Ta	0	+70	°C
Storage Temperature	Ts	-55	+150	°C
Supply Voltage	Vcc	-0.3	+4	V
Input Voltage	Vin	-0.3	Vdd+0.5	V
Output Voltage	Vout	-0.3	Vdd+0.5	V
Lead Temperature (soldering 10 seconds maximum)	Tl	-55	+220	°C

Note : Stress above those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to Absolute Maximum Ratings conditions for extended period, adversely affect device life and reliability

5.2 General Operation Conditions

Description	SYM	Min	Max	Units
Operating Temperature	Ta	0	+70	°C
Supply Voltage	Vdd	+3.0	+3.6	V

5.3 DC Characteristics

(Vdd=3.0V to 3.6V, Vss=0V, Ta=0°C to 70°C)

Description	SYM	Min	Max	Units
Low Input Voltage	Vil	Vss-0.3	0.8	V
High Input Voltage	Vih	2	Vdd+0.5	V
Low Output Voltage	Vol		0.4	V
High Output Voltage	Voh	2.4		V
Input Leakage Current 1 (Note 1)	Iil1		10	uA
Input Leakage Current 2 (Note 2)	Iil1		500	uA
Output Leakage Current	Iol		10	uA

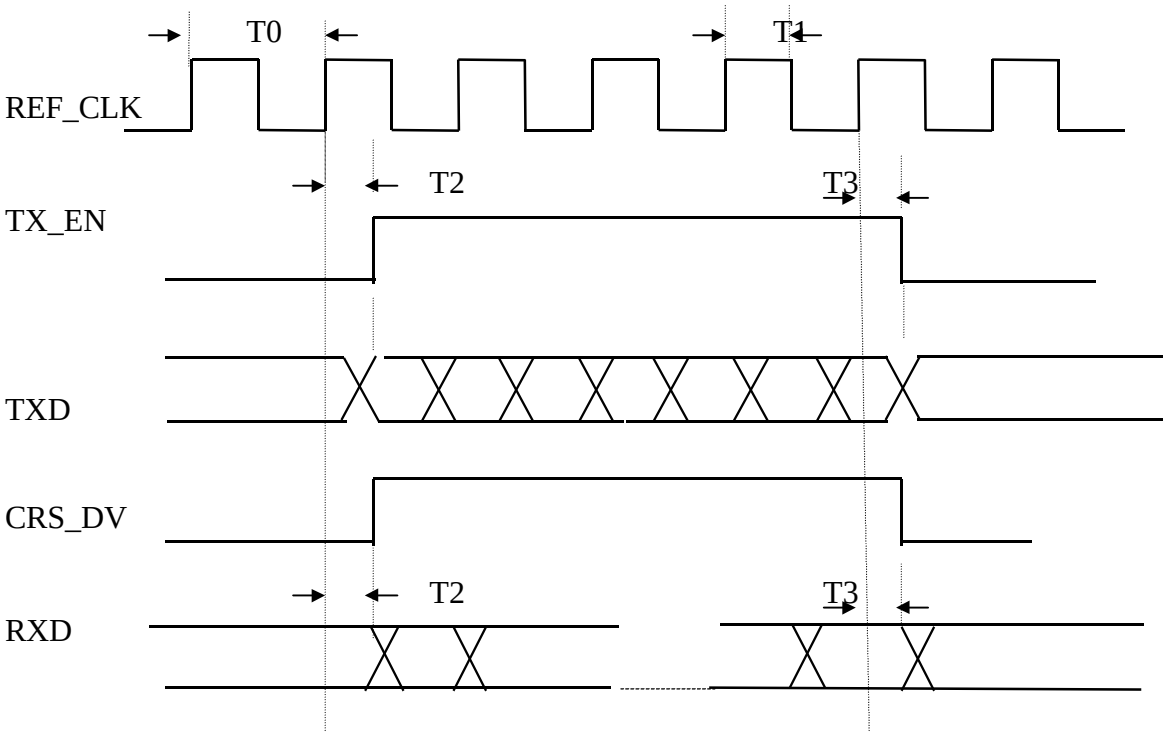
Description	SYM	Min	Tpy	Max	Units
Power Consumption	Pc		TBD		mA

Note :

1. All the input pins without pull low or pull high.
2. Those pins had been pull low or pull high.

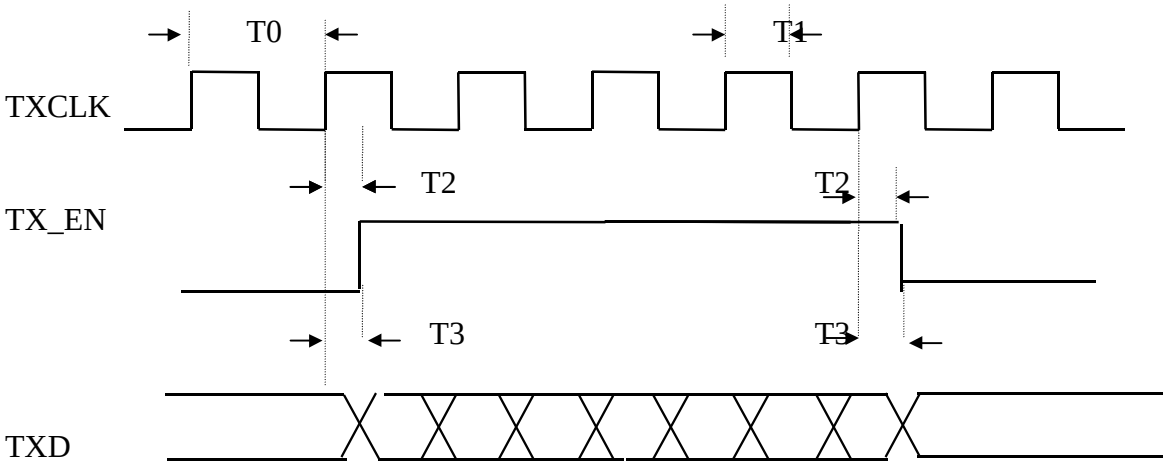
5.4 AC specifications

5.4.1 RMII Interface Timing TX & RX

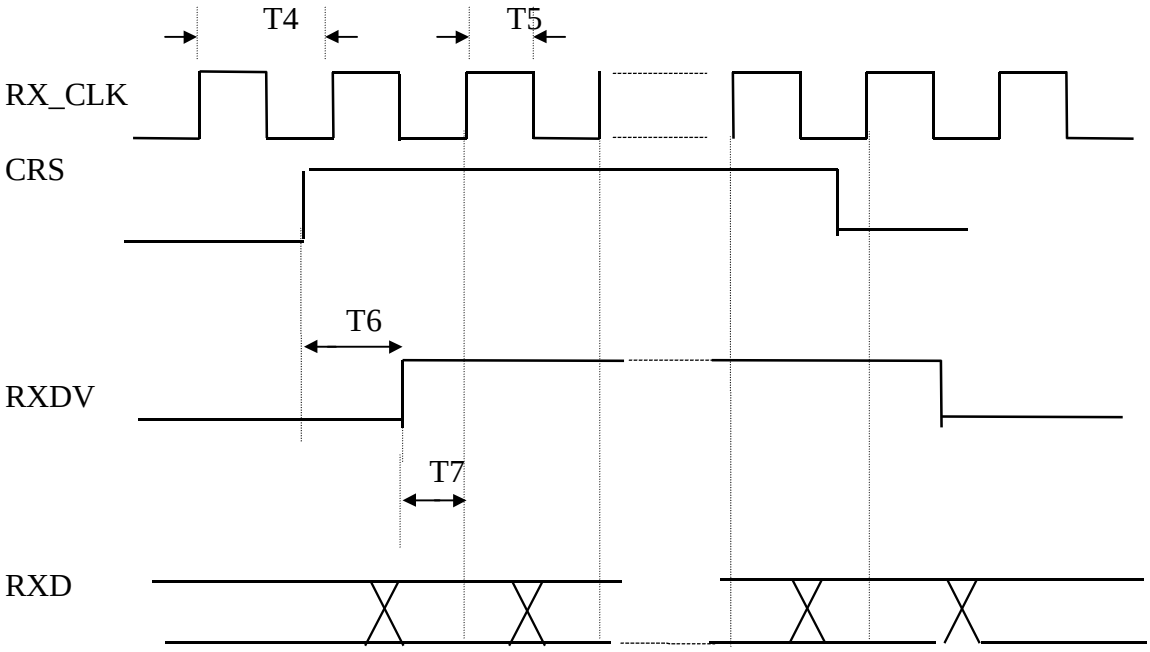


Symbol	Description	Min	Typ.	Max	Units
T0	REF_CLK Clock Cycle Time	19.998	20	20.002	ns
T1	REF_CLK Clock High Time	7	10	13	ns
T2	CRS_DV, RXD, TXEN and TXD data setup to REF_CLK rising edge	4			ns
T3	CRS_DV, RXD, TXEN and TXD data hold from REF_CLK rising edge	2			ns

5.4.2 MII Interface Timing TX & RX

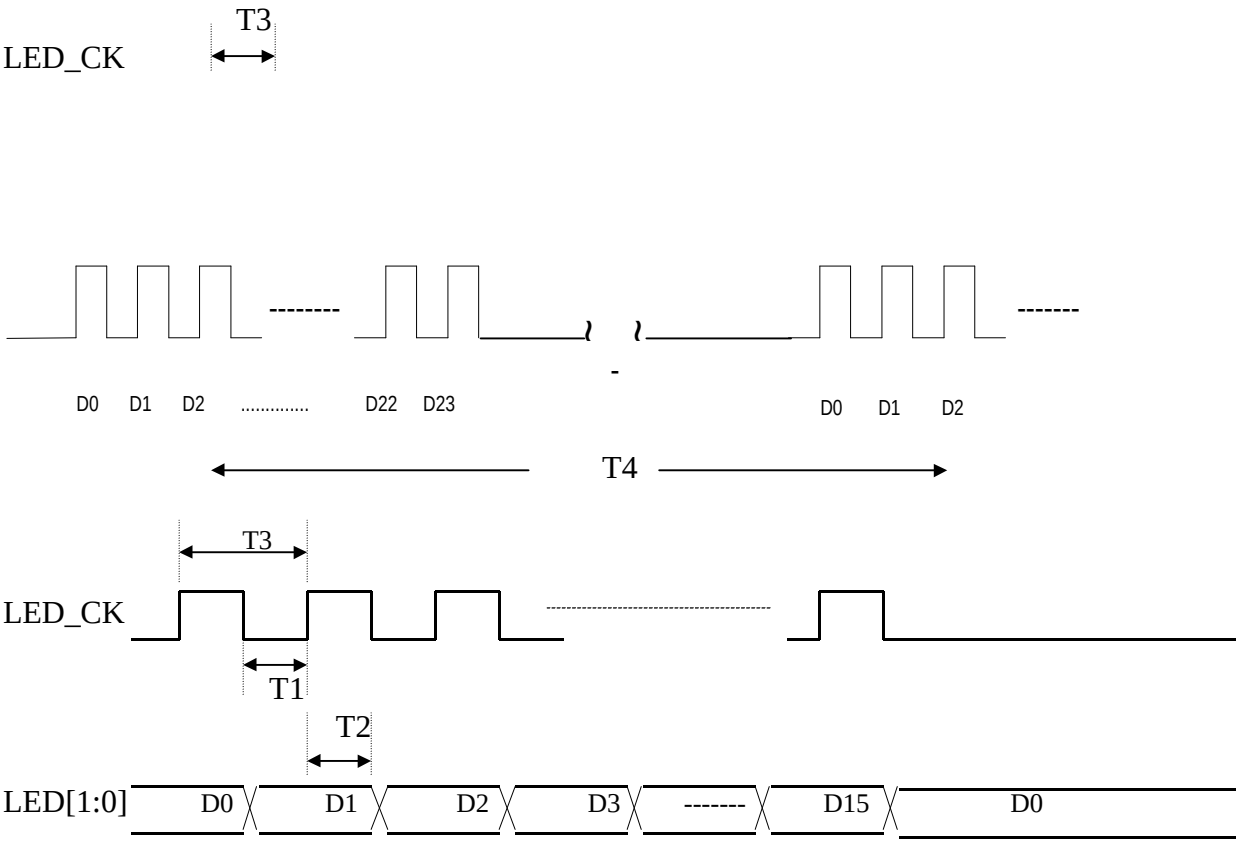


Symbol	Description	Min	Typ.	Max	Units
T0	TXCLK Cycle Time	39.996	40	40.004	ns
T1	TXCLK High Time	14	20	26	ns
T2	TX_EN Delay from TXCLK High	7.440		21.760	ns
T3	TXD Delay from TXCLK High	3.410		13.320	ns



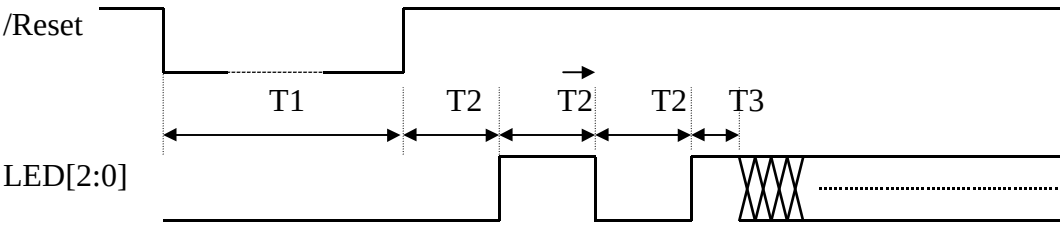
Symbol	Description	Min	Typ.	Max	Units
T4	RX_CLK Clock Cycle Time	39.996	40	40.004	ns
T5	RX_CLK Clock High Time	14	20	26	ns
T6	CRS to RXDV Delay Requirement	40		160	ns
T7	RXD or RXDV setup to RX_CLK rise time	10		-	ns

5.4.3 LED DISPLAY



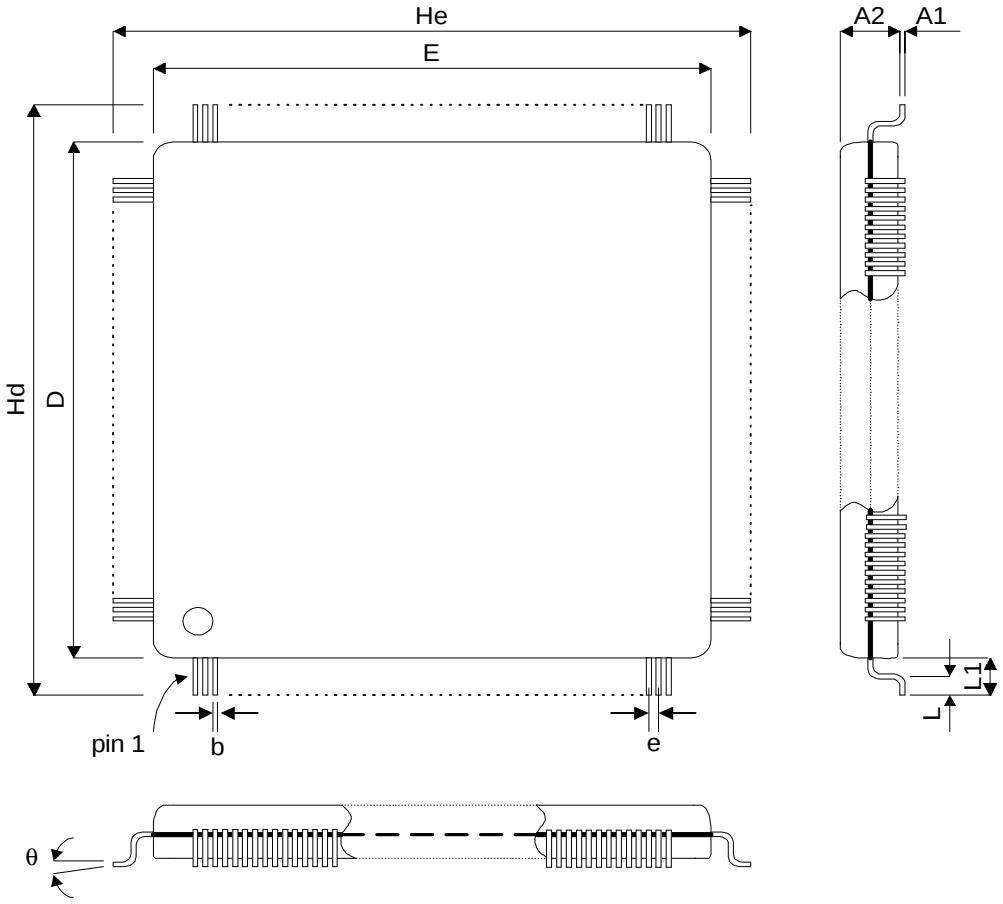
Symbol	Description	Min	Typ.	Max	Units
T1	LED setup to LED_CK High	190		200	ns
T2	LED hold from LED_CK High	200		210	ns
T3	LED_CK Period Width		400		ns
T4	LED_CK Cycle burst out period		52.4		ms

5.4.4 LED Display after Reset



Symbol	Description	Min	Typ.	Max	Units
T1	Repeater reset time	1000			ns
T2	LED Blink Time After Reset		838.4		ms
T3	LED Dark Time Before Normal Display		419.2		ms

6.0 Package Information

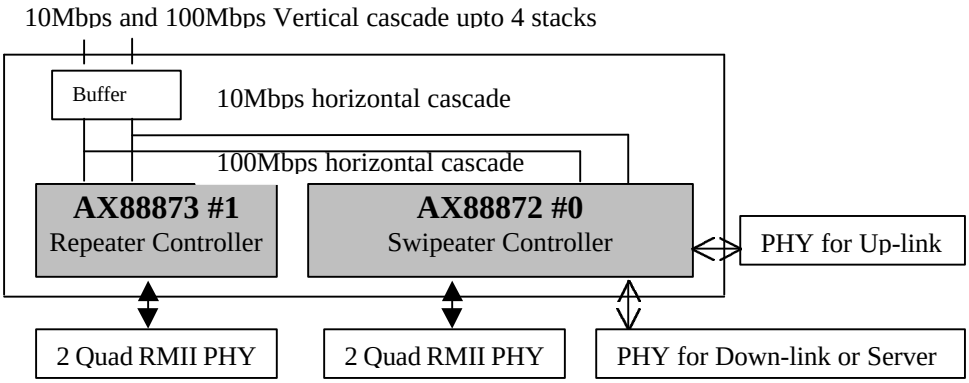


SYMBOL	MILIMETER		
	MIN.	NOM	MAX
A1	0.21	0.31	0.41
A2	2.80	2.85	2.90
b	0.15	0.20	0.30
D	13.80	14.00	14.20
E	19.80	20.00	20.20
e		0.50	
Hd	17.10	17.20	17.30
He	23.10	23.20	23.30
L	0.70	0.80	0.90
L1		1.60	
θ	0		8

Appendix A: Applications

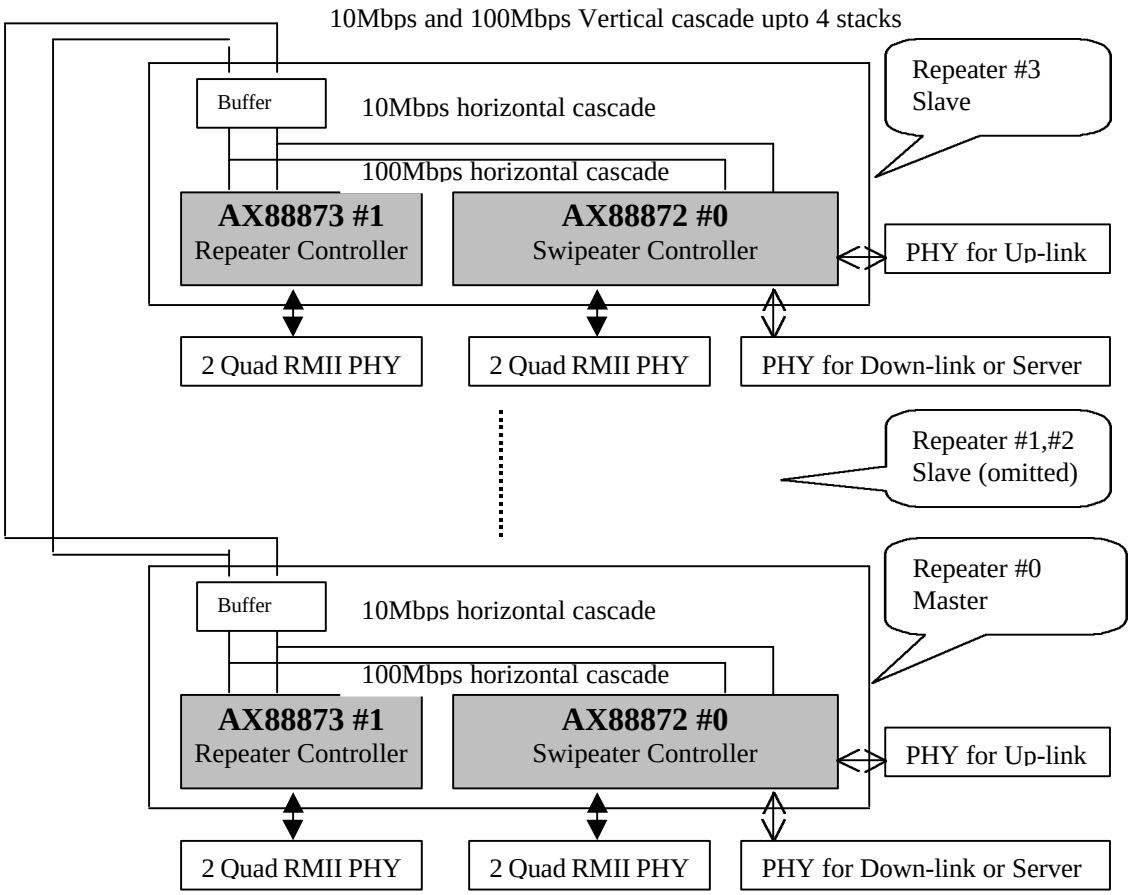
Some typical applications for AX88873 are illustrated bellow.

A.1 16-port (24-port) repeater with 2-port switch



Note : Add additional AX88873 to build a 24-port repeater

A.2 16-port repeater with upto 4 stacks



A.3 16-port repeater with upto 4 stacks up-link to external switch