AS17xx

Semicustom Bipolar Array

Features

Size (single tile)

- 87 x 75 mils
  Expandability of array
  (to 2 or 4 tiles)

Component Availability (single tile)

• Small NPN	48
• Dual collector PNP	21
• Vertical PNP	4
• Power NPN	3
• Diffused Resistors (total)	≈300 kΩ
• Pinch Resistors (3-terminal, 30kΩ)	8
• Cross-unders	13
• Buses	6

Basic Electrical Specs

• Transistor Matching (NPN & PNP)	<2%
• Primary voltage limitations:	
LV_{CEO}	18 V
BV_{CBO}	30 V
• Diffusion to substrate (Ground)	30 V
• NPN Parameters	
Beta	80–500
f_T (1mA)	300 MHz
BV_{EBO}	7 V
• PNP Parameters:	
Beta	20–300
f_T (1mA)	300 MHz
BV_{EBO}	30 V

Description

The AS17xx is Astec's proprietary semicustom bipolar array. This semicustom IC is a collection of individual transistors and resistors in a fixed configuration. The custom circuit is manufactured by creating a single metal mask to connect the components. This allows the designer to deal with only one mask for the IC layout instead of the actual 10 mask process. The semicustom array is useful for a wide range of functions, both analog and digital. In its simplest configuration, the AS17xx has 76 active devices available, but can be expanded to give up to four times this number in its largest configuration. This expandability of the array is a unique feature, allowing a whole range of semicustom circuits to be manufactured.

Because Astec has ongoing manufacturing of high volume circuits on this array, incremental wafer costs for engineering purposes are low. Therefore quality and reliability can be maintained even with small volume or engineering lots. Since the silicon can be completely processed and held awaiting only the metal etch and passivation steps, extremely fast turn-around times can be achieved.

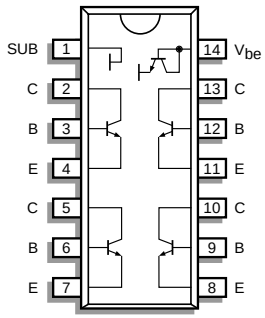
The AS17xx bipolar array uses a standard "20 Volt" bipolar technology. Although quite similar to industry standard arrays, it has a number of important improvements. First, the ratio of PNPs to NPNs has been increased to allow for more modern design practice. Second, the process has been modified to allow for a deep collector diffusion (sinker) which not only improves the $V_{CE(SAT)}$ of the transistors, but also allows for the elimination of regions with thin oxide which historically plague semicustom die with electrostatic discharge reliability concerns. Third, a set of low resistance sinker resistors allows for bussing supply or signal lines without using active components for cross-unders. In addition, the specific component geometries have been further optimized to facilitate the layout compared to the industry standard arrays. Resistors are now in a binary weighted 500 / 1k / 2k / 4k sequence for more simple value calculations. The power devices use multiple standard size emitters

so that they may also be used to create a device with an integral emitter area ratio with respect to a standard small NPN.

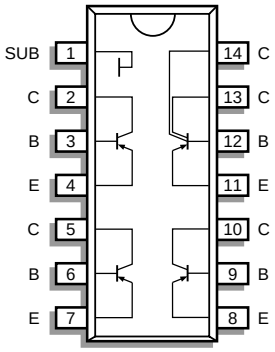
The AS17xx bipolar array can be packaged in industry standard DIP or surface mount packages with 8 to 40 leads. The number of pads available on the AS17xx varies with the number of tiles used as follows: single tile per die = 18 pads, two tiles per die = 30 pads, and four tiles per die = 40 pads. The extra pads not used for bonding to leads can be used for wafer level testing, trimming, and debugging.

Pin Configuration — Top view

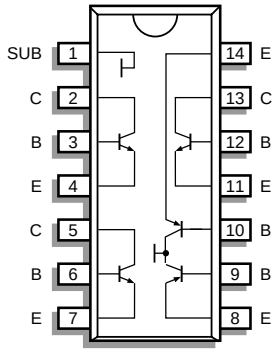
PDIP (N)
AS1700-NPN Kit Part



PDIP (N)
AS1700-PNP Kit Part



PDIP (N)
AS1700-PWR Kit Part



Die Configuration — Top view

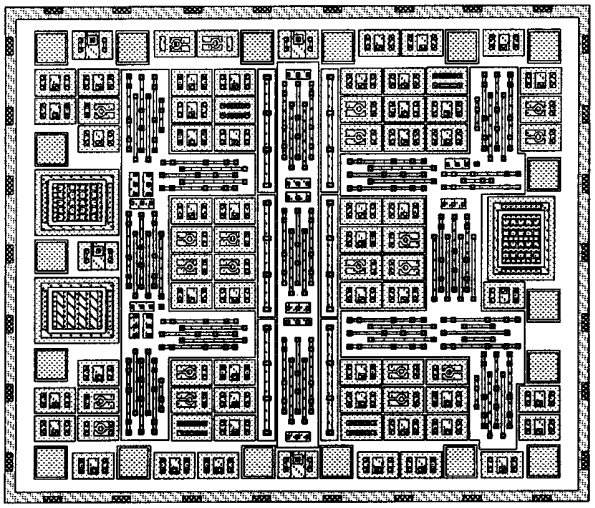


Figure 1. Single Tile Bipolar Array

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Continuous Power Dissipated at 25° C	P_D		
Single Transistor		300	mW
Total Package		1400	mW
Junction Temperature	T_J	150	°C
Storage Temperature	T_{STG}	–65 to 150	°C
Lead Temperature, Soldering 10 Seconds	T_L	300	°C

Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Electrical Characteristics

All parameters measured at 25° C.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
AS1700-NPN: Minimum NPN						
Collector-to-Emitter Breakdown Voltage	LV_{CEO}	I_C = 1 mA	20	35		V
Collector-to-Base Breakdown Voltage	BV_{CBO}	I_C = 100 µA	50	60		V
Emitter-to-Base Breakdown Voltage	BV_{EBO}	I_E = 10 µA	5	8		V
Collector Cutoff Current	I_{CEO}	V_{CE} = 18 V	0	2	100	nA
Collector-to-Emitter Saturation Voltage	$V_{CE\ SAT}$	I_B = 10 µA, I_C = 100 µA	0	95	200	mV
Base-to-Emitter Voltage	V_{BE}	V_{CE} = 3 V, I_C = 100 µA	650	680	700	mV
Static Forward Current-Transfer Ratio	β (h_{FE})	V_{CE} = 3 V, I_C = 100 µA	80	125	500	
Early Voltage	V_A			–150		V
Transistor Matching (measuring ΔI_C)		I_C = 200 µA	–10	<1	10	%
AS1700-PWR: Large NPN (20-emitter)						
Collector-to-Emitter Breakdown Voltage	LV_{CEO}	I_C = 1 mA	20	35		V
Collector-to-Base Breakdown Voltage	BV_{CBO}	I_C = 100 µA	50	58		V
Emitter-to-Base Breakdown Voltage	BV_{EBO}	I_E = 10 µA	5	7.6		V
Collector Cutoff Current	I_{CEO}	V_{CE} = 18 V	0	2	100	nA
Collector-to-Emitter Saturation Voltage	$V_{CE\ SAT}$	I_B = 200 µA, I_C = 2 mA	0	20	200	mV
Base-to-Emitter Voltage	V_{BE}	V_{CE} = 3 V, I_C = 200 µA	650	680	700	mV
Static Forward Current-Transfer Ratio	β (h_{FE})	V_{CE} = 3 V, I_C = 2 mA	80	125	500	
Early Voltage	V_A			–150		V

Electrical Characteristics (cont'd)

All parameters measured at 25° C.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
AS1700-PNP: Lateral PNP						
Collector-to-Emitter Breakdown Voltage	LV_{CEO}	I_E = 100 µA	30	50		V
Field-Effect Threshold Voltage	VTF	I_E = 10 µA		36		V
P + to Substrate Leakage	I_{SUB}	I_E = 100 µA, V_B = 1 V	0	150	500	nA
Collector Cutoff Current	I_{CEO}	V_{CE} = 18 V	0	2	100	nA
Collector-to-Emitter Saturation Voltage	$V_{CE\ SAT}$	I_B = 10 µA, I_E = 100 µA	0	150	200	mV
Base-to-Emitter Voltage	V_{EB}	V_{EC} = 3 V, I_E = 100 µA	630	690	700	mV
Static Forward Current-Transfer Ratio	β (h_{FE})	V_{EC} = 3 V, I_E = 100 µA	20	60	300	
Early Voltage	V_A			–105		V
Transistor Matching (measuring Δ I_E)		I_E = 200 µA	–10	<1	10	%
Double Collector Matching (meas. Δ I_E)		I_E = 200 µA	–10	<1	10	%
AS1700-PWR: Vertical PNP						
Collector-to-Emitter Breakdown Voltage	LV_{CEO}	I_E = 100 µA	30	50		V
Collector Cutoff Current	I_{CEO}	V_{CE} = 18 V	0	2	100	nA
Collector-to-Emitter Saturation Voltage	$V_{CE\ SAT}$	I_B = 10 µA, I_E = 100 µA	0	150	200	mV
Base-to-Emitter Voltage	V_{EB}	V_{EC} = 3 V, I_E = 100 µA	650	680	700	mV
Static Forward Current-Transfer Ratio	β (h_{FE})	V_{EC} = 3 V, I_E = 100 µA	20	125	500	

Typical Performance Curves

Minimum NPN

BETA vs I_C Over Temperature
(–55° C to 125° C)

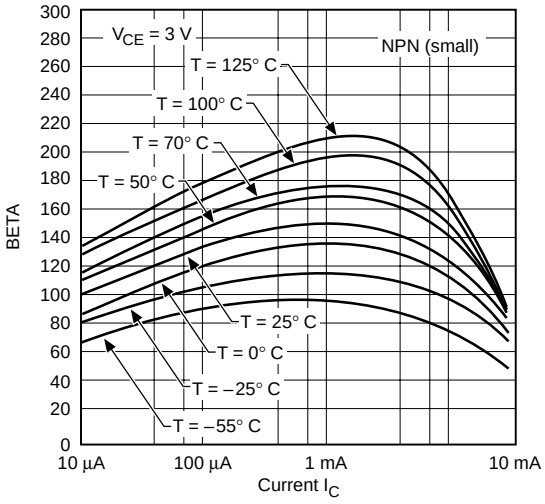


Figure 19

V_{EBO} Breakdown Voltage vs Temperature

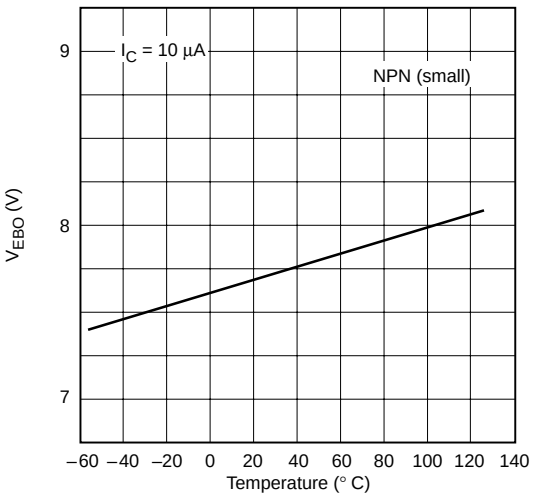


Figure 20

$V_{CE\ SAT}$ vs I_C Over Temperature
(–55° C to 125° C)

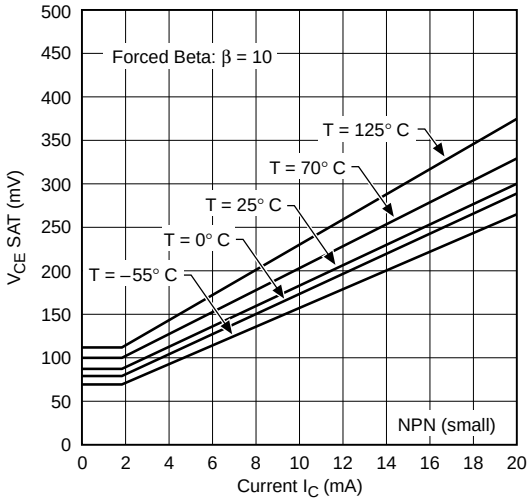


Figure 21

$V_{BE\ SAT}$ vs I_C Over Temperature
(–55° C to 125° C)

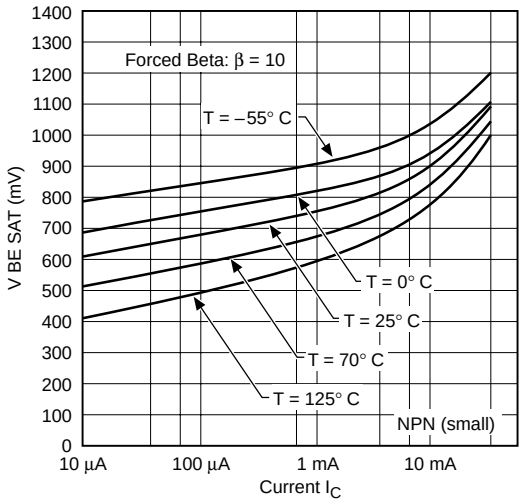


Figure 22

Typical Performance Curves

V_{BE} vs I_C Over Temperature
(–55° C to 125° C)

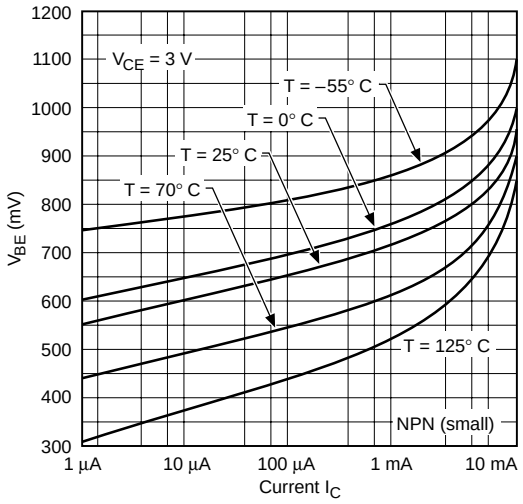


Figure 23

V_{BE} vs Temperature with Different I_C

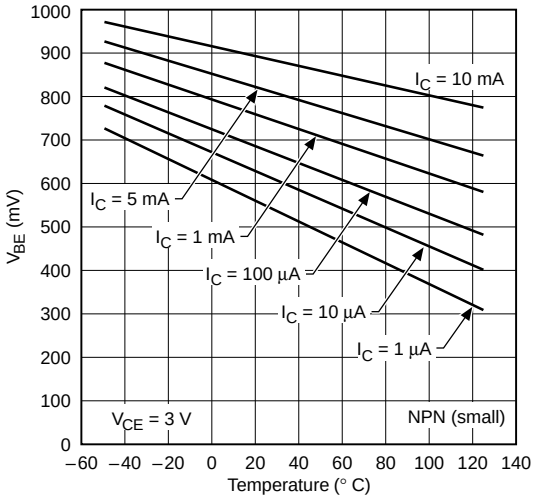


Figure 24

BETA vs I_C Over Temperature
(–55° C to 125° C)

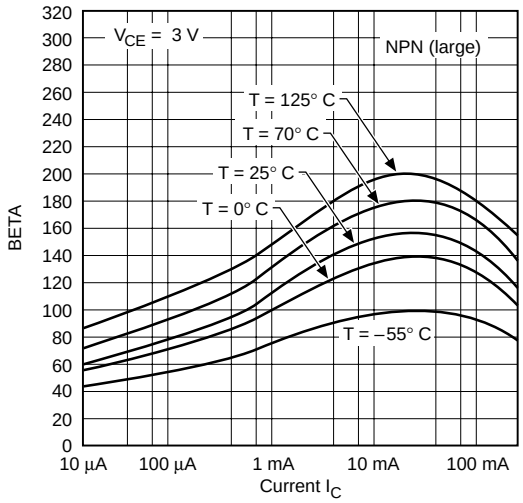


Figure 25

V_{EBO} Breakdown Voltage vs Temperature

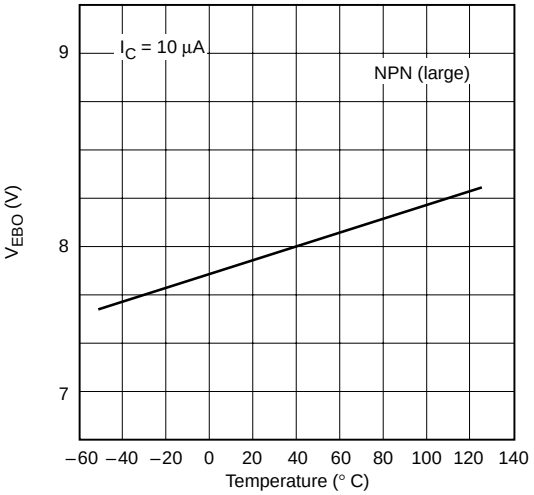


Figure 26

Typical Performance Curves

$V_{CE\ SAT}$ vs I_C Over Temperature
(–55° C to 125° C)

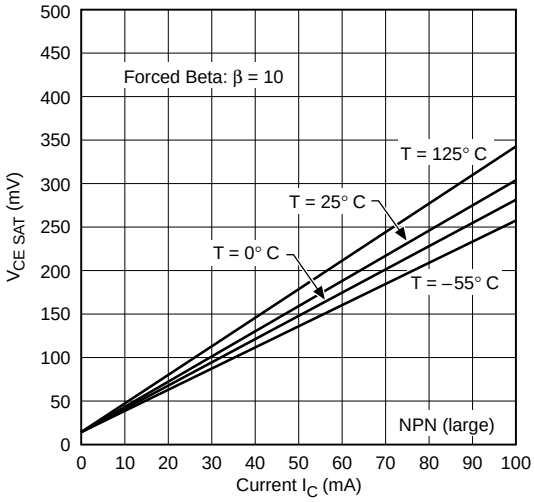


Figure 27

$V_{BE\ SAT}$ vs I_C Over Temperature
(–55° C to 125° C)

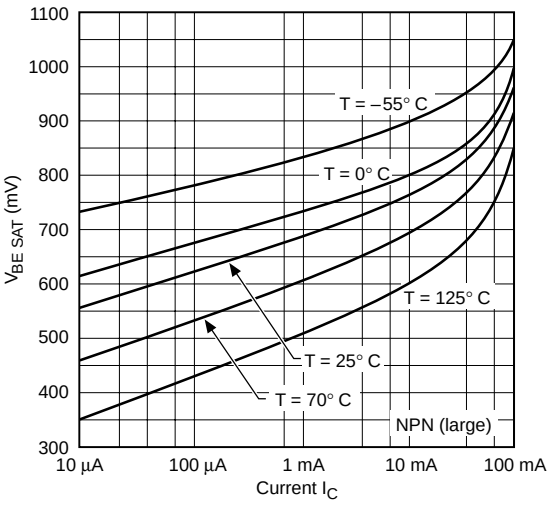


Figure 28

V_{BE} vs I_C Over Temperature
(–55° C to 125° C)

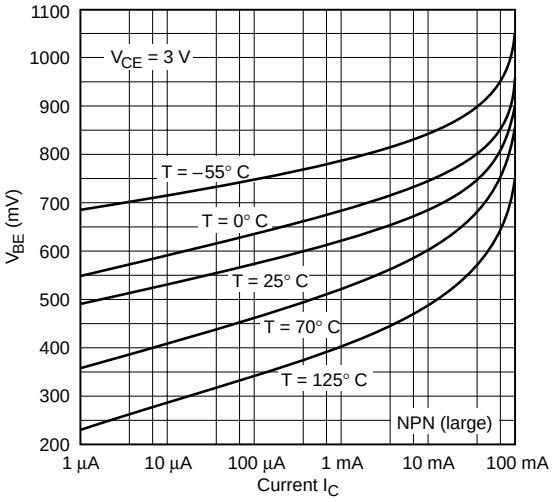


Figure 29

V_{BE} vs Temperature with Different I_C

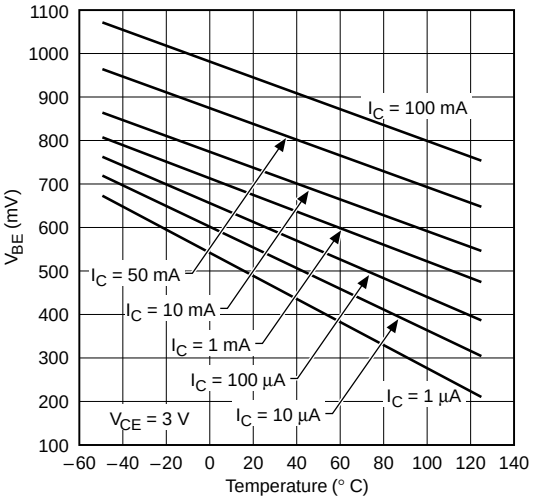


Figure 30

Typical Performance Curves

BETA vs I_E Over Temperature
(–55° C to 125° C)

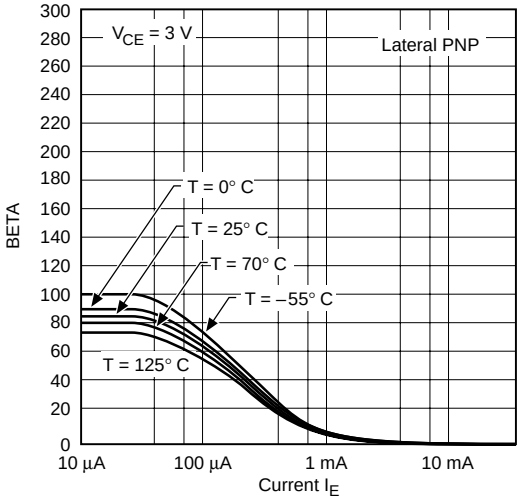


Figure 31

BETA vs I_E Over Temperature
(–55° C to 125° C)

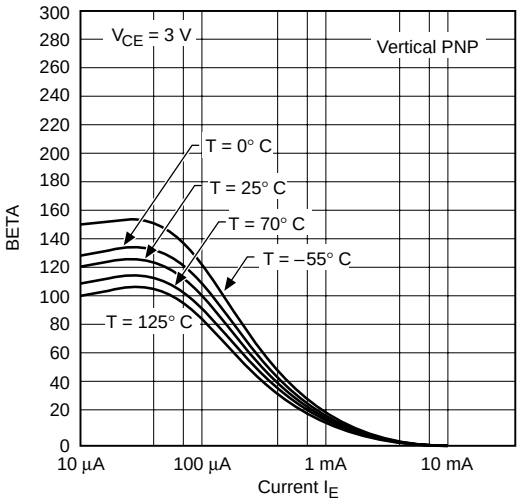


Figure 32

$V_{CE\ SAT}$ vs I_C

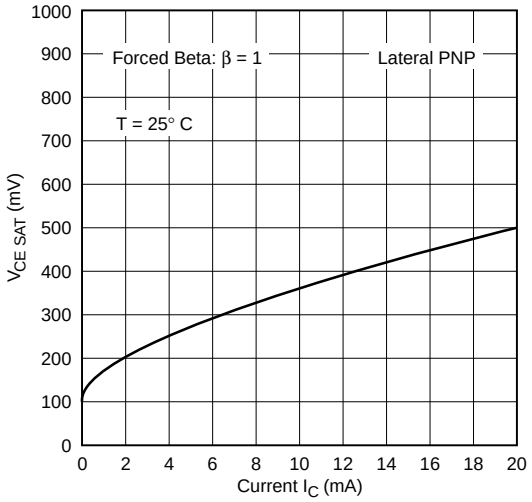


Figure 33

$V_{BE\ SAT}$ vs Temperature
(With different I_C)

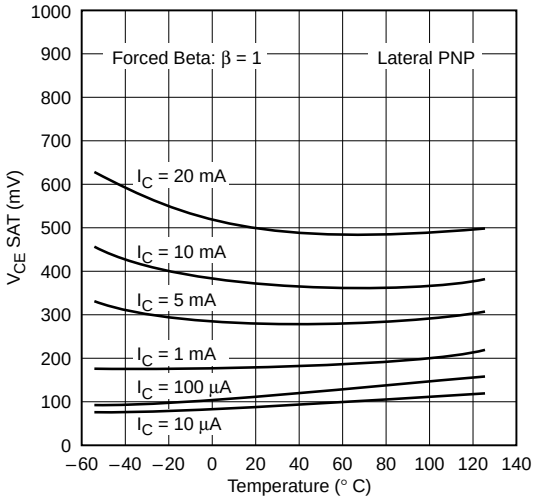


Figure 34

Typical Performance Curves

V_{BE} vs I_C Over Temperature
(–55° C to 125° C)

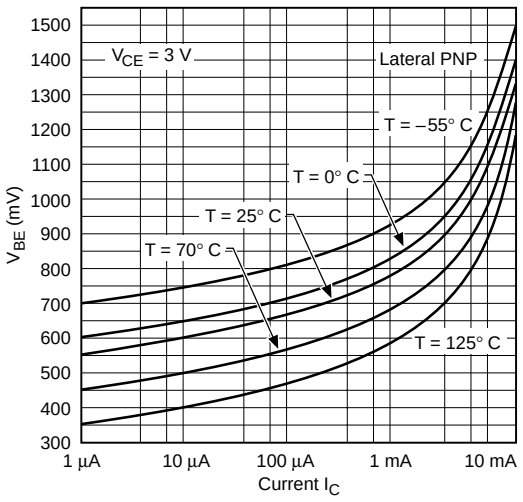


Figure 35

V_{BE} vs I_C Over Temperature
(–55° C to 125° C)

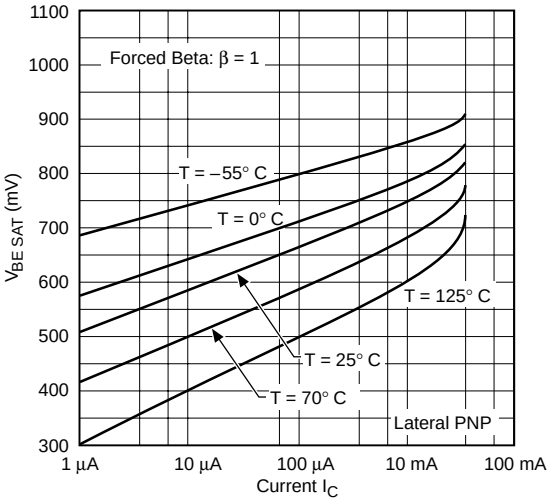


Figure 36

The Semicustom Application

The Design Considerations

The designer should take advantage of the resistor and transistor matching available with ICs and not rely on the absolute values of parameters. If a certain emitter area is desired for current ratioing, several transistors can be connected in parallel to simulate this condition, or by using the desired emitter area of an NPN power device (when breadboarding use the previous method). When using the double-collector PNP transistors, do not float one of the collectors; either tie them together or tie one to the substrate. Floating one of the collectors will severely reduce the beta. There are several values and types of resistors available on the AS17xx semicustom array as outlined in the resistor summary.

Resistor Summary

8 - Pinch Resistors
(≈30 kΩ ± 50%, use at ≤ 5 V)

80 - Base String Resistors
Using full string lengths gives:
73 – 4 kΩ
7 – 1.5 kΩ
Using separate pieces of the strings gives:
67 – 500 Ω
63 – 1 kΩ
43 – 2 kΩ
30 – 4 kΩ

Note: Do not try to use one resistor string for more than one resistor unless they are connected together in the circuit.

Additional components and their resistances are as follows:

13 - Cross-unders (370 Ω for full length, and 190 Ω for half length)

6 - Buses (at 10 Ω between connection points)

Non-Integratable Components

Identify all non-integratable components such as inductors and capacitors. These will have to be supplied with external components. Note that junction capacitors can be formed using transistors with collector and emitter tied together for limited capacitance values.

Minimizing Stray Effects (Parasitics, Currents, and Capacitance)

The following steps are recommended:

1) Try to keep substrate currents as low as possible (under a few mA) to prevent isolation loss and cross-talk between adjacent components. If a component has a high substrate current, try to isolate it from the other components and keep it as close to the substrate bonding pad as possible. The substrate current should be measured for either each kit part or the whole breadboard (with all the substrates tied together) using a 10 Ω resistor connected to the most negative potential in the circuit.
2) Do not saturate any PNP. If this is unavoidable, limit the base current so that the substrate current in the kit part lead is kept low. This is because of the parasitic vertical PNP formed between the emitter, base and substrate in a lateral PNP will become active when the lateral PNP is saturated.
3) Do not use any diode-connected PNP over about 500 μA to avoid the above mentioned parasitic PNP.
4) Contact the N-layer (collector-plug) in the resistor-tubs to the most positive potential (this is for resistor-tub biasing and isolation, and is a concern only for the semicustom implementation of the circuit), and the substrate to the most negative potential in the circuit.
5) High-frequency oscillations can, on rare occasions, occur in the integrated circuit when the breadboard did not show any tendency toward oscillation. This can be caused by the stray capacitances in the breadboard, which are larger than those associated with the IC and tend to stabilize potentially unstable circuits. Therefore, every effort should be made to minimize stray capacitances in the breadboard. This can be done by using DIP sockets and soldered wire or printed circuit interconnects rather than the popular solderless plug-in breadboards which have up to 10 pF of pin-to-pin capacitance.

Breadboarding with Kit Parts

All circuits should be breadboarded before being implemented on the semicustom array using AS1700 Kit Parts, (which are transistor arrays made using the AS17xx semicustom array). This breadboard will simulate as accurately as possible all stray effects and how the circuit will perform when implemented with the semicustom array. We recommend that standard carbon resistors be used to simulate the integrated resistors, or precision thin film resistors if accurate ratios are required.

Evaluating your breadboard

After obtaining satisfactory performance from the breadboard, evaluate the effects of resistor, transistor and temperature variations.

We recommend simulating the worst-case resistance variations (which is 30% globally and 1% for matching and ratioing) on the breadboard by substituting the appropriate values for all resistors. Sensitivity to transistor parameter variations can be seen by interchanging kit parts. We also recommend that the breadboard be tested over the full operating temperature range of the circuit.

After testing is complete, make sure that the breadboard circuit is accurately reflected in the schematic by doing a thorough check to see if all modifications to the breadboard are included.

Layout options

After thoroughly testing the breadboard, begin the layout process. There are three options for doing the layout:

- **Customer layout** - You do the layout and provide Astec with a completed layout sheet (at 500x - which Astec will provide) ready for entry into our CAD system. Astec will review the layout for design rule violations and advise you so that you can correct them yourself or elect to have Astec fix them.
- **Vendor layout** - You may assign Astec the responsibility of the IC layout.
- **Customer supervised layout** - You assign the layout implementation to Astec but retain the responsibility for the final form and content. Basically you are subcontracting Astec to do the IC layout under your direction. This option requires a great deal of communication between the customer and Astec, but can yield the greatest control for the customer while reducing the layout time.

Layout guidelines

We recommend that several copies of the layout on the data sheet be made to facilitate the layout process before working with the 500x layout sheet. The layout copies can be used to sketch various interconnect options, and work out any design problems that may be encountered because of the layout process.

Functional blocks: We recommend that the circuit be broken down into functional blocks. The blocks are selected in such a way as to minimize the the number of interconnections with the other blocks. If the blocks are in sequence, the circuit can usually be divided so that only one or two connections are made between the blocks (other than power supply connections).

Block location: Next, add up the number of devices and pads required by each block. Then select an area of the chip for each block. There are a few considerations which must be kept in mind for the block placement. First, the selected area must contain the required number of components and pads. Second, the various areas should be located so that interconnections between them are as easy as possible. Finally, the locations of the various pads to be bonded to pins and their relationships to each other and the blocks should be considered. Bond wires should not cross each other.

Cross-unders & buses: Cross-unders can be useful for small resistance values, but be careful of connections that can not tolerate cross-under resistance (see resistor summary), such as the base connections for a diode-biased current source, etc. To make sure that a connection can tolerate the cross-under resistance, insert the appropriate valued resistor in the breadboard and evaluate its effect on circuit performance. Buses have low resistance and are valuable for connecting functional blocks together, and busing power supply voltages.

Thermal considerations: If one or more components dissipate heat, they should be located away from other components that require close matching. The matched components should be placed together an equal distance from the thermal source. This way both of the matched components will be heated equally. Total power dissipation in the circuit is a function of the package type and size. On average at least 500 mW can be dissipated without trouble. Larger packages can dissipate more heat.

Signal & common coupling: If high frequency signals are present which have large amplitude swings, these lines should be separated as much as possible with respect to their pin locations because of inductive or capacitive coupling between their pins and bonding wires.

Another coupling problem arises when there are long metal lines. For example, if there is a common ground line for both the input and output of an amplifier, the fluctuating current from the output could cause a voltage drop along the line that could effect the input. This coupling could cause distortion or oscillations. The solution to this problem is to run two separate ground lines to the ground pad.

Resistor ratioing: Where matched resistor values or precise ratios are required, identical resistor constructs and orientations should be used. Identical resistors orientated 90° to each other may have different values due to directionally dependent fabrication and packaging tolerances.

Component interconnection: We recommend numbering the components on the circuit schematic and using these numbers on the layout. Work on only one circuit block at a time and leave the block interconnections until all the blocks are finished. Start the layout by selecting several components of a block and placing them on the layout; sketch their interconnections and work outward marking the schematic as you go.

Metal routing: The metal routing can be sketched on the layout sheet taking into account the design rule considerations as follows:

Design Rules:

- Minimum metal width = 8 microns
- Minimum spacing between metal traces = 8 microns
- Current capacity of metal trace = 4 mA per micron of width
- Metal line to pad (active) = 24 microns (note: metal resistance ≈ 0.02 Ω per square)

The area around the outside of the chip has a metalized ring with numerous contacts to the substrate. The substrate must be connected to the most negative potential in the circuit. When laying out the circuit, the ground conductors should lead inward from the outer ring. There are several N-layer contacts for the different resistor tub areas that must be connected to the most positive potential in the circuit to maintain isolation.

Bonding pads: The rules for bonding pad layouts are very simple. You must be able to draw a straight line from a bonding pad to its pin without crossing any other wires, and the pads should be evenly spaced around the chip. The pin assignments are arbitrary, but they should be organized such that the pin numbers correspond to the pads in a counter-clockwise rotation around the chip, and not some random pattern that would cause bonding wires to cross each other.

Layout sheets (500x) are available upon request for final layout, and are used to make the metal interconnect mask and check spacing rules. We recommend that the metal interconnect be done on a clear film over the layout sheet with erasable markers before making the final layout. This will allow for modifications to be made with a minimum amount of effort.

Functional Circuit Blocks

The following circuits are presented as a guide to assist in circuit design using the AS17xx Semicustom Array.Complex circuit functions can be created from these elementry building blocks.These circuit blocks can be modified and improved to suit the designer's needs in creating a complete system.

Current Sources

Here are a few examples of PNP current sources; NPN current sinks can easly be derived from the analog of these PNP examples.

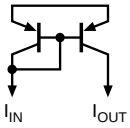


Figure 2. Simple PNP Current Source. Has Slower Frequency Response, and up to ±15% Tolerance Error.
$I_{OUT} = I_{IN} * (1 + 2/\beta)$

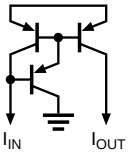


Figure 3. Widlar Current Source, Moderate Frequency Response.
$I_{OUT} = I_{IN} * (1 + 2/\beta^2)$

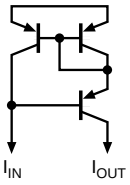


Figure 4. Wilson Current Source, Fast Frequency Response.
$I_{OUT} = I_{IN} * (1 + 1/2\beta^2)$

Comparator Input Stages

Several comparator input stages are illustrated below.

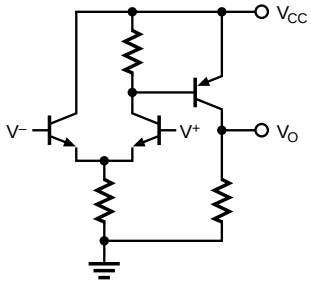


Figure 5. Simple NPN Type Comparator.

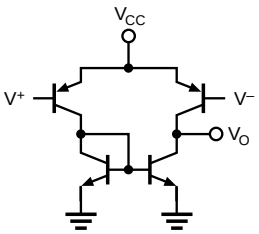


Figure 6. Simple NPN Type Comparator Input Stage.

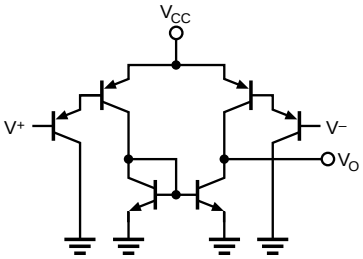


Figure 7. Improved PNP Type (Good GND Sensing) Comparator Input Stage.

Functional Circuit Blocks

Voltage Regulators/References

Figure 8. Zener Diode V_Z = 7 V

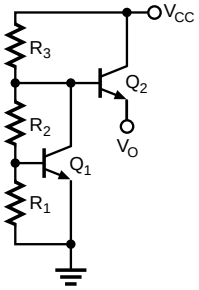


Figure 9. V_{BE} Multipled Regulator.
$V_{OUT} = V_{BE} * R2 / R1$

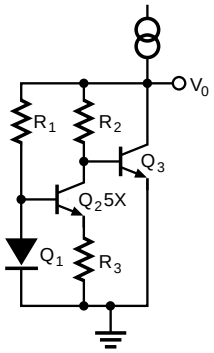


Figure 10. Widlar Band Gap Reference.
$\Delta V_{BE} = V(R3) = V_T * \ln (A2/A1)$
$V_{OUT} = V_{BE}(Q3) + (R2/R3) * \Delta V_{BE}$

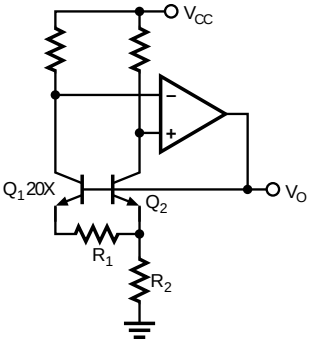


Figure 11. Brokaw Band Gap Reference.
$\Delta V_{BE} = V(R1) = V_T * \ln (A1/A2)$
$V_{OUT} = V_{BE}(Q2) + V(R1) * 2 * R2/R1$

Functional Circuit Blocks

Flip-Flop

Here are two examples of flip-flop circuits.

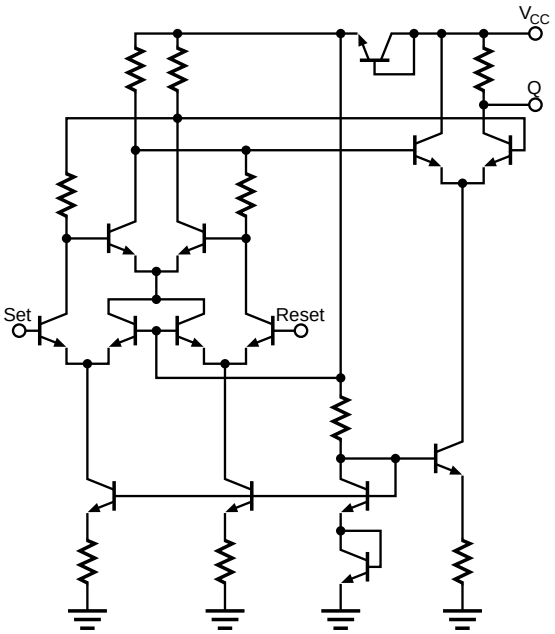


Figure 17. Fast, ECL Flip-Flop

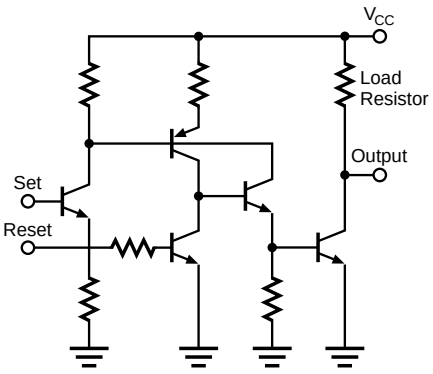


Figure 18. Four Layer Latch Flip-Flop

Functional Circuit Blocks

Trimming Schemes

There often arises the need to trim a parameter (i.e. voltage, current, oscillator frequency, offset null, etc.) to some particular value because of processing variations involved with wafer fabrication. We have developed two methods to accomplish this goal: 1) fuse link, where a fuse is blown to cause an open; and 2) zener zap, where a zener is taken well into breakdown until a short occurs.

Fuse Link

Fuse links can be used similar to zeners for trimming, but the fuses must be located on a bonding pad inside the pad cut because a fuse won't blow if there is passivation over it. One possible trim scheme using fuse links is shown below.

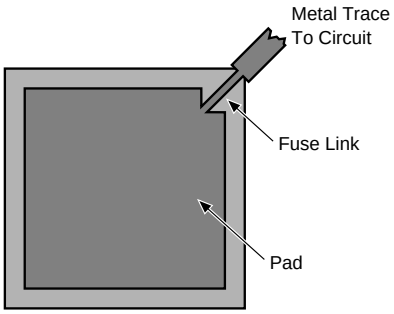


Figure 12.

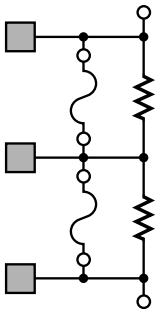


Figure 13.

Zener Zap

When using zener zap trim methods there are several points to keep in mind: the zener should be located near a pad, no cross-unders should be used to connect the zener with the pad, and the metal lines connecting the pad to the zener should be as thick as possible to allow the high current necessary to blow the zener. A few examples of the many possible trim schemes are shown in Figure 14, Figure 15 and Figure 16.

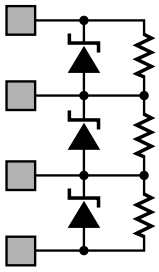


Figure 14. Simple Trim Setup with 8 Trim Steps.

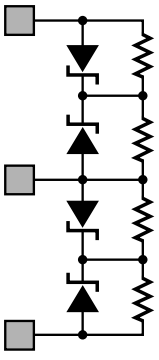


Figure 15. Trim Scheme Using Only 3 Pads to Get 16 Trim Steps.

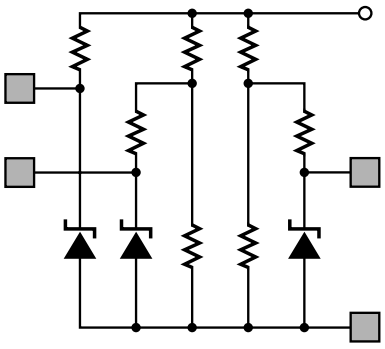


Figure 16. Parallel Trim Scheme with 8 Trim Steps.

Spice Models:

```
.MODEL Nmin NPN; Minimum NPN
+ (IS = 0.5FA   BF = 200   NF = .995   VAF = 100   IKF = 20M   NE = 1.45
+ EG = 1.185  BR = 5  NR = 0.98  VAR = 30  IKR = 2M  XTB = 0.3
+ RB = 270  RC = 60  RE = 7  TRB1 = 1.5M  XTI = 2.5
+ CJE = 450FF  VJE = 0.85  MJE = 0.36  TF = 300PS
+ CJC = 200FF  VJC = 0.57  MJC = 0.47
+ CJS = 1.4PF  VJS = 0.31  MJS = 0.35)

.MODEL Plat LPNP; Lateral PNP
+ (IS = 0.9FA  BF = 80  NF = 1  IKF = 60U  NE = 1.5
+ EG = 1.2  BR = 30  NR = 0.98  IKR = 2M
+ RB = 30  RC = 200  RE = 15  TRC1 = 1.5M  TRE1 = 1.5M
+ VAF = 45  VAR = 30
+ CJE = 150FF  VJE = 0.57  MJE = 0.47  TF = 30NS
+ CJC = 950FF  VJC = 0.57  MJC = 0.47  XTB = 0.5
+ CJS = 1.4PF  VJS = 0.31  MJS = 0.35)

.MODEL Pvert LPNP; Vertical PNP
+ (IS = 0.9FA  BF = 100  NF = .995  VAF = 45  IKF = 1.5M
+ EG = 1.22  BR = 30  NR = 0.98  VAR = 30  IKR = 2M  NE = 1.25
+ RB = 350  RC = 200  RE = 300  TRC1 = 1.5M  TRE1 = 1.5M
+ CJE = 150FF  VJE = 0.57  MJE = 0.47  TF = 30NS
+ CJC = 1.6PF  VJC = 0.57  MJC = 0.47  XTB = 0.5)

.MODEL RBase RES; Base Resistor
+ (R = 1  TC1 = 2.1m  TC2 = 7u)

.MODEL RImp RES; Implant Resistor
+ (R = 1.0  TC1 = 4m  TC2 = 6u)

.MODEL RPinch RES; Pinch Resistor
+ (R = 1.0  TC1 = 7m)

.MODEL Dzener D;
+ (BV = 7.2V  IBV = 1uA  RS = 270  IS = .1fA)
```

Component Summary

Components Available (single tile):

Small NPN:	48
Dual collector PNP:	21
Vertical PNP	4
Power NPN	3
Diffused Resistors (total)	≈300 kΩ
Pinch Resistors (3-terminal, 30kΩ)	8
Cross-unders	13
Buses	6

Resistor Summary

Resistor Summary:

8 - Pinch Resistors
(≈30 kΩ ± 50%, use at ≤ 5 V)

80 - Base String Resistors
Using full string lengths gives:
73 - 4 kΩ
7 - 1.5 kΩ
Using separate pieces of the strings gives:
67 - 500 Ω
63 - 1 kΩ
43 - 2 kΩ
30 - 4 kΩ

Additional components and their resistances are as follows:

13 - Cross-unders (370 Ω for full length, and 190 Ω for half length)

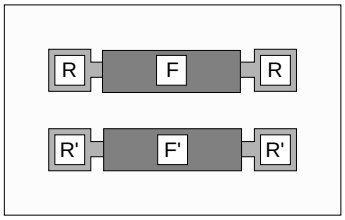
6 - Buses (at 10 Ω between connection points)

Design Rules

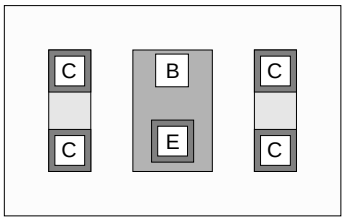
Design Rules:

- Minimum metal width = 8 microns
- Minimum spacing between metal traces = 8 microns
- Current capacity of metal trace = 4 mA per micron of width
- Metal line to pad (active) = 24 microns (note: metal resistance ≈ 0.02 Ω per square)

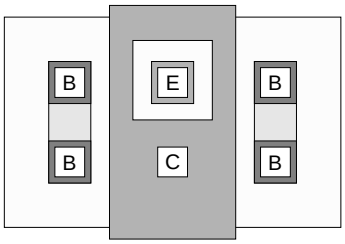
Device Layout



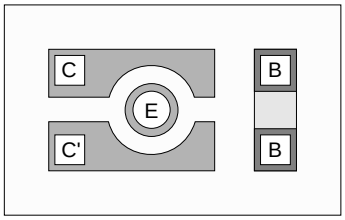
Pinch Resistor with Field Contact



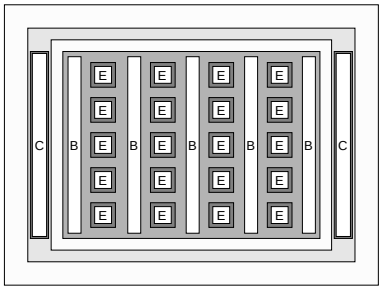
Minimum NPN



Vertical PNP

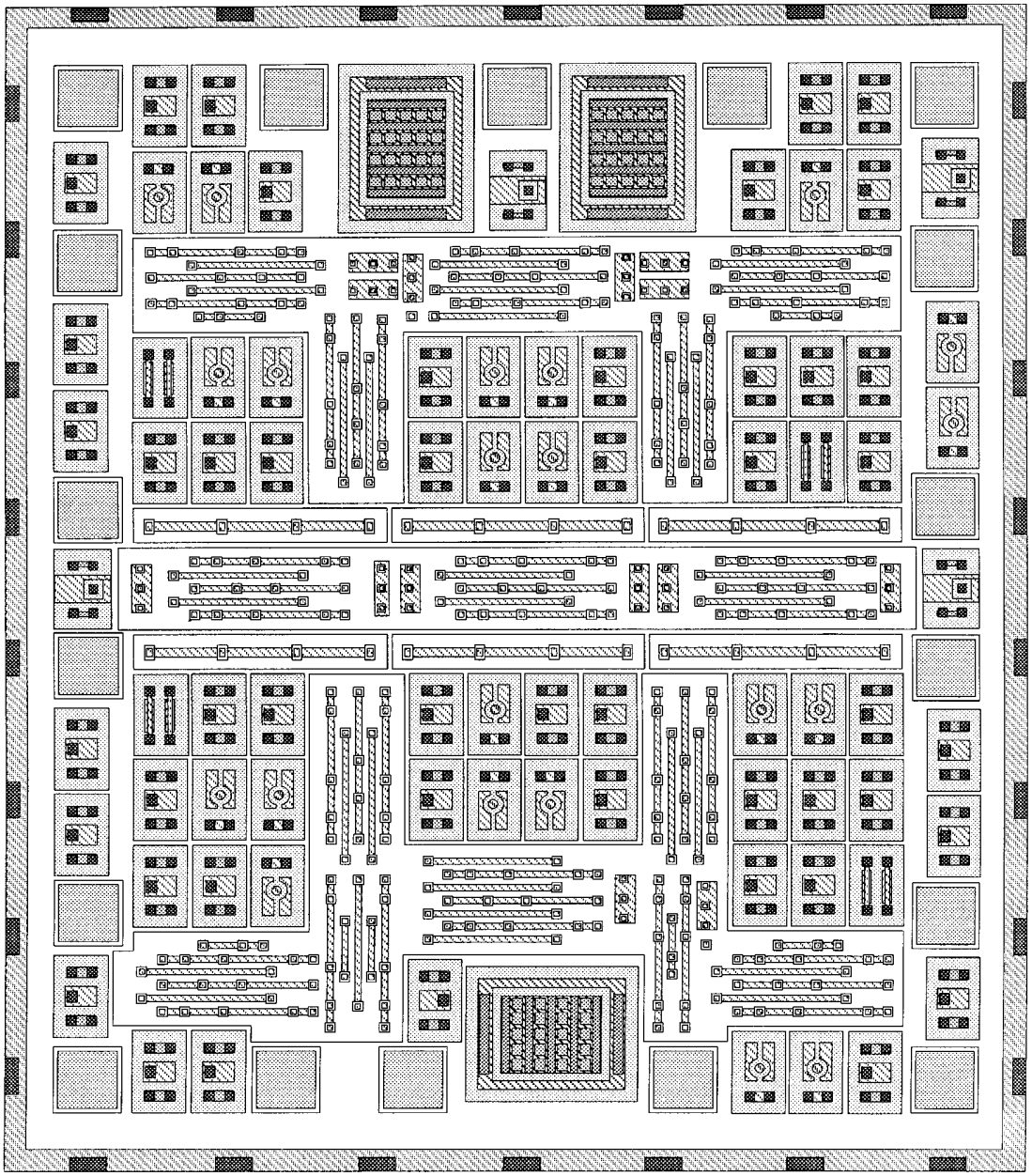


Lateral PNP with Split Collector



Power (20x) NPN

Device Layout



Notes