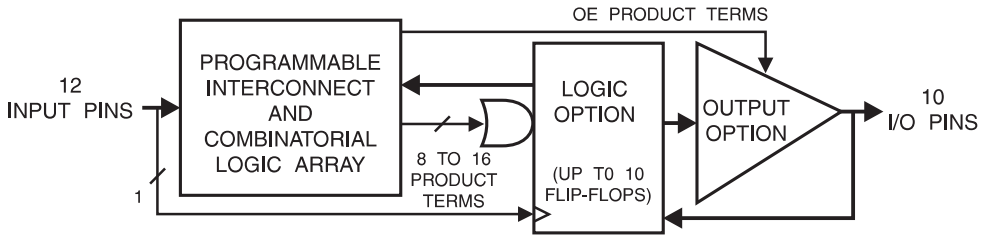
Features

- **Third Generation Programmable Logic Structure**
  - **High-Density Replacement for Discrete Logic**
- **High-Speed — Plus a New, Low-Power Version**
- **Increased Logic Flexibility**
  - **42 Inputs and 20 Sum Terms**
- **Flexible Output Logic**
  - **20 Flip-Flops - 10 Extra**
  - **All Can Be Individually Buried or 10 Output Directly**
  - **Each has Individual Asynchronous Reset and Clock Terms**
- **Multiple Feedback Paths Provide for Buried State Machines and I/O Bus Compatibility**
- **Proven and Reliable High-Speed CMOS EPROM Process**
  - **2000V ESD Protection**
  - **200 mA Latchup Immunity**
- **Reprogrammable**
  - **Tested 100% for Programmability**
- **24-pin, 300-mil Dual-In-line and 28-Lead Surface Mount Packages**

Logic Diagram



Description

The ATV750(L) is 100% more powerful than most other programmable logic devices in 24-pin packages. Increased product terms, sum terms, and flip-flops translate into more usable gates.

Each of the ATV750(L)'s twenty-two logic pins can be used as an input. Ten of these can be used as input, output, or bi-directional I/O pins. All twenty flip-flops can be fed back into the array independently. This flexibility allows burying all of the sum terms and flip-flops.

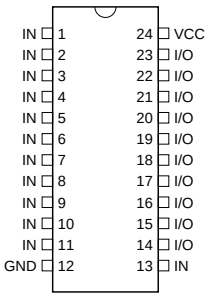
There are 171 product terms available. A variable format is used to assign between four and eight product terms per sum term. There are two sum terms per output, providing added flexibility.

(continued)

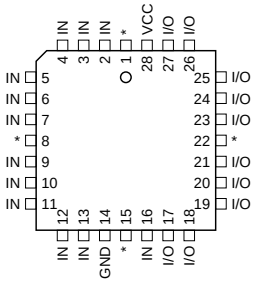
Pin Configurations

Pin Name	Function
IN	Logic Inputs
I/O	Bidirectional Buffers
*	No Internal Connection
VCC	+5V Supply

DIP/SOIC



PLCC/LCC
(Top View)



High Density UV Erasable Programmable Logic Device

ATV750
ATV750L

Rev. 0024E–05/98

The ATV750(L) has more flip-flops available than other PLDs in this density range. Complex state machines are easily implemented.

Product terms are available providing asynchronous resets, flip-flop clocks, and output enables. One reset and one clock term are provided per flip-flop, with one enable term per output. One product term provides a global synchronous preset. Register preload simplifies testing. The device has an internal power up clear function.

Absolute Maximum Ratings

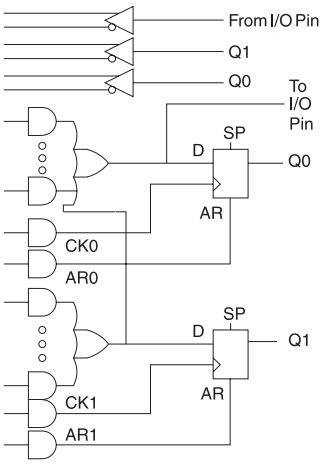
Temperature Under Bias	-55°C to + 125°C
Storage Temperature	-65°C to + 150°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V(1)
Voltage on Input Pins with Respect to Ground During Programming	-2.0V to +14.0V(1)
Programming Voltage with Respect to Ground	-2.0V to +14.0V(1)
Integrated UV Erase Dose	7258 W.sec/cm^2

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

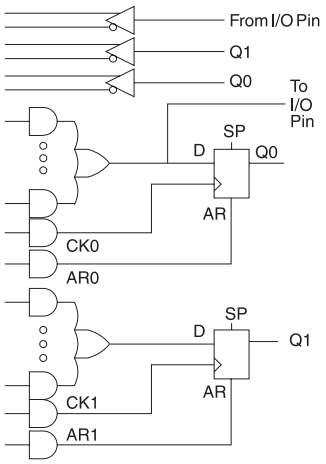
Note: 1. Minimum voltage is -0.6V DC, which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is Vcc + 0.75V DC, which may overshoot to 7.0V for pulses of less than 20 ns.

Logic Options

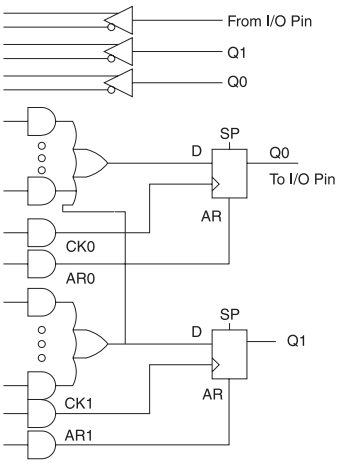
Combined Terms



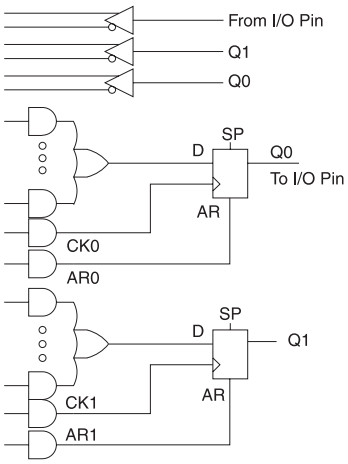
Separate Terms



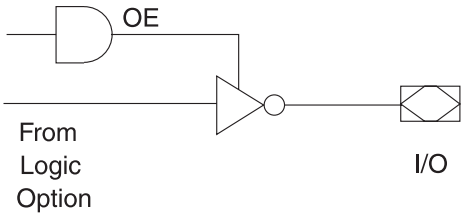
Combined Terms

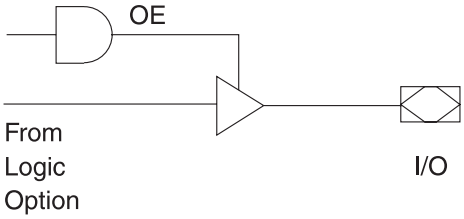


Separate Terms



Output Options





DC and AC Operating Conditions

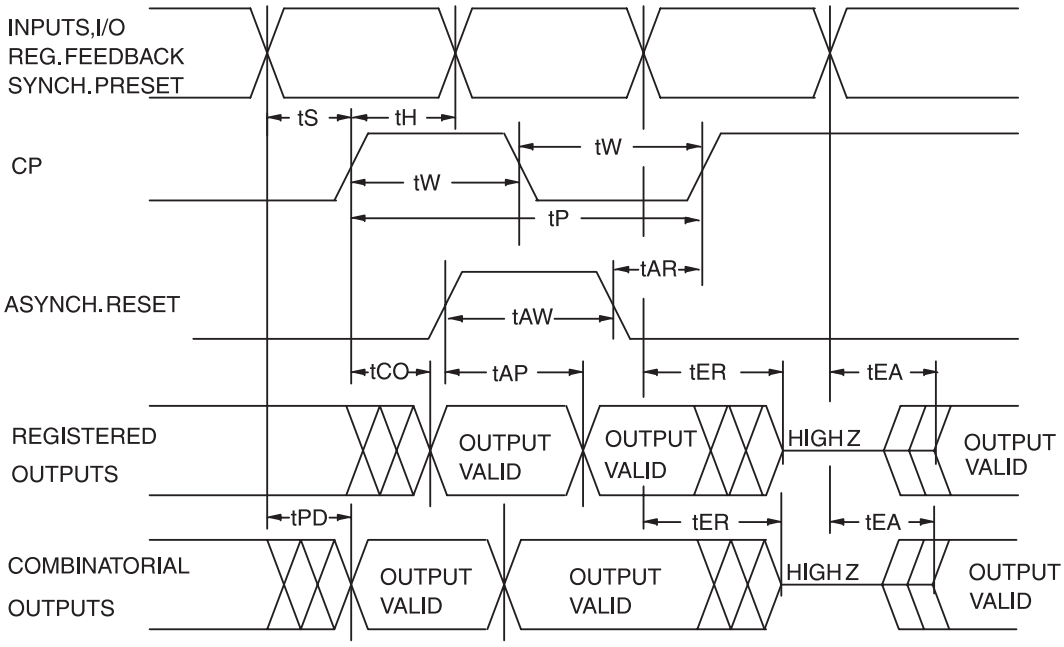
		ATV750-20	ATV750/750L-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C
	Mil.	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5V ± 10%	5V ± 10%

DC Characteristics

Symbol	Parameter	Condition			Min	Typ	Max	Units
I_{LI}	Input Load Current	V_{IN} = -0.1V to V_{CC} + 1V					10	µA
I_{LO}	Output Leakage Current	V_{OUT} = -0.1V to V_{CC} + 0.1V					10	µA
I_{CC}	Power Supply Current	V_{CC} = MAX, V_{IN} = GND, Outputs Open	ATV750	Com.			120	mA
				Ind.,Mil.			140	mA
			ATV750L	Com.		1.0	12	mA
				Ind.,Mil.		1.0	15	mA
I_{OS}[1]	Output Short Circuit Current	V_{OUT} = 0.5V					-120	mA
V_{IL}	Input Low Voltage				-0.6		0.8	V
V_{IH}	Input High Voltage				2.0		V_{CC} + 0.75	V
V_{OL}	Output Low Voltage	V_{IN} = V_{IH} or V_{IL}, V_{CC} = MIN	I_{OL} = 12 mA Com.,Ind.				0.5	V
			I_{OL} = 8 mA Mil.				0.5	V
			I_{OL} = 24 mA, Com.				1.0	V
V_{OH}	Output High Voltage	V_{IN} = V_{IH} or V_{IL}, V_{CC} = MIN	I_{OH} = -100 µA		V_{CC} - 0.3			V
			I_{OH} = -4.0 mA		2.4			V

Note: 1. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 sec.

AC Waveforms[1]

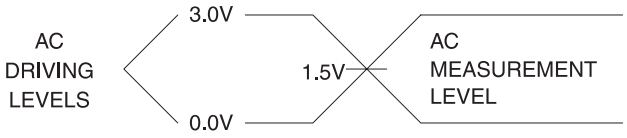


Note: 1. Timing measurement reference is 1.5V. Input AC driving levels are 0.0V and 3.0V, unless otherwise specified.

AC Characteristics

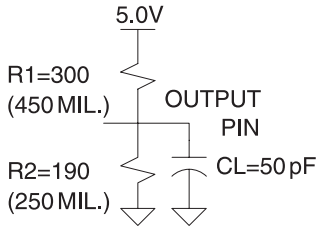
Symbol	Parameter	ATV750-20		ATV750/750L-25		Units
		Min	Max	Min	Max	
t_{PD}	Input or Feedback to Non-Registered Output		20		25	ns
t_{EA}	Input to Output Enable		20		25	ns
t_{ER}	Input to Output Disable		20		25	ns
t_{CO}	Clock to Output		20		22	ns
t_{CF}	Clock to Feedback	5	10	5	10	ns
t_{S}	Input Setup Time	10		12		ns
t_{SF}	Feedback Setup Time	5		7		ns
t_{H}	Hold Time	5		5		ns
t_{P}	Clock Period	18		22		ns
t_{W}	Clock Width	8		10		ns
F_{MAX}	Maximum Frequency		55		45	MHz
t_{AW}	Asynchronous Reset Width	15		20		ns
t_{AR}	Asynchronous Reset Recovery Time	15		20		ns
t_{AP}	Asynchronous Reset to Registered Output Reset		20		25	ns
t_{SP}	Setup Time, Synchronous Preset	12		15		ns

Input Test Waveforms and Measurement Levels

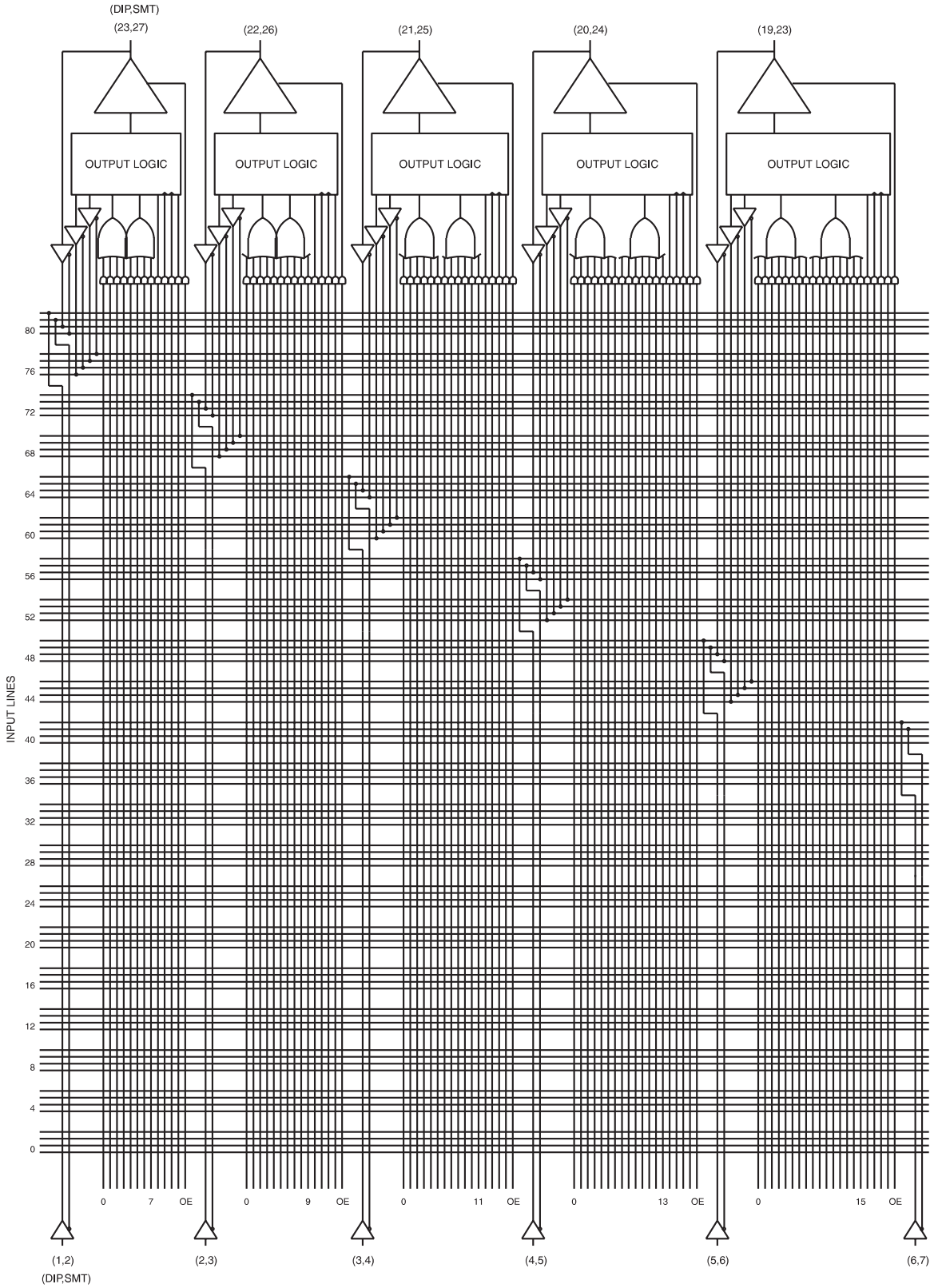


t_R, t_F < 5 ns (10% to 90%)

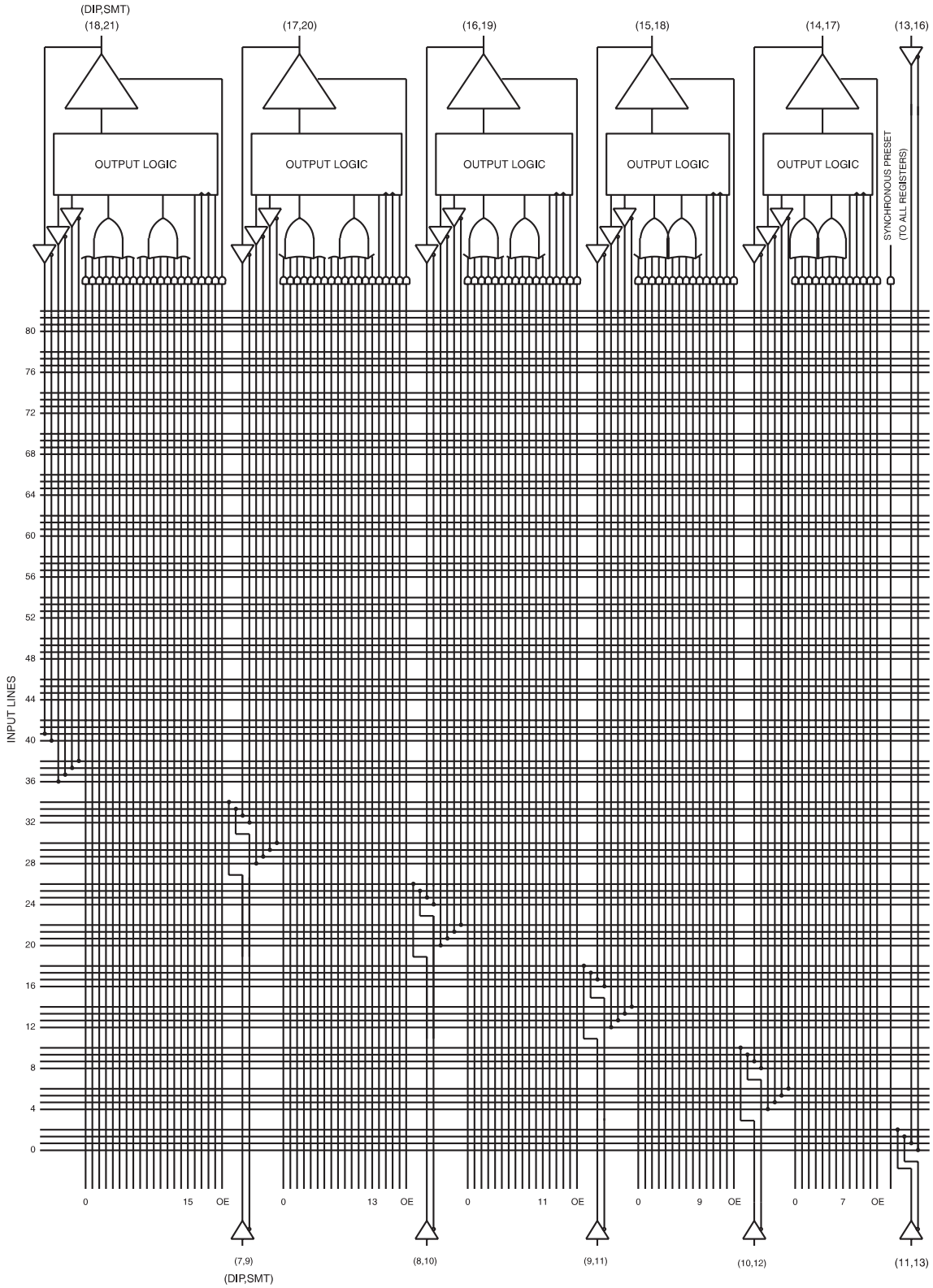
Output Test Loads



Functional Logic Diagram ATV750, Upper Half

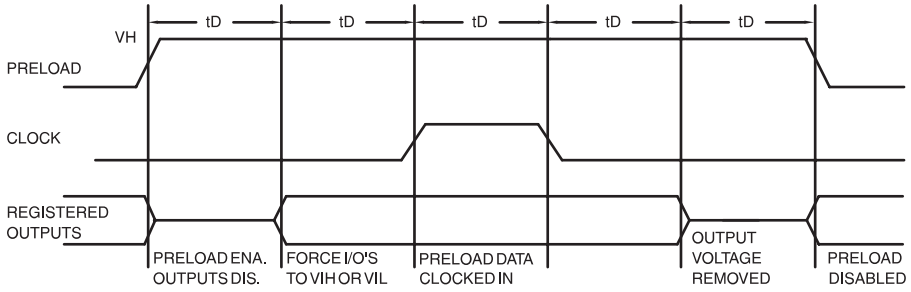


Functional Logic Diagram ATV750, Lower Half



Preload of Registered Outputs

The ATV750's registers are provided with circuitry to allow loading of each register asynchronously with either a high or a low. This feature will simplify testing since any state can be forced into the registers to control test sequencing. A V_{IH} level on the I/O pin will force the register high; a V_{IL} will force it low, independent of the output polarity. The preload state is entered by placing an 10.5V to 11.5V signal on pin 8 on DIPs, and pin 10 on SMPs. When the clock term is pulsed high, the data on the I/O pin is placed into the register chosen by the Select Pin.



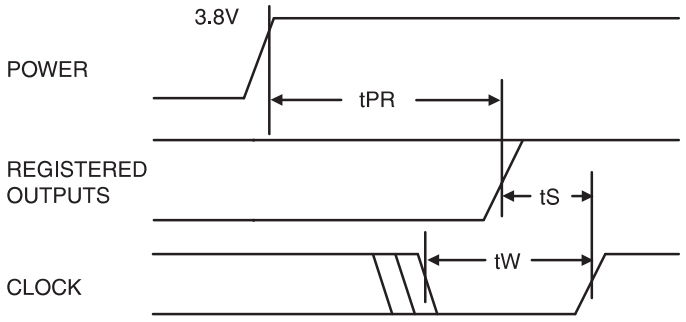
Level forced on registered output pin during PRELOAD cycle	Select Pin State	Register #1 state after cycle	Register#2 State after cycle
V_{IH}	Low	High	X
V_{IL}	Low	Low	X
V_{IH}	High	X	High
V_{IL}	High	X	Low

Power-Up Reset

The registers in the ATV750(L) are designed to reset during power up. At a point delayed slightly from V_{CC} crossing 3.8V, all registers will be reset to the low state. The output state will depend on the polarity of the output buffer.

This feature is critical for state machine initialization. However, due to the asynchronous nature of reset and the uncertainty of how V_{CC} actually rises in the system, the following conditions are required:

1. The V_{CC} rise must be monotonic,
2. After reset occurs, all input and feedback setup times must be met before driving the clock term high, and
3. The signals from which the clock is derived must remain stable during t_{PR}.



Parameter	Description	Min	Typ	Max	Units
t_{PR}	Power-Up Reset Time		600	1000	ns

Pin Capacitance (f = 1 MHz, T = 25°C)[1]

	Typ	Max	Units	Conditions
C_{IN}	**5**	**8**	**pF**	V_{IN} = 0V
C_{OUT}	**6**	**8**	**pF**	V_{OUT} = 0V

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Using the ATV750's Many Advanced Features

The ATV750's flexibility puts more usable gates in 24-pins than other PLDs. The ATV750(L) starts with an architecture similar to the popular AT22V10, and adds several features:

- **Asynchronous Clocks -**
  Each of the flip-flops in the ATV750(L) has a dedicated product term driving the clock. The user is no longer constrained to using one clock for all the registers. Buried state machines, counters, and registers can all coexist in one device, while running on separate clocks. The ATV750(L) clock period matches that of similar synchronous devices.
- **A Full Bank of 10 More Registers -**
  The ATV750(L) provides two flip-flops for each output macrocell - a total of 20. Each register has its own clock and reset product terms, as well as its own SUM term.
- **Independent I/O Pin and Feedback Paths -**
  Each I/O pin on the ATV750(L) has a dedicated input path. Each of the 20 registers has individual feedback terms into the array. This feature, combined with individual product terms for each I/O's output enable, facilitates designs using bi-directional I/O buses.
- **Combinable Sum Terms -**
  Each output macrocell's two SUM terms can be combined in an OR gate before the output or the register. This provides up to 16 product terms per output or flip-flop. This architecture increases the number of usable gates available.

Programming Software Support

Software which is capable of transforming Boolean equations, state machine descriptions and truth tables into JEDEC files for the ATV750(L) is available from several PLD software vendors. Please refer to the Software Support Information table in the *Programmable Logic Development Tools* section for more information.

Synchronous Preset and Asynchronous Reset

One synchronous preset line is provided for all 20 registers in the ATV750(L). The appropriate input signals to cause the internal clocks to go to a high state must be received during a synchronous preset. Appropriate setup and hold times must be met, as shown in the switching waveform diagram.

An individual asynchronous reset line is provided for each of the 20 flip-flops. Both master and slave halves of the flip-flops are reset when the input signals received combine so as to force the internal resets high.

Security Fuse Usage

A single fuse is provided to prevent unauthorized copying of the ATV750(L) fuse patterns. Once programmed, the output buffers will remain in a high impedance state during verify.

The security fuse should be programmed last, as its effect is immediate.

Erasure Characteristics

The entire memory array of an ATV750(L) is erased after exposure to ultraviolet light at a wavelength of 2537 Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000 $\mu W/cm^2$ intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of 15 $W \cdot sec/cm^2$. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable PLD which will be subjected to continuous fluorescent indoor lighting or sunlight.

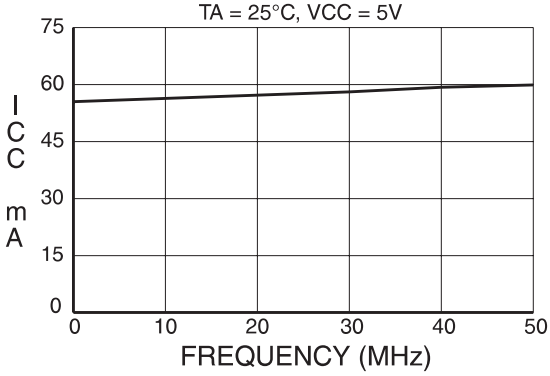
Atmel CMOS PLDs

Atmel's Programmable Logic Devices utilize an advanced 1.5-micron CMOS EPROM technology. This technology's state of the art features are the optimum combination for PLDs:

- CMOS technology provides high speed, low power, and high noise immunity.
- EPROM technology is the most cost effective method for producing PLDs - surpassing bipolar fusible link technology in low cost, while providing the necessary reprogrammability.
- EPROM reprogrammability, which is 100% tested before shipment, provides inherently better programmability and reliability than one-time fusible PLDs.
- Atmel's EPROM process has proven extremely reliable in the volume production of a full line of advanced EPROM memory products, from 64K to one-megabit devices.

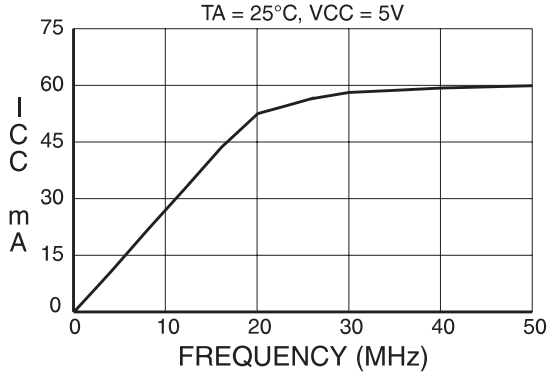
V750 ICC vs FREQUENCY

TA = 25°C, VCC = 5V



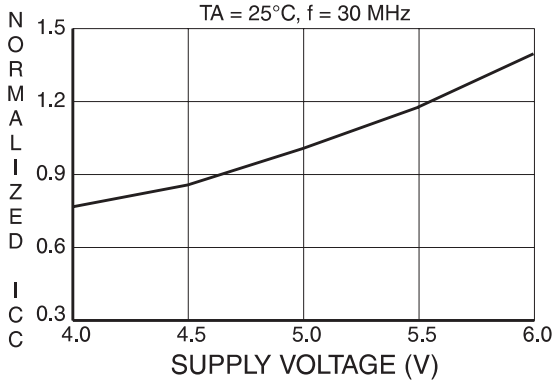
V750L ICC vs FREQUENCY

TA = 25°C, VCC = 5V



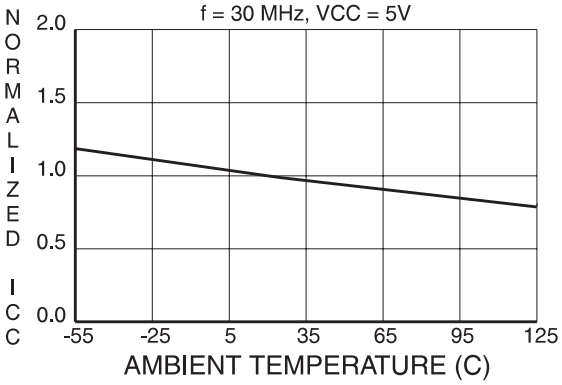
NORMALIZED ICC vs. VCC

TA = 25°C, f = 30 MHz



NORMALIZED ICC vs. AMBIENT TEMP.

f = 30 MHz, VCC = 5V



Ordering Information

t_{PD} (ns)	t_{CO} (ns)	f_{MAX} (MHz)	Ordering Code	Package	Operation Range
20	20	55	ATV750-20JC ATV750-20PC ATV750-20SC	28J 24P3 24S	Commercial (0°C to 70°C)
			ATV750-20JI ATV750-20PI ATV750-20SI	28J 24P3 24S	Industrial (-40°C to 85°C)
			ATV750-20DM ATV750-20GM ATV750-20LM ATV750-20NM	24DW3 24D3 28LW 28L	Military (-55°C to 125°C)
			ATV750-20DM/883 ATV750-20GM/883 ATV750-20LM/883 ATV750-20NM/883	24DW3 24D3 28LW 28L	Military/883C (-55°C to 125°C)
25	22	45	ATV750-25JC ATV750-25PC ATV750-25SC	28J 24P3 24S	Commercial (0°C to 70°C)
			ATV750-25JI ATV750-25PI ATV750-25SI	28J 24P3 24S	Industrial (-40°C to 85°C)
			ATV750-25DM ATV750-25GM ATV750-25LM ATV750-25NM	24DW3 24D3 28LW 28L	Military (-55°C to 125°C)
			ATV750-25DM/883 ATV750-25GM/883 ATV750-25LM/883 ATV750-25NM/883	24DW3 24D3 28LW 28L	Military/883C (-55°C to 125°C) Class B, Fully Compliant
20	20	55	5962-88726 04 LA 5962-88726 04 3X 5962-94524 03 MLA 5962-94524 03 M3X	24DW3 28LW 24D3 28L	Military/883C (-55°C to 125°C) Class B, Fully Compliant
25	22	45	5962-88726 03 LA 5962-88726 03 3X 5962-94524 02 MLA 5962-94524 02 M3X	24DW3 28LW 24D3 28L	Military/883C (-55°C to 125°C) Class B, Fully Compliant

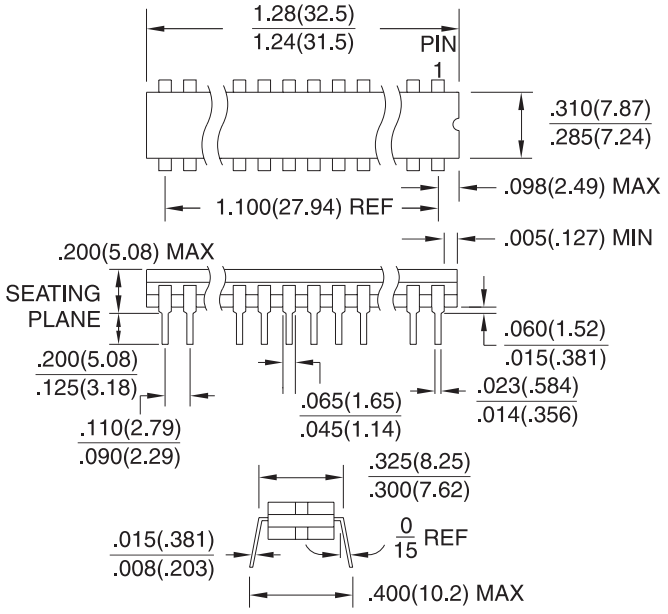
Ordering Information (Continued)

t_{PD} (ns)	t_{CO} (ns)	f_{MAX} (MHz)	Ordering Code	Package	Operation Range
25	22	45	ATV750L-25JC ATV750L-25PC ATV750L-25SC	28J 24P3 24S	Commercial (0°C to 70°C)
			ATV750L-25JI ATV750L-25PI ATV750L-25SI	28J 24P3 24S	Industrial (-40°C to 85°C)
			ATV750L-25DM ATV750L-25GM ATV750L-25LM ATV750L-25NM	24DW3 24D3 28LW 28L	Military (-55°C to 125°C)
			ATV750L-25DM/883 ATV750L-25GM/883 ATV750L-25LM/883 ATV750L-25NM/883	24DW3 24D3 28LW 28L	Military/883C (-55°C to 125°C) Class B, Fully Compliant
25	22	45	5962-88726 07 LX 5962-88726 07 3X 5962-94524 05 MLA 5962-94524 05 M3X	24DW3 28LW 24D3 28L	Military/883C (-55°C to 125°C) Class B, Fully Compliant

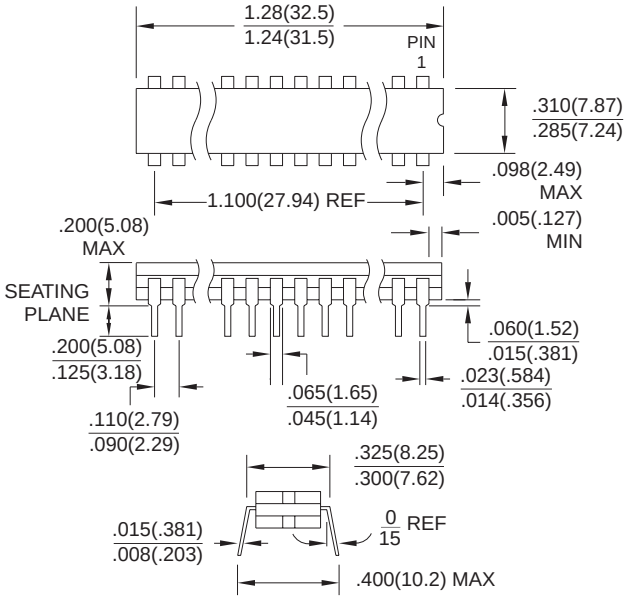
Package Type	
24DW3	24-Lead, 0.300" Wide, Windowed, Ceramic Dual In-line Package (Cerdip)
24D3	24-Lead, 0.300" Wide, Non-Windowed (OTP) Ceramic Dual In-line Package (Cerdip)
28J	28-Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
28LW	28-Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
28L	28-Pad, Non-Windowed, Ceramic Leadless Chip Carrier OTP (LCC)
24P3	24-Lead, 0.300" Wide, Plastic Dual In-line Package OTP (PDIP)
24S	24-Lead, 0.300" Wide, Plastic Gull Wing Small Outline OTP (SOIC)

Packaging Information

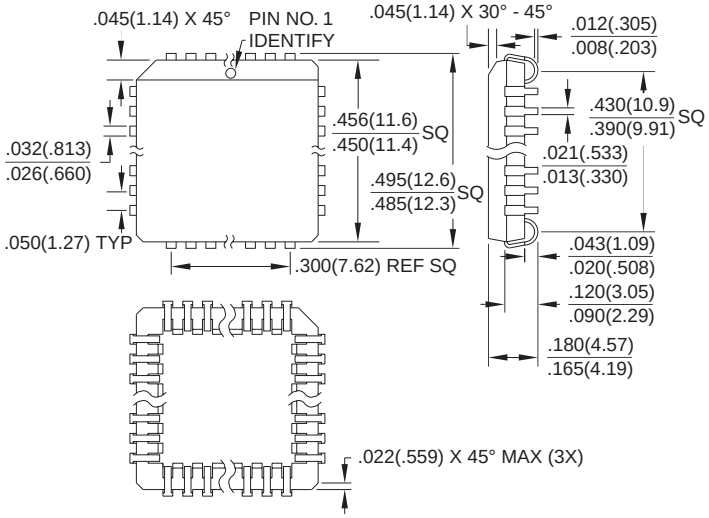
24DW3, 24-Lead, 0.300" Wide, Windowed, Ceramic Dual In-line Package (Cerdip)
Dimensions in Inches and (Millimeters)



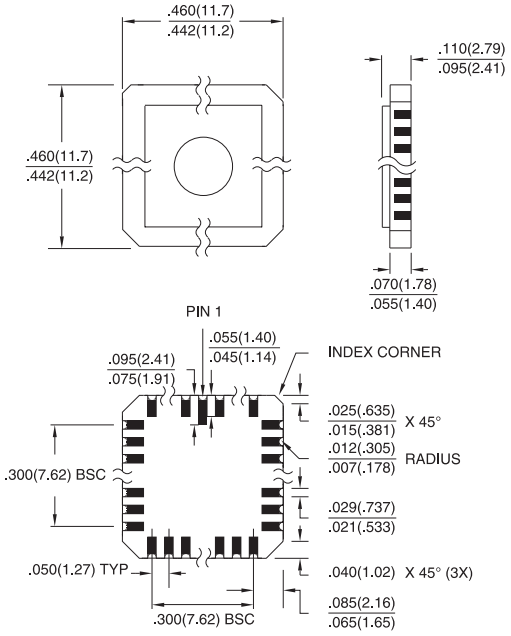
24D3, 24-Lead, 0.300" Wide, Non-Windowed (OTP) Ceramic Dual In-line Package (Cerdip)
Dimensions in Inches and (Millimeters)



28J, 28-Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
Dimensions in Inches and (Millimeters)

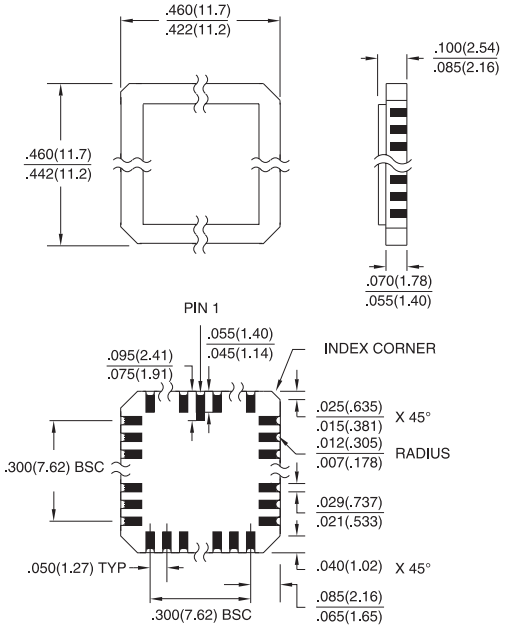


28LW, 28-Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
Dimensions in Inches and (Millimeters)

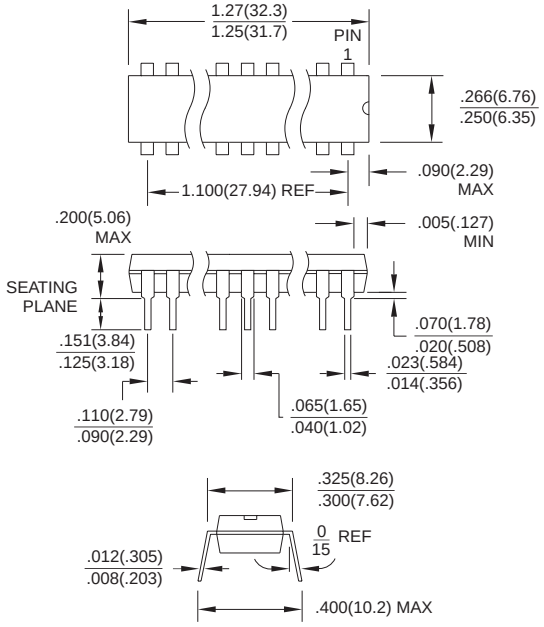


Packaging Information

28L, 28-Pad, Non-Windowed, Ceramic Leadless Chip Carrier OTP (LCC)
Dimensions in Inches and (Millimeters)



24P3, 24-Lead, 0.300" Wide, Plastic Dual Inline Package OTP (PDIP)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-001 AF



24S, 24-Lead, 0.300" Wide, Plastic Gull Wing Small Outline OTP (SOIC)
Dimensions in Inches and (Millimeters)