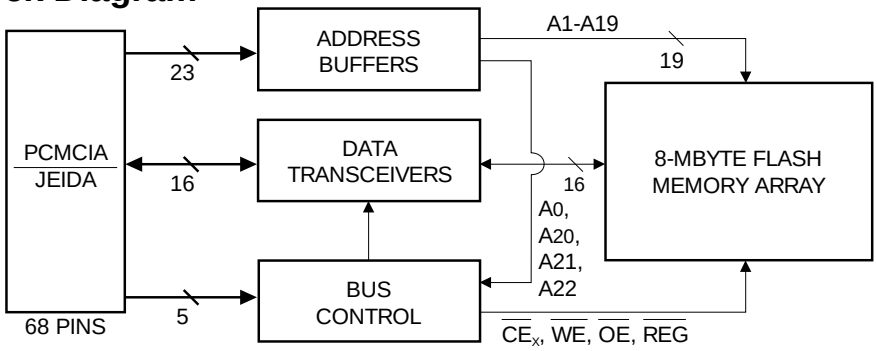
Features

- **Single Power Supply**
  - **Read and Write Voltage, 5 V ± 5%**
- **High Performance**
  - **200 ns Maximum Access Time**
  - **6 ms Typical Sector Write**
- **CMOS Low Power Consumption**
  - **25 mA Typical Active Current (Byte Mode)**
  - **400 µA Typical Standby Current**
- **Fully MS-DOS Compatible Flash Driver and Formatter**
  - **Virtual-Disk Flash Driver with 512 Bytes/Sector**
  - **Random Read/Write to any Sector**
  - **No Erase Operation Required Prior to any Write**
- **Zero Data Retention Power**
  - **Batteries not Required for Data Storage**
- **PCMCIA/JEIDA 68-Pin Standard**
  - **Selectable Byte- or Word-Wide Configuration**
- **High Re-programmable Endurance**
  - **Built-in Redundancy for Sector Replacement**
  - **Minimum 100,000 Write Cycles**
- **Five Levels of Write Protection**
  - **Prevent Accidental Data Loss**

8-Megabyte Flash Memory PCMCIA Card

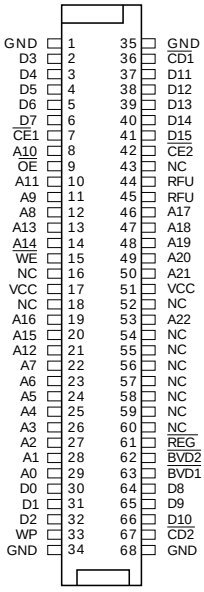
AT5FC008 Preliminary

Block Diagram



Pin Configuration

Pin Name	Function
A0-A22	Addresses
D0-D15	Data
$\overline{CE1}$, $\overline{CE2}$, $\overline{WE}$, $\overline{OE}$, REG	Control Signals
$\overline{CD}$, WP $\overline{BVD1}$, $\overline{BVD2}$	Card Status



Description

Atmel's Flash Memory Card provides the highest system level performance for data and file storage solutions to the portable PC market segment. Data files and applications programs can be stored on the AT5FC008. This allows OEM manufacturers of portable system to eliminate the weight, power consumption and reliability issues associated with electro-mechanical disk-based systems. The AT5FC008 requires a single voltage power supply for total system operation. No batteries are needed for data retention due to its Flash-based technology. Since no high voltage (12 V) is required to perform any write operation, the AT5FC008 is suitable for the emerging "mobile" personal systems.

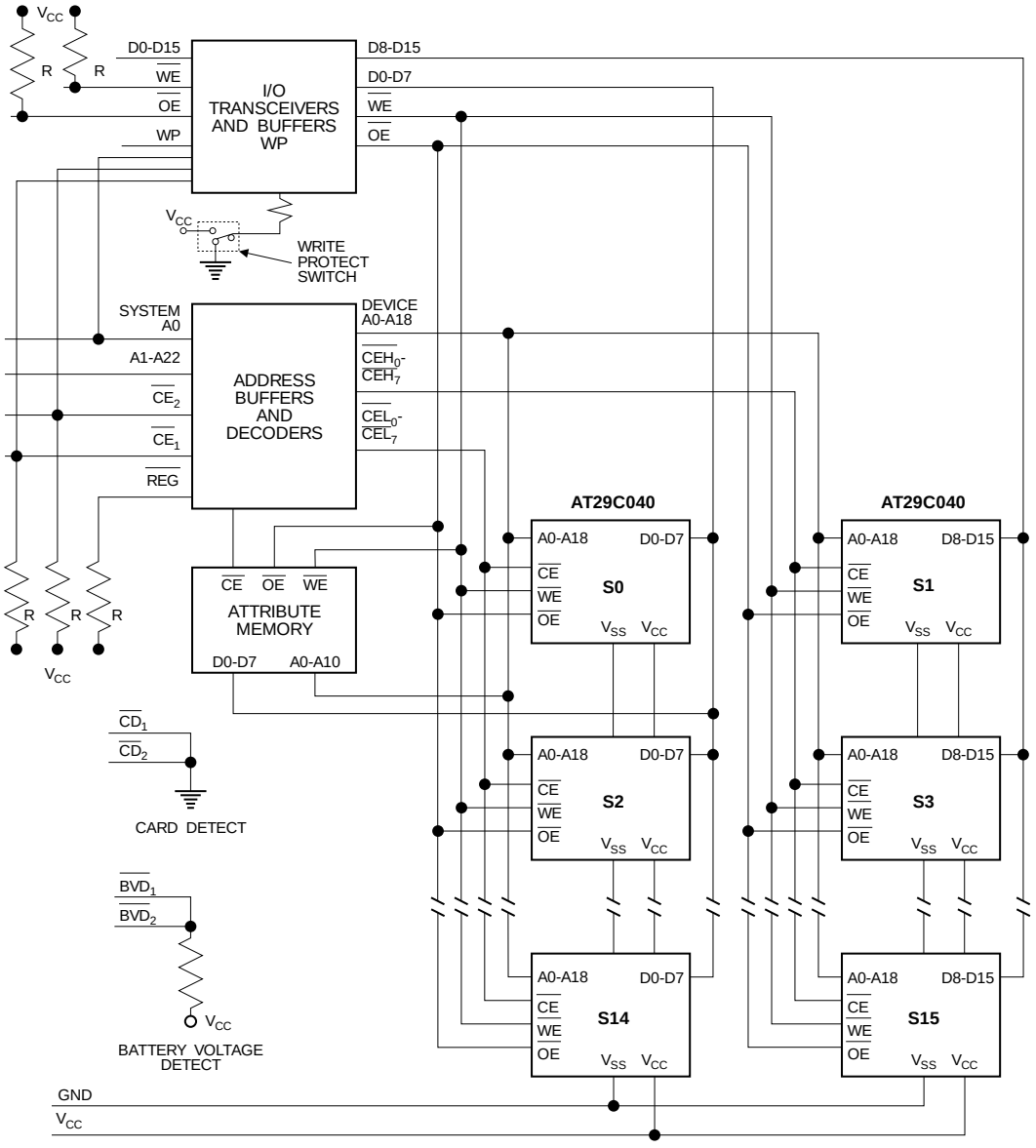
The AT5FC008 is compatible with the 68-pin PCMCIA/JEIDA international standard. Atmel's Flash Memory Cards can be read in either a byte-wide or word-wide mode which allows for flexible integration into various system platforms. It can be read like any typical PCMCIA SRAM or ROM card.

The Card Information Structure (CIS) can be written by the OEM or by Atmel at the attribute memory address space using a format utility. The CIS appears at the beginning of the card's attribute memory space and defines the low-level organization of data on the PC card. The AT5FC008 contains a separate 2K byte EEPROM memory for the card's attribute memory space.

The third party software solutions such as AWARD Software's CardWare™ system and the SCM's Flash File System (FFS), enables Atmel's Flash Memory Card to emulate the function of essentially all the major brand personal computers that are DOS/Windows compatible.

For some unique portable computers, such as the HP200/100/95LX series, the software Driver and Formatter are also available. The Atmel Driver and Formatter utilizes a self-contained spare sector replacement algorithm, enabled by Atmel's small 512-byte sectors, to achieve long term card reliability and endurance.

Block Diagram



Absolute Maximum Ratings*

Storage Temperature	-30°C to +70°C
Ambient Temperature with Power Applied	-10°C to +70°C
Voltage with Respect to Ground, All pins(1)	-2.0 V to +7.0 V
V_{CC}(1)	-2.0 V to +7.0 V
Output Short Circuit Current (2)	-200 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the card. This is a stress rating only and functional operation of the card at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes:
1. Minimum DC voltage on input or I/O pins is -0.5 V. During voltage transients, inputs may overshoot V_{SS} to -2.0 V for periods of up to 20 ns. Maximum DC voltage on output and I/O pins is V_{CC}+0.5 V. During voltage transitions, outputs may overshoot to V_{CC}+2.0 V for periods up to 20 ns.
2. No more than one output shorted at a time. Duration of the short circuit should not be greater than one second. Conditions equal V_{OUT} = 0.5 V or 5.0 V, V_{CC} = Max.

D.C. and A.C. Operating Range

		AT5FC008-20
Operating Temperature (Case)	Com.	0^oC - 70^oC
V_{CC} Power Supply		5 V ± 5%

Pin Capacitance (f = 1 MHz, T = 25°C) (1)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN1}	Address Capacitance	V_{IN} = 0 V		20	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V		20	pF
C_{IN2}	Control Capacitance	V_{IN} = 0 ($\overline{CE}$)		45	pF
$C_{I/O}$	I/O Capacitance	$V_{I/O}$ = 0 V		20	pF

Note: 1. This parameter is characterized and is not 100% tested.

PC Card Pin Assignments

I = Input, O = Output, I/O = Bi-directional, NC = No Connect

Pin	Signal	I/O	Function
1	GND		Ground
2	D3	I/O	Data Bit 3
3	D4	I/O	Data Bit 4
4	D5	I/O	Data Bit 5
5	D6	I/O	Data Bit 6
6	D7	I/O	Data Bit 7
7	$\overline{CE}_1$	I	Card Enable 1 (1)
8	A10	I	Address Bit 10
9	$\overline{OE}$	I	Output Enable
10	A11	I	Address Bit 11
11	A9	I	Address Bit 9
12	A8	I	Address Bit 8
13	A13	I	Address Bit 13
14	A14	I	Address Bit 14
15	$\overline{WE}$	I	Write Enable
16	NC		No Connect
17	V_{CC}		Power Supply
18	NC		No Connect
19	A16	I	Address Bit 16
20	A15	I	Address Bit 15
21	A12	I	Address Bit 12
22	A7	I	Address Bit 7
23	A6	I	Address Bit 6
24	A5	I	Address Bit 5
25	A4	I	Address Bit 4
26	A3	I	Address Bit 3
27	A2	I	Address Bit 2
28	A1	I	Address Bit 1
29	A0	I	Address Bit 0
30	D0	I/O	Data Bit 0
31	D1	I/O	Data Bit 1
32	D2	I/O	Data Bit 2
33	WP	O	Write Protect (1)
34	GND		Ground

Pin	Signal	I/O	Function
35	GND		Ground
36	$\overline{CD}_1$	O	Card Detect 1 (1)
37	D11	I/O	Data Bit 11
38	D12	I/O	Data Bit 12
39	D13	I/O	Data Bit 13
40	D14	I/O	Data Bit 14
41	D15	I/O	Data Bit 15
42	$\overline{CE}_2$	I	Card Enable 2 (1)
43	NC		No Connect
44	RFU		Reserved
45	RFU		Reserved
46	A17	I	Address Bit 17
47	A18	I	Address Bit 18
48	A19	I	Address Bit 19
49	A20	I	Address Bit 20
50	A21	I	Address Bit 21
51	V_{CC}		Power Supply
52	NC		No Connect
53	A22	I	Address Bit 22
54	NC		No Connect
55	NC		No Connect
56	NC		No Connect
57	NC		No Connect
58	NC		No Connect
59	NC		No Connect
60	NC		No Connect
61	$\overline{REG}$	I	Register Select
62	$\overline{BVD}_2$	O	Battery Voltage Detect 2 (2)
63	$\overline{BVD}_1$	O	Battery Voltage Detect 1 (2)
64	D8	I/O	Data Bit 8
65	D9	I/O	Data Bit 9
66	D10	I/O	Data Bit 10
67	$\overline{CD}_2$	O	Card Detect 2 (1)
68	GND		Ground

Notes: 1. Signal must not be connected between cards.
2. $\overline{BVD}$ = Internally pulled up.

Pin Description

Symbol	Name	Type	Function
A0-A22	Address Inputs	Input	Address Inputs are internally latched during write cycles.
D0-D15	Data Input/Output	Input/Output	Data Input/Outputs are internally latched on write cycles. Data outputs are latched during read cycles. Data pins are active high. When the memory card is de-selected or the outputs are disabled the outputs float to tri-state.
$\overline{CE}_1$, $\overline{CE}_2$	Card Enable	Input	Card Enable is active low. The memory card is de-selected and power consumption is reduced to standby levels when $\overline{CE}$ is high. $\overline{CE}$ activates the internal memory card circuitry that controls the high and low byte control logic of the card, input buffers, segment decoders, and associated memory devices.
$\overline{OE}$	Output Enable	Input	Output Enable is active low and enables the data buffers through the card outputs during read cycles.
$\overline{WE}$	Write Enable	Input	Write Enable is active low and controls the write function to the memory array. The target address is latched on the falling edge of the $\overline{WE}$ pulse and the appropriate data is latched on the rising edge of the pulse.
V_{CC}	PC Card Power Supply		PC Card Power Supply for device operation (5.0 V ± 5%)
GND	Ground		Ground
$\overline{CD}_1$, $\overline{CD}_2$	Card Detect	Output	When Card Detect 1 and 2 = Ground the system detects the card.
WP	Write Protect	Output	Write Protect is active high and indicates that all card write operations are disabled by the write protect switch.
NC	No Connect		Corresponding pin is not connected internally.
$\overline{BVD}_1$, $\overline{BVD}_2$	Battery Voltage Detect	Output	Internally pulled up. (There is no battery in the card.)
$\overline{REG}$	Register Select	Input	Provide access to Card Information Structure in the Attribute Memory Device

Memory Card Operations

The AT5FC008 Flash Memory Card is organized as an array of 16 individual AT29C040 devices. They are logically defined as contiguous sectors of 512 bytes. Each sector can be read and written randomly as designated by the host. There is NO need to *erase* any sector prior to any *write* operation. Also, there is NO high voltage (12 V) required to perform any write operations.

The common memory space data contents are altered in a similar manner as writing to individual Flash memory devices. On-card address and data buffers activate the appropriate Flash device in the memory array. Each device internally latches address and data during write cycles. Refer to the **Common Memory Operations** table.

Byte-Wide Operations

The AT5FC008 provides the flexibility to operate on data in byte-wide or word-wide operations. Byte-wide data is available on D0-D7 for read and write operations ($\overline{CE}_1$ = low, $\overline{CE}_2$ = high). Even and odd bytes are stored in a pair of memory chip segments (i.e., S0 and S1) and are accessed when A0 is low and high respectively.

Word-Wide Operations

The 16-bit words are accessed when both $\overline{CE}_1$ and $\overline{CE}_2$ are forced low, A0 = don't care. D0-D15 are used for word-wide operations

Read Enable/Output Disable

Data outputs from the card are disabled when $\overline{OE}$ is at a logic-high level. Under this condition, outputs are in the high-impedance state. The A20, A21 and A22 select the paired memory chip segments, while A0 decides the upper or lower bank. The $\overline{CE}_1$/$\overline{CE}_2$ pins determine either byte or word mode operation. The Output Enable ($\overline{OE}$) is forced low to activate all outputs of the memory chip segments. The on-card I/O transceiver is set in the output mode. The AT5FC008 sends data to the host. Refer to A.C. Read Waveforms drawing.

Standby Operations

When both $\overline{CE}_1$ and $\overline{CE}_2$ are at logic-high level, the AT5FC008 is in Standby mode; i.e., all memory chip segments as well as the decoder/transceiver are completely de-selected at minimum power consumption. Even in the byte-mode read operation, only one memory chip segment (even or odd) is active at any time. The other seven memory chip segments remain in standby. In the word-mode there are two memory chip segments in active and six in standby.

Write Operations

The AT5FC008 is written on a sector basis. Each sector of 512 bytes can be selected randomly and written independently without any prior erase cycle. A9 to A19 specify the sector address, while A20, A21 and A22 specify the Flash chip segment pair. Within each sector, the individual byte address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Each byte pair to be programmed must have its high-to-low transition on $\overline{WE}$ (or $\overline{CE}$) within 150 µs of the low-to- high transition of $\overline{WE}$ (or $\overline{CE}$) of the preceding byte pair. If a high-to-low transition is not detected within 150 µs of the last low-to-high transition, the data load period will end and the internal programming period will start. All the bytes of a sector are simultaneously programmed during the internal programming period. A maximum write time of 10 ms per sector is self-controlled by the Flash devices. Refer to A.C. Write Waveforms drawings.

Write Protection

The AT5FC008 has five types of write protection. The PCMCIA/JEIDA socket itself provides the first type of write protection. Power supply and control pins have specific pin lengths in order to protect the card with proper power supply sequencing in the case of hot insertion and removal.

A mechanical write protection switch provides a second type of write protection. When this switch is activated, $\overline{WE}$ is internally forced high. The Flash memory arrays are therefore write-disabled.

The third type of write protection is achieved with the built-in low VCC sensing circuit within each Flash device. If the external VCC is below 3.8 V (typical), the write function is inhibited.

The fourth type of write protection is a noise filter circuit within each Flash device. Any pulse of less than 15 ns (typical) on the $\overline{WE}$, $\overline{CE}_1$ or $\overline{CE}_2$ inputs will not initiate a program cycle.

The last type of write protection is based on the Software Data Protection (SDP) scheme of the AT29C040 devices. Each of the sixteen devices needs to enable and disable the SDP individually. Refer to the **Software Data Protected Programming/Disable Algorithm** tables for descriptions of enable and disable SDP operations.

Card Detection

Each $\overline{CD}$ (output) pin should be read by the host system to determine if the memory card is properly seated in the socket. $\overline{CD}_1$ and $\overline{CD}_2$ are internally tied to the ground. If both bits are not detected, the system should indicate that the card must be re-inserted.

CIS Data

The Card Information Structure (CIS) describes the capabilities and specifications of a card. The CIS of the AT5FC008 can be written either by the OEM or by Atmel at the attribute memory space beginning at address 00000H by using a format utility. The AT5FC008 contains a separate 2K byte EEPROM memory for the card's attribute memory space. The attribute is active when the $\overline{REG}$ pin is driven low. D0-D7 are active during attribute memory access. D8-D15 should be ignored. Odd order bytes present invalid data. Refer to the **Attribute Memory Operations** table.

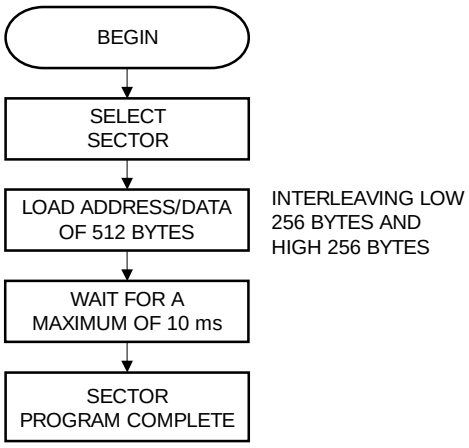
Common Memory Operations

X = Don't Care, where Don't Care is either V_{IL} or V_{IH} levels.

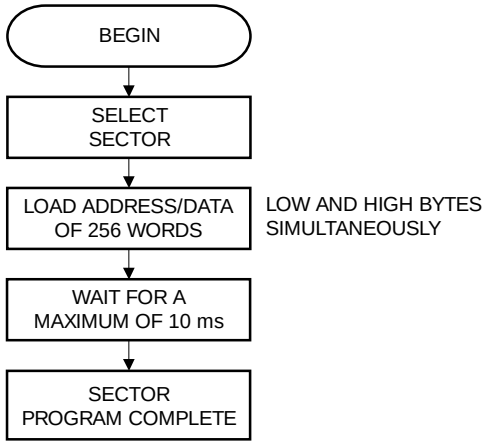
Pins	$\overline{REG}$	$\overline{CE_2}$	$\overline{CE_1}$	$\overline{OE}$	$\overline{WE}$	A0	D8-D15	D0-D7
Read-Only								
Read (x8) (1)	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	High Z	Data Out-Even
Read (x8) (2)	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	High Z	Data Out-Odd
Read (x8) (3)	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	X	Data Out-Odd	High Z
Read (x16) (4)	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	X	Data Out-Odd	Data Out-Even
Output Disable	V_{IH}	X	X	V_{IH}	V_{IH}	X	High Z	High Z
Standby	X	V_{IH}	V_{IH}	X	X	X	High Z	High Z
Write-Only								
Write (x8) (1)	V_{IH}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	High Z	Data In-Even
Write (x8) (2)	V_{IH}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	High Z	Data In-Odd
Write (x8) (3)	V_{IH}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	X	Data In-Odd	High Z
Write (x16) (4)	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	X	Data In-Odd	Data In-Even
Output Disable	V_{IH}	X	X	V_{IH}	V_{IL}	X	High Z	High Z

Notes:
1. Byte access - Even. In this x8 mode, D0-D7 contain the "even" byte (low byte) of the x16 word. D8-D15 are inactive.
2. Byte access - Odd. In this x8 mode, D0-D7 contain the "odd" byte (high byte) of the x16 word. This is accomplished internal to the card by transposing D8-D15 to D0-D7. D8-D15 are inactive.
3. Odd byte only access. In this x8 mode, D8-D15 contain the "odd" byte (high byte) of the x16 word. D0-D7 are inactive. A0 = X.
4. Word access. In this mode D0-D7 contain the "even" byte while D8-D15 contain the "odd" byte. A0 = X

Memory Card Program Routine
Byte Mode



Memory Card Program Routine
Word Mode



Attribute Memory Operations

X = Don't Care, where Don't Care is either V_{IL} or V_{IH} levels.

Pins	$\overline{REG}$	$\overline{CE_2}$	$\overline{CE_1}$	$\overline{OE}$	$\overline{WE}$	A0	D8-D15	D0-D7
Read-Only								
Read (x8) (1)	V_{IL}	VIH	V_{IL}	V_{IL}	V_{IH}	V_{IL}	High Z	Data Out-Even
Read (x8)	V_{IL}	VIH	V_{IL}	V_{IL}	V_{IH}	V_{IH}	High Z	Not Valid
Read (x8)	V_{IL}	VIL	V_{IH}	V_{IL}	V_{IH}	X	Not Valid	High Z
Read (x16)	V_{IL}	VIL	V_{IL}	V_{IL}	V_{IH}	X	Not Valid	Data Out-Even
Output Disable	V_{IL}	X	X	VIH	V_{IH}	X	High Z	High Z
Standby	X	V_{IH}	V_{IH}	X	X	X	High Z	High Z
Write-Only								
Write (x8) (1)	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	High Z	Data In-Even
Write (x8)	V_{IL}	VIH	V_{IL}	V_{IH}	V_{IL}	V_{IH}	High Z	Not Valid
Write (x8)	V_{IL}	VIL	V_{IH}	V_{IH}	V_{IL}	X	Not Valid	High Z
Write (x16)	V_{IL}	VIL	V_{IL}	V_{IH}	V_{IL}	X	Not Valid	Data In-Even
Output Disable	V_{IL}	X	X	V_{IH}	V_{IL}	X	High Z	High Z

Note: 1. Byte access - Even. In this x8 mode, D0-D7 contain the "even" byte (low byte) of the x16 word. D8-D15 are inactive.

D.C. Characteristics, Byte-Wide Operation

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{LI}	Input LeakageCurrent	V_{CC} = V_{CC} Max, V_{IN} = V_{CC} or V_{SS}		1.0	±20	µA
I_{LO}	Output Leakage Current	V_{CC} = V_{CC} Max, V_{OUT} = V_{CC} or V_{SS}		1.0	20	µA
I_{SB}	V_{CC} Standby Current	V_{CC} = V_{CC} Max, $\overline{CE}$ = V_{CC} ± 0.2 V		0.6	1.2	mA
I_{CC1} (1)	V_{CC} Active Read Current	V_{CC} = V_{CC} Max, $\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}, I_{OUT} = 0 mA, at 5 MHz		25	40	mA
I_{CC2}	V_{CC} Active Write Current	$\overline{CE}$ = V_{IL},$\overline{WE}$ = V_{IL}, Programming in Progress		25	40	mA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage		2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 3.2 mA			0.40	V
V_{OH}	Output High Voltage	I_{OH} = -2.0 mA	3.8			V

Notes: 1. One Flash device active, 15 in standby.

D.C. Characteristics, Word-Wide Operation

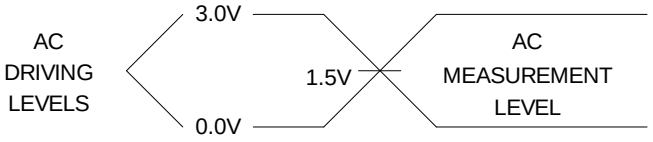
Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{LI}	Input LeakageCurrent	V_{CC} = V_{CC} Max, V_{IN} = V_{CC} or V_{SS}		1.0	±20	µA
I_{LO}	Output Leakage Current	V_{CC} = V_{CC} Max, V_{OUT} = V_{CC} or V_{SS}		1.0	20	µA
I_{SB}	V_{CC} Standby Current	V_{CC} = V_{CC} Max, $\overline{CE}$ = V_{CC} ± 0.2 V		0.6	1.2	mA
I_{CC1} (1)	V_{CC} Active Read Current	V_{CC} = V_{CC} Max, $\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}, I_{OUT} = 0 mA, at 5 MHz		50	80	mA
I_{CC2}	V_{CC} Active Write Current	$\overline{CE}$ = V_{IL}, $\overline{WE}$ = V_{IL}, Programming in Progress		50	80	mA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage		2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 3.2 mA			0.40	V
V_{OH}	Output High Voltage	I_{OH} = -2.0 mA	3.8			V

Notes: 1. Two Flash devices active, 14 in standby.

A.C. Read Characteristics

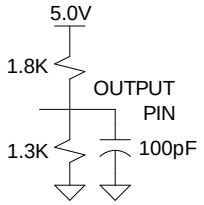
Symbol	Parameter	Min	Max	Units
t_{RC}	Read Cycle Time	200		ns
t_{CE}	Chip Enable Access Time		200	ns
t_{ACC}	Address Access Time		200	ns
t_{OE}	Output Enable Access Time		100	ns
t_{Lz}	Chip Enable to Output in Low Z	5		ns
t_{DF}	Chip Disable to Output in High Z		60	ns
t_{OLZ}	Output Enable to Output in Low Z	5		ns
t_{DF}	Output Disable to Output in High Z		60	ns
t_{OH}	Output Hold Time from First of Address, $\overline{CE}$, or $\overline{OE}$ Change	5		ns
t_{WC}	Write Recovery Time Before Read		10	ms

Input test Waveforms and Measurement Level

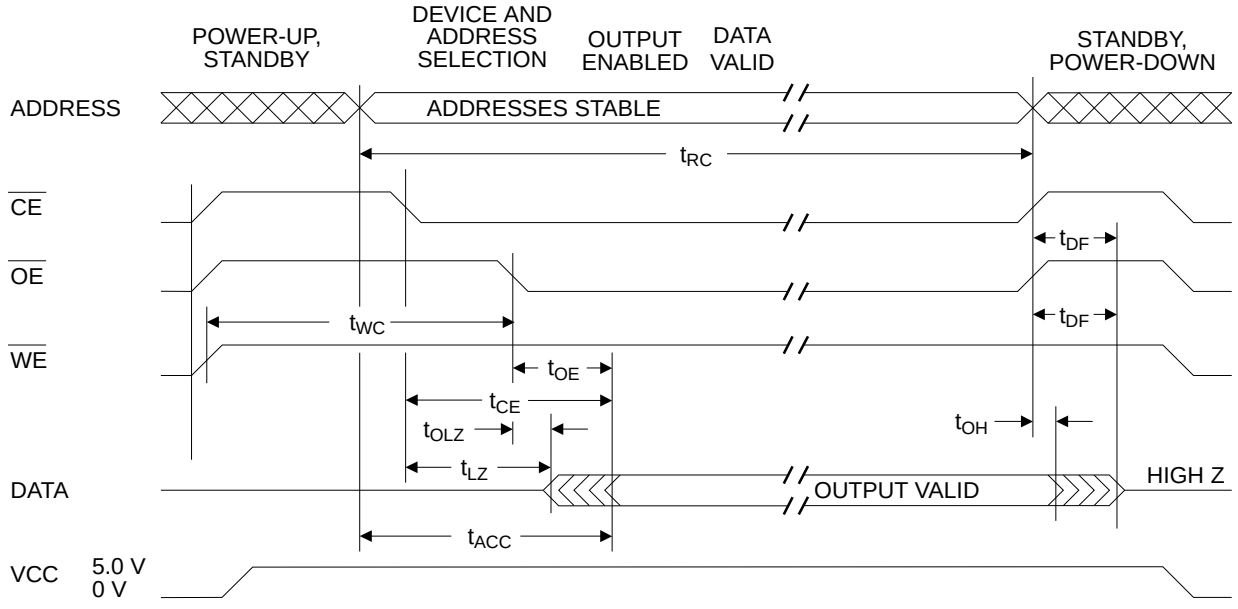


t_R, t_F < 5 ns

Output Test Load



A.C. Read Waveforms (1)

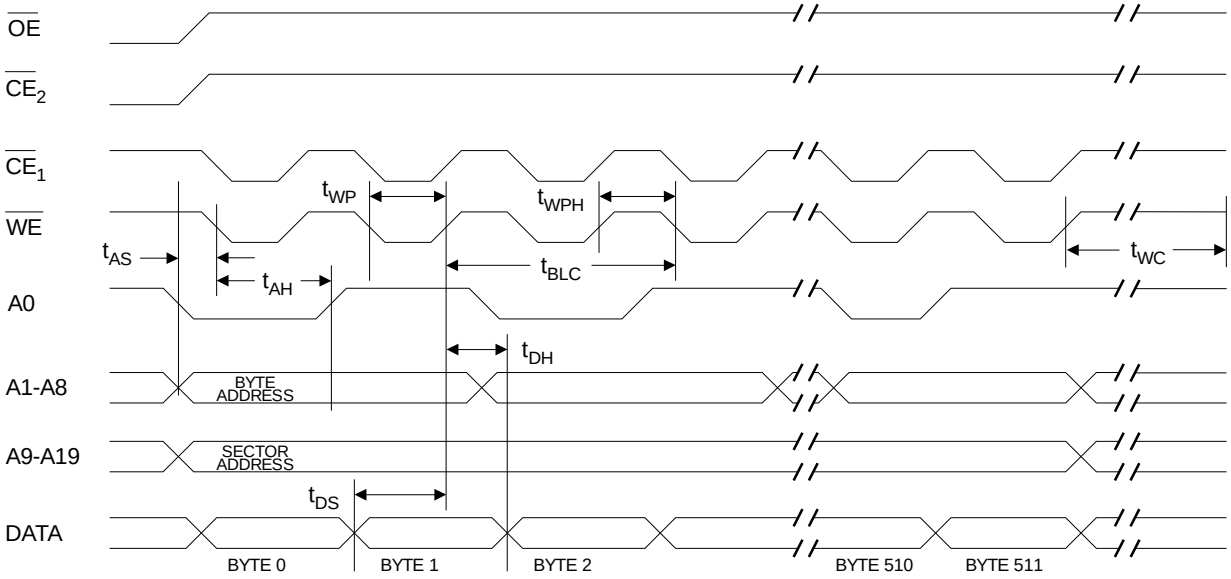


Note:
1. $\overline{CE}$ refers to $\overline{CE_1}$, and/or $\overline{CE_2}$

Write Cycle Characteristics

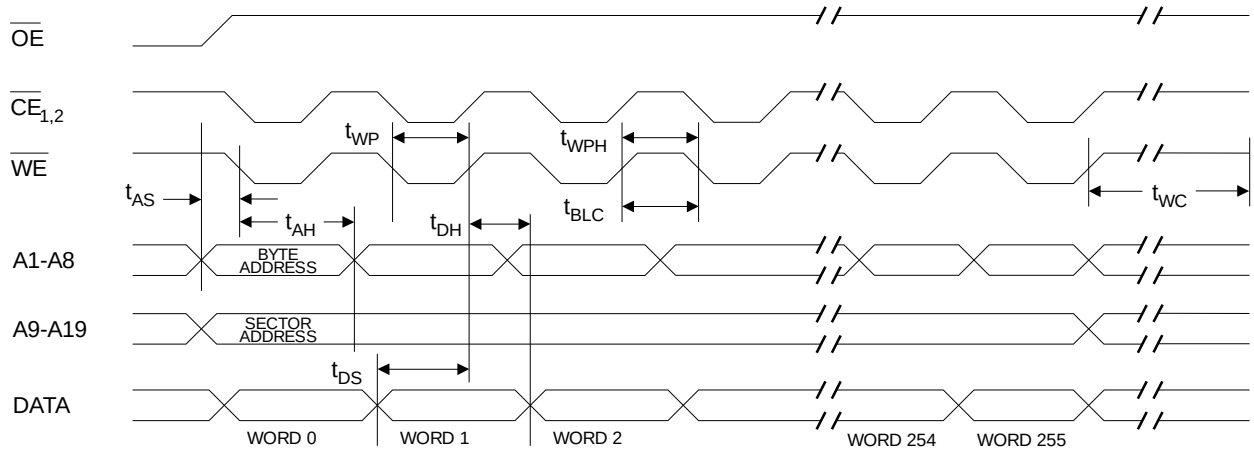
Symbol	Parameter	Min	Max	Units
t_{WC}	Write Cycle Time		10	ms
t_{AS}	Address Set-up Time	10		ns
t_{AH}	Address Hold Time	60		ns
t_{DS}	Data Set-up Time	60		ns
t_{DH}	Data Hold Time	10		ns
t_{WP}	Write Pulse Width	100		ns
t_{BLC}	Byte Load Cycle Time		150	µs
t_{WPH}	Write Pulse Width High	100		ns

A.C. Write Waveforms (Byte Mode)



Notes:
1. A20, A21 and A22 specify the pair of AT29C040 devices to be written, while A0 controls the selection of even and odd bytes. A0, A20, A21 and A22 must be valid throughout the entire $\overline{WE}$ low pulse.
2. A9 through A19 must specify the sector address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
3. $\overline{OE}$ must be high when $\overline{WE}$ and $\overline{CE}$ are both low.
4. **All bytes that are not loaded within the sector being programmed will be erased to FF.**

A.C. Write Waveforms (Word Mode)



1. A20, A21 and A22 specify the pair of AT29C040 devices to be written; they must be valid throughout the entire $\overline{WE}$ low pulse. A0 is don't care.
2. A9 through A19 must specify the sector address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
3. $\overline{OE}$ must be high when $\overline{WE}$ and $\overline{CE}$ are both low.
4. **All bytes that are not loaded within the sector being programmed will be erased to FF.**

Software Data Protected Programming Algorithm [1]

Device	0	1	2	3	4	5	6	7
Data Address	AA 00AAAA	AA 00AAAB	AA 10AAAA	AA 10AAAB	AA 20AAAA	AA 20AAAB	AA 30AAAA	AA 30AAAB
Data Address	55 005554	55 005555	55 105554	55 105555	55 205554	55 205555	55 305554	55 305555
Data Address	A0 00AAAA	A0 00AAAB	A0 10AAAA	A0 10AAAB	A0 20AAAA	A0 20AAAB	A0 30AAAA	A0 30AAAB
Writes Enabled	Write Bytes	Write Bytes	Write Bytes	Write Bytes	Write Bytes	Write Bytes	Write Bytes	Write Bytes

Device	8	9	10	11	12	13	14	15
Data Address	AA 40AAAA	AA 40AAAB	AA 50AAAA	AA 50AAAB	AA 60AAAA	AA 60AAAB	AA 70AAAA	AA 70AAAB
Data Address	55 405554	55 405555	55 505554	55 505555	55 605554	55 605555	55 705554	55 705555
Data Address	A0 40AAAA	A0 40AAAB	A0 50AAAA	A0 50AAAB	A0 60AAAA	A0 60AAAB	A0 70AAAA	A0 70AAAB
Writes Enabled	Write Bytes	Write Bytes	Write Bytes	Write Bytes	Write Bytes	Write Bytes	Write Bytes	Write Bytes

Note: 1. Load 3 bytes to corresponding Flash chip segment individually to enable software data protection.

Software Data Protected Disable Algorithm [1]

Device	0	1	2	3	4	5	6	7
Data Address	AA 00AAAA	AA 00AAAB	AA 10AAAA	AA 10AAAB	AA 20AAAA	AA 20AAAB	AA 30AAAA	AA 30AAAB
Data Address	55 005554	55 005555	55 105554	55 105555	55 205554	55 205555	55 305554	55 305555
Data Address	80 00AAAA	80 00AAAB	80 10AAAA	80 10AAAB	80 20AAAA	80 20AAAB	80 30AAAA	80 30AAAB
Data Address	AA 00AAAA	AA 00AAAB	AA 10AAAA	AA 10AAAB	AA 20AAAA	AA 20AAAB	AA 30AAAA	AA 30AAAB
Data Address	55 005554	55 005555	55 105554	55 105555	55 205554	55 205555	55 305554	55 305555
Data Address	20 00AAAA	20 00AAAB	20 10AAAA	20 10AAAB	20 20AAAA	20 20AAAB	20 30AAAA	20 30AAAB
Writes Enabled	Write Bytes	Write Bytes	Write Bytes	Write Bytes	Write Bytes	Write Bytes	Write Bytes	Write Bytes

Device	8	9	10	11	12	13	14	15
Data Address	AA 40AAAA	AA 40AAAB	AA 50AAAA	AA 50AAAB	AA 60AAAA	AA 60AAAB	AA 70AAAA	AA 70AAAB
Data Address	55 405554	55 405555	55 505554	55 505555	55 605554	55 605555	55 705554	55 705555
Data Address	80 40AAAA	80 40AAAB	80 50AAAA	80 50AAAB	80 60AAAA	80 60AAAB	80 70AAAA	80 70AAAB
Data Address	AA 40AAAA	AA 40AAAB	AA 50AAAA	AA 50AAAB	AA 60AAAA	AA 60AAAB	AA 70AAAA	AA 70AAAB
Data Address	55 405554	55 405555	55 505554	55 505555	55 605554	55 605555	55 705554	55 705555
Data Address	20 40AAAA	20 40AAAB	20 50AAAA	20 50AAAB	20 60AAAA	20 60AAAB	20 70AAAA	20 70AAAB
Writes Enabled	Write Bytes	Write Bytes	Write Bytes	Write Bytes	Write Bytes	Write Bytes	Write Bytes	Write Bytes

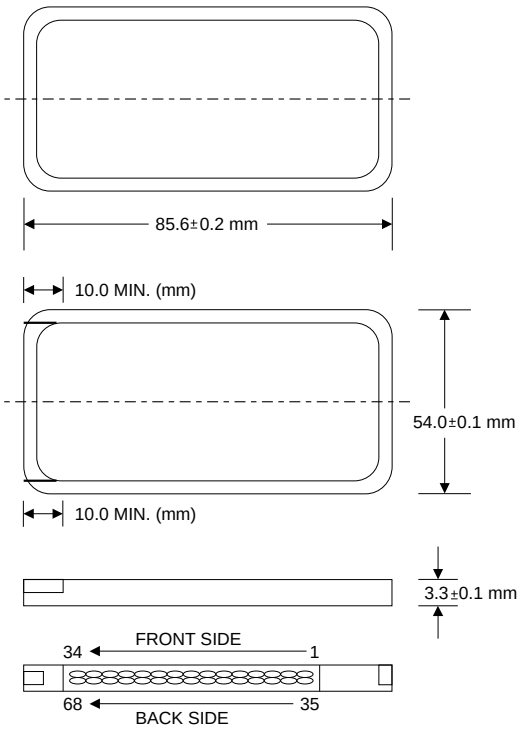
Note: 1. Load 6 bytes to corresponding Flash chip segment individually to disable software data protection.

Ordering Information

t_{ACC} (ns)	Ordering Code	Package	Operation Range
200	AT5FC008-20	PCMCIA Type 1	Commercial (0°C to 70°C)

Packaging Information

PCMCIA, Type 1 PC Memory Card
Dimensions in millimeters



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