Features

- **3.0V to 5.5V Operation**
- **Industry Standard Architecture**
  - **Emulates Many 20-Pin PALs®**
  - **Low Cost Easy-to-Use Software Tools**
- **High Speed**
  - **10 ns Maximum Pin-to-Pin Delay**
- **Ultra-Low Power**
  - **5 µA (Max.) Pin-Controlled Power Down Mode Option**
  - **Typical 100 nA Standby**
- **CMOS and TTL Compatible Inputs and Outputs**
  - **I/O Pin Keeper Circuits**
- **Advanced Flash Technology**
  - **Reprogrammable**
  - **100% Tested**
- **High Reliability CMOS Process**
  - **20 Year Data Retention**
  - **100 Erase/Write Cycles**
  - **2,000V ESD Protection**
  - **200 mA Latchup Immunity**
- **Commercial and Industrial Temperature Ranges**
- **Dual-in-Line and Surface Mount Packages in Standard Pinouts**

Description

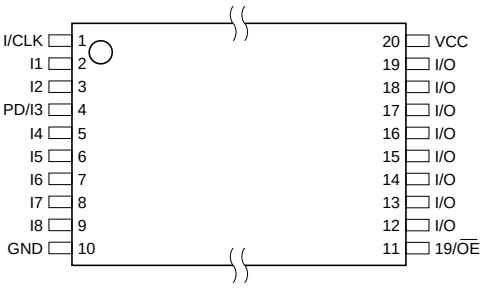
The ATF16LV8C is a high-performance EECMOS Programmable Logic Device that utilizes Atmel's proven electrically erasable Flash memory technology. Speeds down to 10 ns and a 5 µA pin-controlled power down mode option are offered. All speed ranges are specified over the full 3.0V to 5.25V range for industrial and commercial temperature ranges.

(continued)

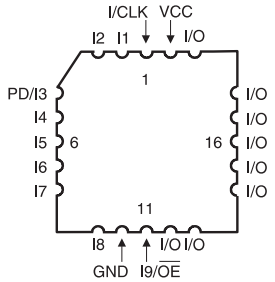
Pin Configurations

Pin Name	Function
CLK	Clock
I	Logic Inputs
I/O	Bidirectional Buffers
OE	Output Enable
VCC	(+3V to 5.5V) Supply
PD	Programmable Power Down Option

TSSOP

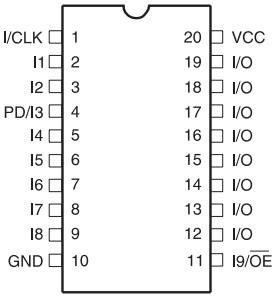


PLCC



Top View

DIP/SOIC



High-Performance EE PLD

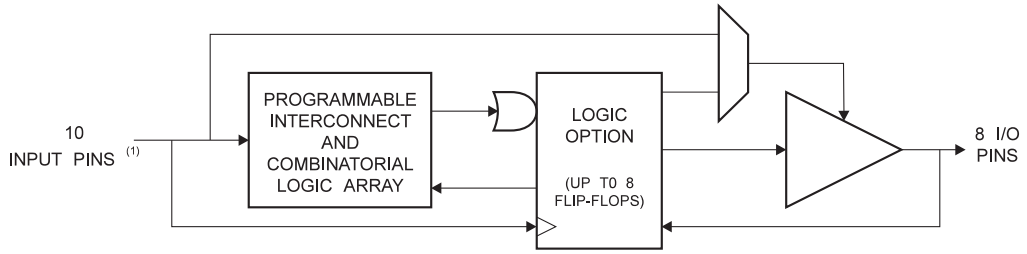
ATF16LV8C

Rev. 0403E–06/98

The ATF16LV8C incorporates a superset of the generic architectures, which allows direct replacement of the 16R8 family and most 20-pin combinatorial PLDs. Eight outputs are each allocated eight product terms. Three different modes of operation, configured automatically with software, allow highly complex logic functions to be realized.

The ATF16LV8C can significantly reduce total system power, thereby enhancing system reliability and reducing power supply costs. When pin 4 is configured as the power down control pin, supply current drops to less than 5 µA whenever the pin is high. If the power down feature isn't required for a particular application, pin 4 may be used as a logic input. Also, the pin keeper circuits eliminate the need for internal pull-up resistors along with their attendant power consumption.

Block Diagram



Note: 1. Includes optional PD control pin.

Absolute Maximum Ratings*

Temperature Under Bias	-40°C to +85°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V(1)
Voltage on Input Pins with Respect to Ground During Programming	-2.0V to +14.0V(1)
Programming Voltage with Respect to Ground	-2.0V to +14.0V(1)

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.6V dc, which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is Vcc + 0.75V dc, which may overshoot to 7.0V for pulses of less than 20 ns.

DC and AC Operating Conditions

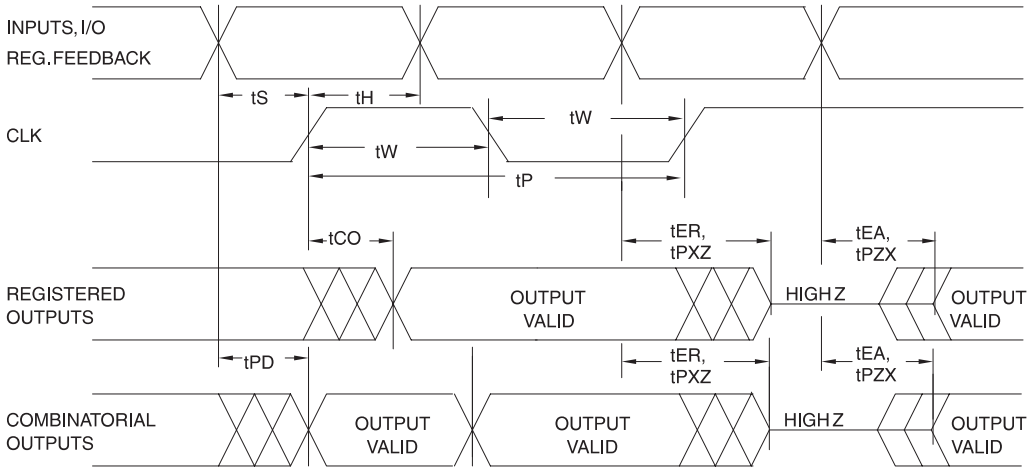
	Commercial
Operating Temperature (Case)	0°C - 70°C
V_{CC} Power Supply	3.0V to 5.5V

DC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{IL}	Input or I/O Low Leakage Current	$0 \le V_{IN} \le V_{IL}$(MAX)			-10	µA
I_{IH}	Input or I/O High Leakage Current	$1.8 \le V_{IN} \le V_{CC}$			10	µA
I_{CC1}[1]	Power Supply Current	15 MHz, V_{CC} = MAX, V_{IN} = 0, $V_{CC,}$ Outputs Open			55	mA
I_{PD}[1]	Power Supply Current, Power Down Mode	V_{CC} = MAX, V_{IN} = 0, V_{CC}		0.1	5	µA
I_{OS}	Output Short Circuit Current	V_{OUT} = 0.5V; V_{CC}= 3V; T_A = 25°C			-150	mA
V_{IL}	Input Low Voltage	MIN < V_{CC} < MAX	-0.5		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 1	V
V_{OL}	Output Low Voltage	V_{CC} = MIN; All Outputs I_{OL} = 8 mA			0.5	V
V_{OH}	Output High Voltage	V_{CC} = MIN I_{OL} = -500 mA	2.4			V
I_{OL}	Output Low Current	V_{CC} = MIN	8			mA
I_{OH}	Output High Current	V_{CC} = MIN	-4			mA

Note: 1. All I_{CC} parameters measured with outputs open.

AC Waveforms[1]



Note: 1. Timing measurement reference is 1.5V. Input AC driving levels are 0.0V and 3.0V, unless otherwise specified.

AC Characteristics

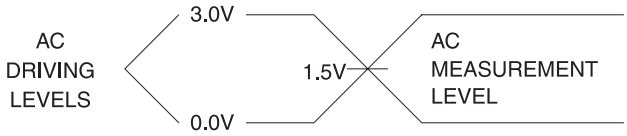
Symbol	Parameter	-10		-15		Units
		Min	Max	Min	Max	
t_{PD}	Input or Feedback to Non-Registered Output	1	10	1	15	ns
t_{CF}	Clock to Feedback		5		8	ns
t_{CO}	Clock to Output	2	7	2	10	ns
t_S	Input or Feedback Setup Time	7		12		ns
t_H	Input Hold Time	0		0		ns
t_P	Clock Period	12		16		ns
t_W	Clock Width	6		8		ns
F_{MAX}	External Feedback $1/(t_S + t_{CO})$		71.4		45.5	MHz
	Internal Feedback $1/(t_S + t_{CF})$		83.3		50	MHz
	No Feedback $1/(t_P)$		83.3		62.5	MHz
t_{EA}	Input to Output Enable — Product Term	3	10	3	15	ns
t_{ER}	Input to Output Disable — Product Term	2	10	2	15	ns
t_{PZX}	$\overline{OE}$ pin to Output Enable	2	8	2	15	ns
t_{PXZ}	$\overline{OE}$ pin to Output Disable	1.5	8	1.5	15	ns

Power Down AC Characteristics (1)(2)(3)

Symbol	Parameter	-10		-15		Units
		Min	Max	Min	Max	
t_{IVDH}	Valid Input Before PD High	10		15		ns
t_{GVDH}	Valid $\overline{OE}$ Before PD High	0		0		ns
t_{CVDH}	Valid Clock Before PD High	0		0		ns
t_{DHIX}	Input Don't Care After PD High		10		15	ns
t_{DHGX}	$\overline{OE}$ Don't Care After PD High		10		15	ns
t_{DHCX}	Clock Don't Care After PD High		10		15	ns
t_{DLIV}	PD Low to Valid Input		10		15	ns
t_{DLGV}	PD Low to Valid $\overline{OE}$		25		30	ns
t_{DLCV}	PD Low to Valid Clock		25		30	ns
t_{DLOV}	PD Low to Valid Output		30		35	ns

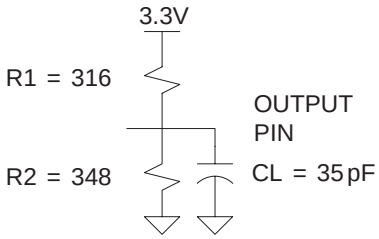
Notes: 1. Output data is latched and held.
2. HI-Z outputs remain HI-Z.
3. Clock and input transitions are ignored.

Input Test Waveforms and Measurement Levels:



t_R, t_F < 1.5ns (10% to 90%)

Output Test Loads: Commercial



Note: Similar devices are tested with slightly different loads. These load differences may affect output signals' delay and slew rate. Atmel devices are tested with sufficient margins to meet compatible devices.

Pin Capacitance

(f = 1 MHz, T = 25°C)[1]

	Typ	Max	Units	Conditions
C_{IN}	5	8	pF	V_{IN} = 0V
C_{OUT}	6	8	pF	V_{OUT} = 0V

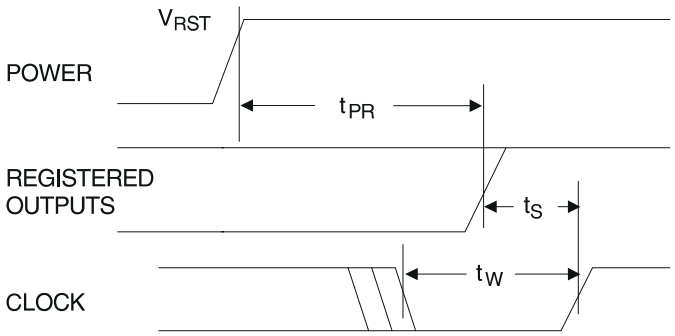
Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Power Up Reset

The ATF16LV8C's registers are designed to reset during power up. At a point delayed slightly from V_{CC} crossing V_{RST}, all registers will be reset to the low state. As a result, the registered output state will always be high on power-up.

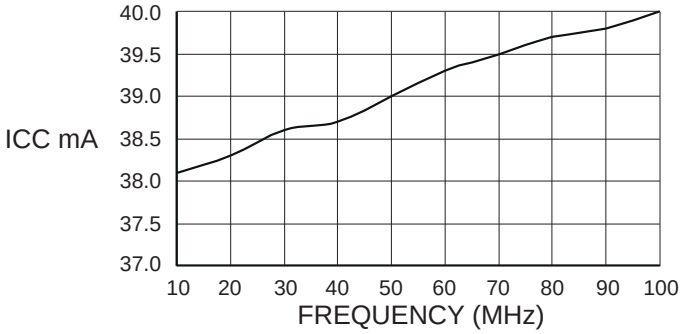
This feature is critical for state machine initialization. However, due to the asynchronous nature of reset and the uncertainty of how V_{CC} actually rises in the system, the following conditions are required:

1. The V_{CC} rise must be monotonic from below 0.7 volts.
2. The signals from which the clock is derived must remain stable during T_{PR}.
3. After T_{PR}, all input and feedback setup times must be met before driving the clock term high.

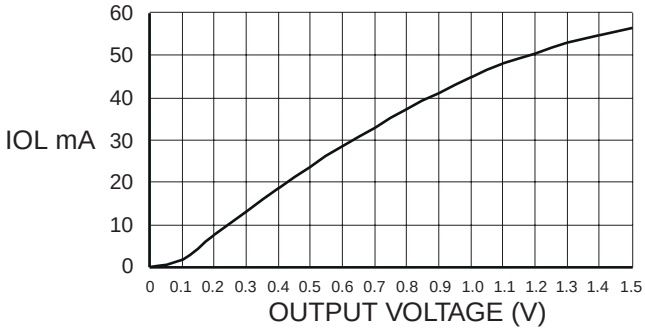


Parameter	Description	Typ	Max	Units
T_{PR}	Power-Up Reset Time	600	1,000	ns
V_{RST}	Power-Up Reset Voltage	2.5	3.0	V

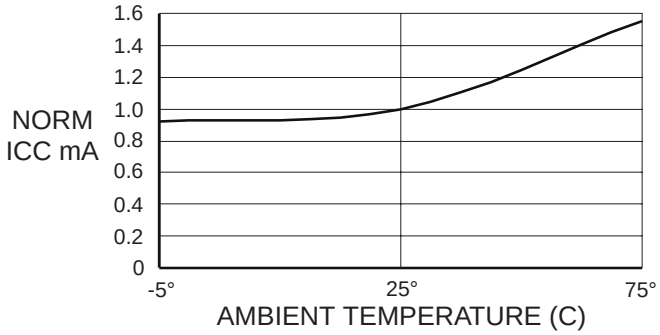
SUPPLY CURRENT
VS. INPUT FREQUENCY
(VCC = 3.3V, TA = 25°C)



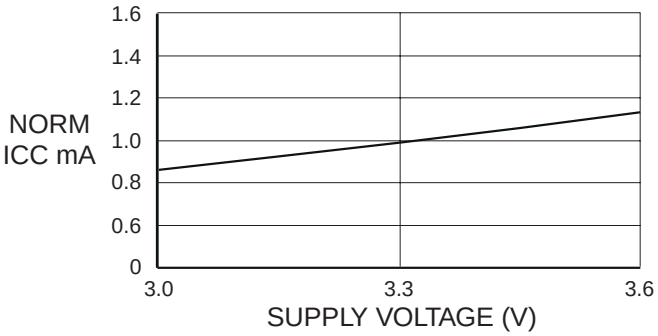
OUTPUT SINK CURRENT
VS. OUTPUT VOLTAGE (VCC = 5V, TA = 25°C)



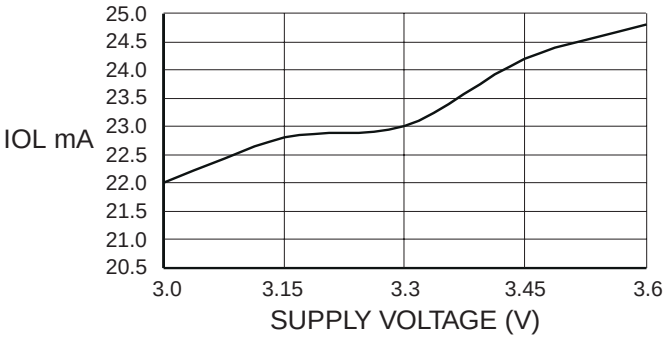
NORMALIZED SUPPLY CURRENT
VS. AMBIENT TEMPERATURE
(VCC = 3.3V, STANDBY)



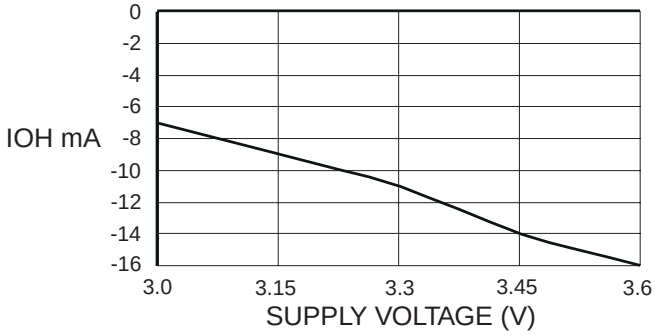
NORMALIZED SUPPLY CURRENT
VS. SUPPLY VOLTAGE
(TA = 25°C, STANDBY)



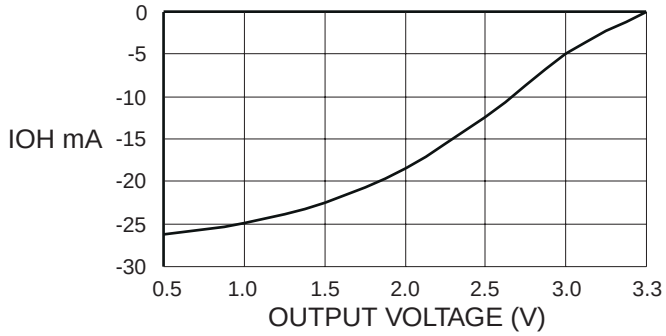
OUTPUT SINK CURRENT
VS. SUPPLY VOLTAGE (TA = 25°C, VOL = 0.45V)



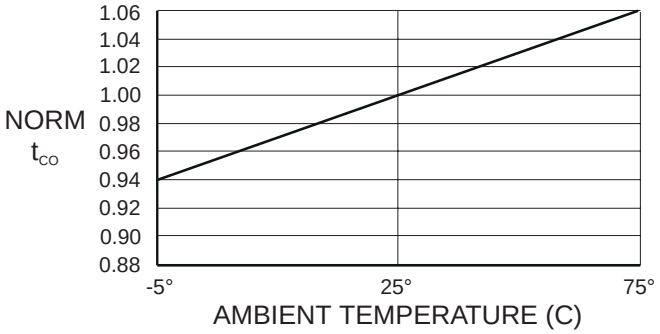
OUTPUT SOURCE CURRENT
VS. SUPPLY VOLTAGE (VOH = 2.4V, TA = 25°C)



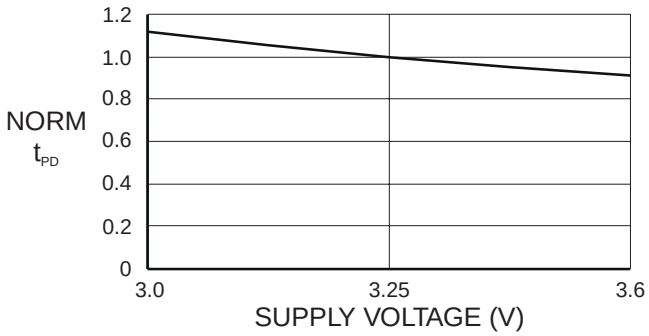
OUTPUT SOURCE CURRENT
VS. OUTPUT VOLTAGE (VCC = 5V, TA = 25°C)



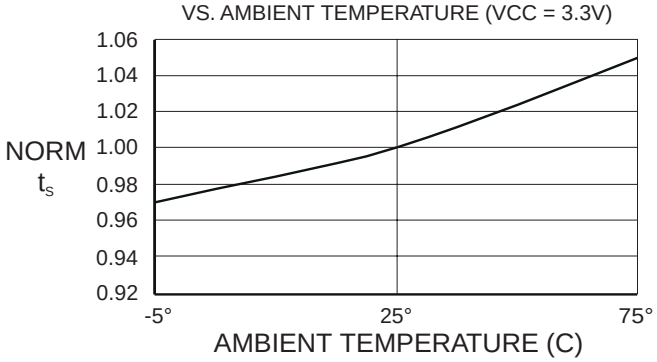
NORMALIZED t_{CO}
VS. AMBIENT TEMPERATURE (VCC = 3.3V)



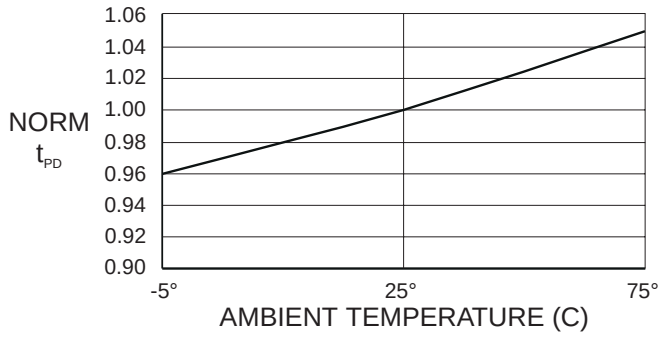
NORMALIZED t_{PD}
VS. SUPPLY VOLTAGE (TA = 25°C)



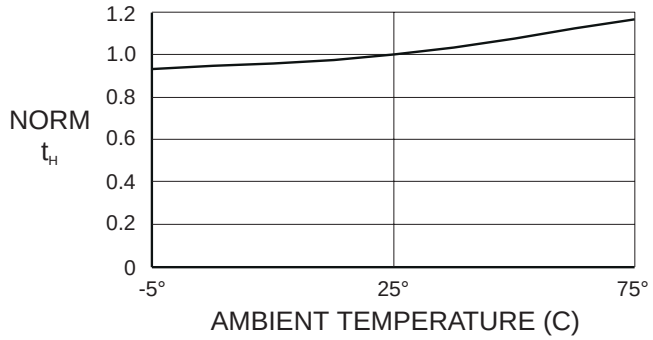
NORMALIZED t_{S}
VS. AMBIENT TEMPERATURE (VCC = 3.3V)



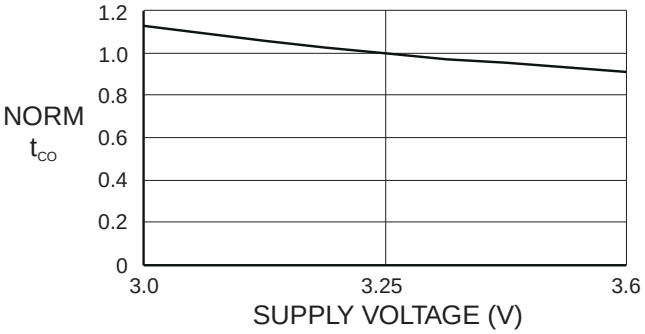
NORMALIZED t_{PD}
VS. AMBIENT TEMPERATURE (VCC = 3.3V)



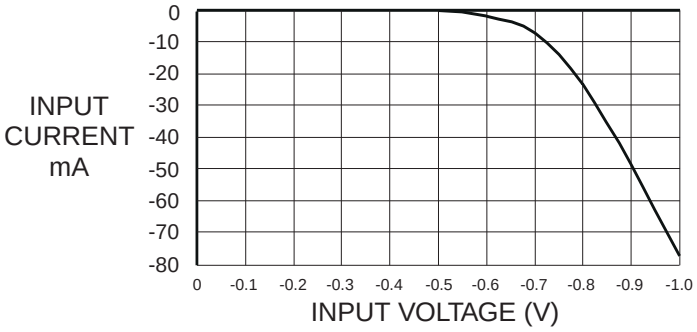
NORMALIZED t_{H}
VS. AMBIENT TEMPERATURE (VCC = 3.3V)



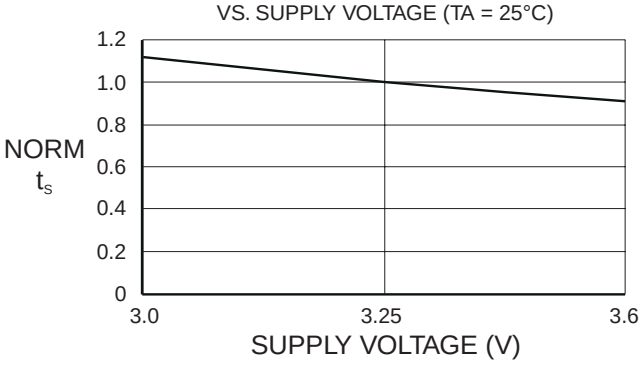
NORMALIZED t_{CO}
VS. SUPPLY VOLTAGE (TA = 25°C)



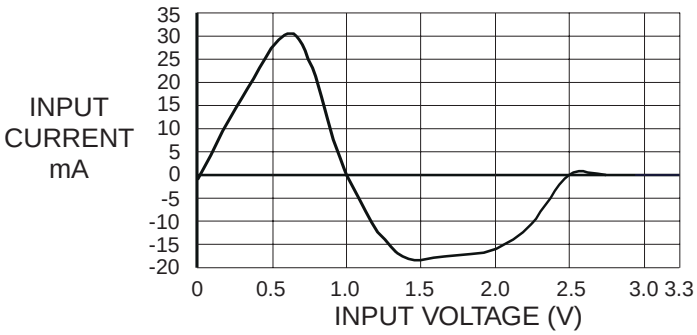
INPUT CLAMP CURRENT
VS. INPUT VOLTAGE (TA = 25°C, VCC = 3.3V)



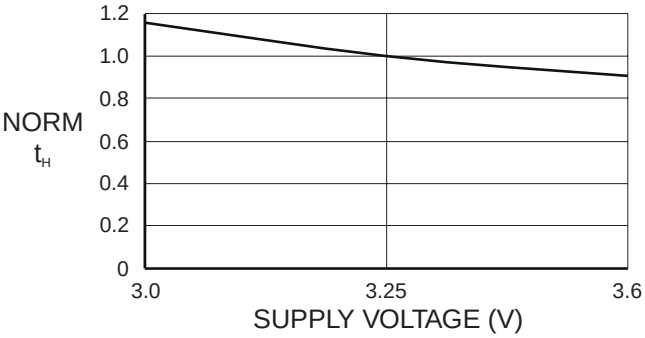
NORMALIZED t_S
VS. SUPPLY VOLTAGE (TA = 25°C)



INPUT CURRENT
VS. INPUT VOLTAGE (TA = 25°C, VCC = 3.3V)



NORMALIZED t_H
VS. SUPPLY VOLTAGE (TA = 25°C)



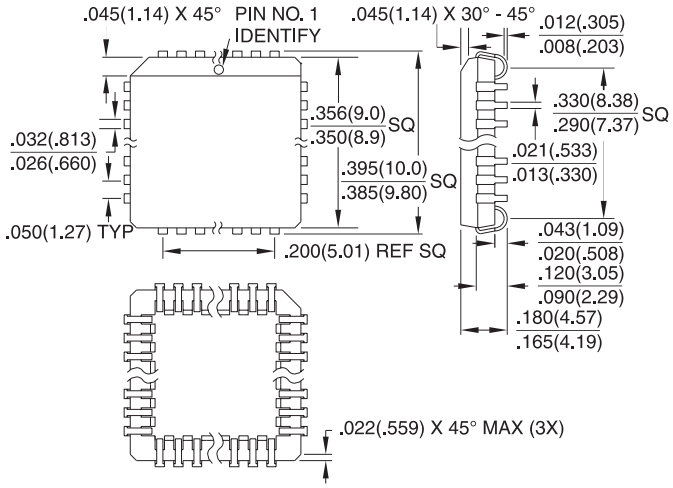
Ordering Information

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package	Operation Range
10	7	7	ATF16LV8C-10JC ATF16LV8C-10PC ATF16LV8C-10SC ATF16LV8C-10XC	20J 20P3 20S 20X	Commercial (0°C to 70°C)
15	12	10	ATF16LV8C-15JC ATF16LV8C-15PC ATF16LV8C-15SC ATF16LV8C-15XC	20J 20P3 20S 20X	Commercial (0°C to 70°C)
10	7	7	ATF16LV8C-10JI ATF16LV8C-10PI ATF16LV8C-10SI ATF16LV8C-10XI	20J 20P3 20S 20X	Industrial (0°C to 85°C)
15	12	10	ATF16LV8C-15JI ATF16LV8C-15PI ATF16LV8C-15SI ATF16LV8C-15XI	20J 20P3 20S 20X	Industrial (0°C to 85°C)

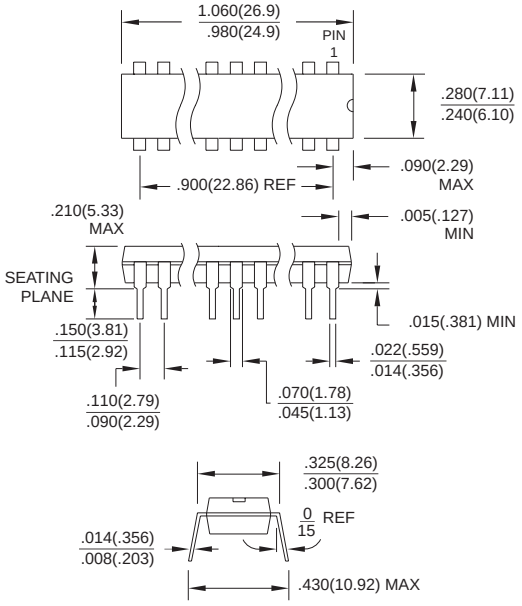
Package Type	
20J	20-Lead, Plastic J-Leaded Chip Carrier (PLCC)
20P3	20-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
20S	20-Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)
20X	20-Lead, 4.4 mm Wide, Plastic Thin Shrink Small Outline (TSSOP)

Packaging Information

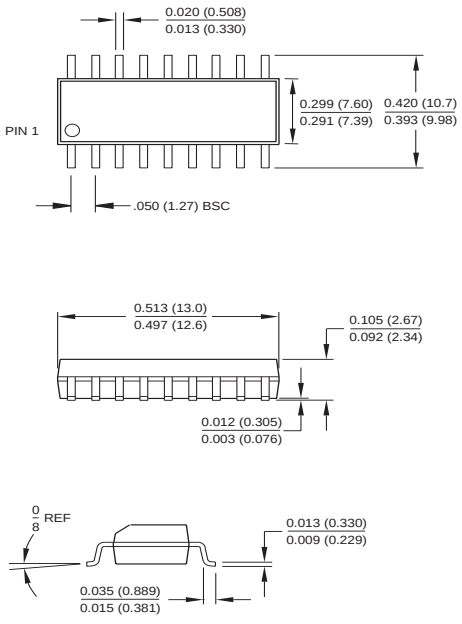
20J, 20-Lead, Plastic J-Leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-018 AA



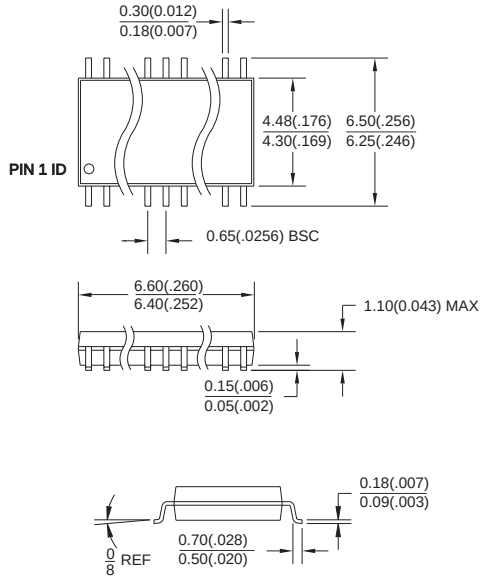
20P3, 20-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-001 AD



20S, 20-Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)
Dimensions in Inches and (Millimeters)



20X, 20-Lead, 4.4 mm Wide, Plastic Thin Shrink Small Outline (TSSOP)
Dimensions in Millimeters and (Inches)*



*Controlling dimension: millimeters.