

DECT Single-Chip Transceiver

Description

The T2801 is an RF IC for low-power DECT applications. The HP-VFQFP-N48-packaged IC is a complete transceiver including image rejection mixer, IF amplifier, FM demodulator, baseband filter, RSSI, TX preamplifier, power-ramping generator for power amplifiers, integrated synthesizer, fully integrated VCO, TX filter and

modulation compensation circuit for advanced closed-loop modulation concept. No mechanical tuning is necessary in production.

Electrostatic sensitive device.

Observe precautions for handling.



Features

- Supply-voltage range 3 V to 4.6 V (unregulated)
- Auxiliary-voltage regulator on-chip
- Low current consumption
- Few low cost external components
- No mechanical tuning required
- Non-blindslot and blindslot operation
- Unlimited multislot operation with advanced closed-loop modulation
- Supports multiple reference clocks (10.368 MHz/ 13.824 MHz/ 20.736 MHz)
- TX preamplifier with 0 dBm output power at 1.9 GHz and ramp-signal generator for SiGe power amplifier

Block Diagram

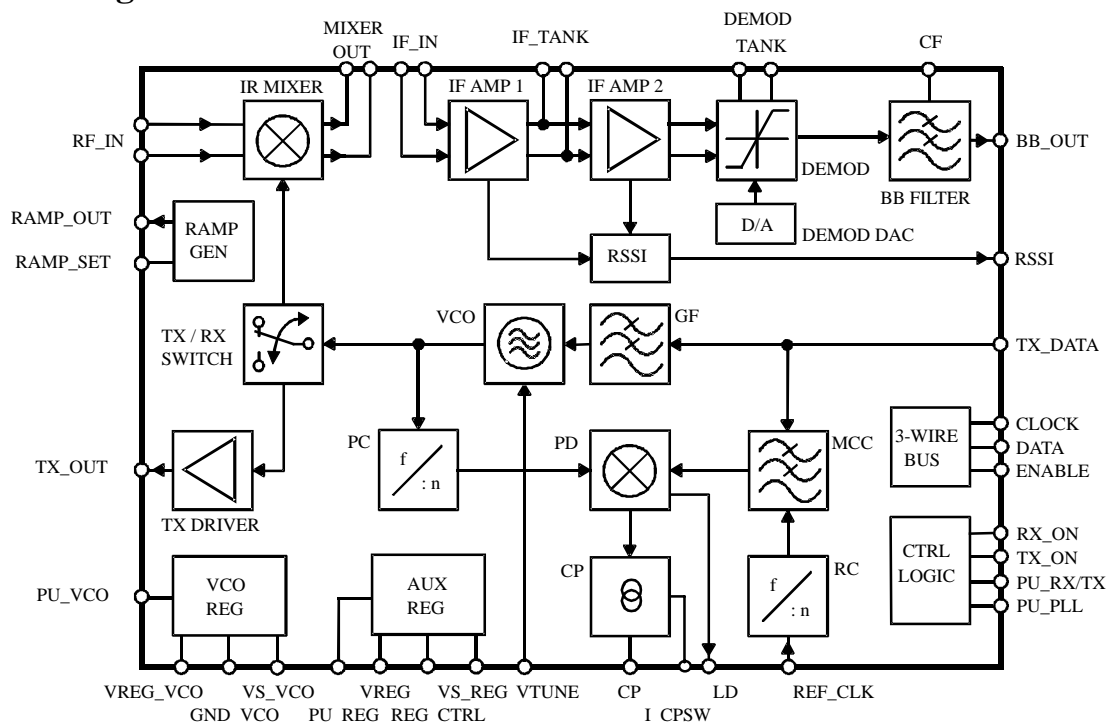


Figure 1. Block diagram

Ordering Information

| Extended Type Number | Package | Remarks |
|----------------------|--------------|------------------|
| T2801-PLH | HP-VFQFP-N48 | Taped and reeled |

Functional Block Description

| Name | Description |
|----------|--------------------------------------|
| AUX REG | Auxiliary voltage regulator |
| BBF | Baseband filter |
| CP | Charge pump |
| DAC | D/A converter for demodulator tuning |
| DEM0D | Demodulator |
| GF | Gaussian filter for transmit data |
| IF AMP1 | 1st intermediate frequency amplifier |
| IF AMP2 | 2nd intermediate frequency amplifier |
| IR MIXER | Image rejection mixer |
| MCC | Modulation compensation circuit |

| Name | Description |
|--------------|---|
| PC | Programmable counter |
| PD | Phase detector |
| RAMP GEN | Ramp-signal generator |
| RC | Reference counter |
| RSSI | Received signal-strength indicator |
| TX DRIVER | Buffer amplifier for TX_OUT |
| TX/RX SWITCH | Switches VCO signal to IR MIXER resp. TX DRIVER |
| VCO | Voltage-controlled oscillator |
| VCO REG | Voltage regulator for VCO |

Pinning

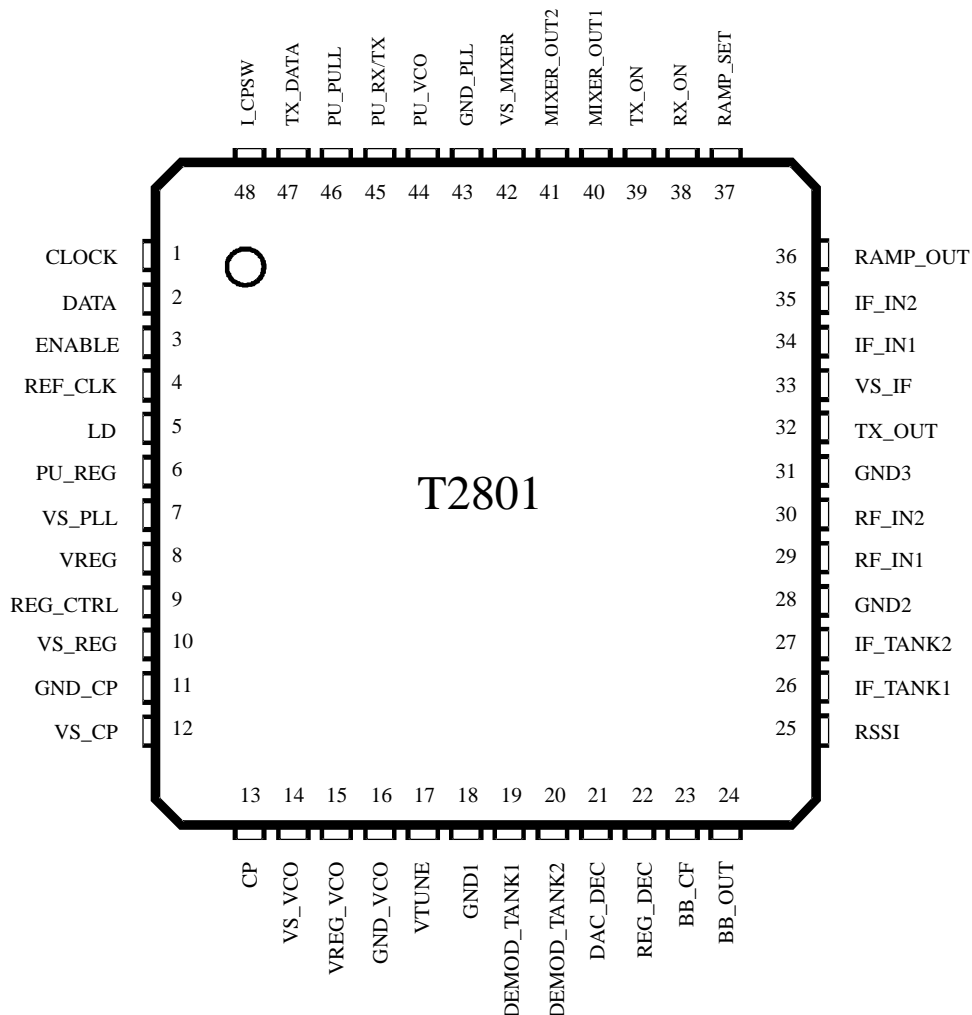


Figure 2. Pinning

Pin Description

| Pin | Symbol | Function | Configuration |
|-----|---------|---|---------------|
| 1 | CLOCK | 3-wire-bus: Clock input | |
| 2 | DATA | 3-wire-bus: Data input | |
| 3 | ENABLE | 3-wire-bus: Enable input | |
| 4 | REF_CLK | Reference-frequency input | |
| 5 | LD | Lock-detect output | |
| 6 | PU_REG | Power-up input for aux. voltage regulator | |

Pin Description (continued)

| Pin | Symbol | Function | Configuration |
|-----|----------|---------------------------------------|---------------|
| 7 | VS_PLL | PLL supply voltage | |
| 8 | VREG | Aux. voltage-regulator output | |
| 9 | REG_CTRL | Aux. voltage-regulator control output | |
| 10 | VS_REG | Aux. voltage-regulator supply voltage | |
| 11 | GND_CP | Charge-pump ground | |
| 12 | VS_CP | Charge-pump supply voltage | |
| 13 | CP | Charge-pump output | |

Pin Description (continued)

| Pin | Symbol | Function | Configuration |
|-----|----------|--------------------------------------|---------------|
| 14 | VS_VCO | VCO voltage-regulator supply voltage | |
| 15 | VREG_VCO | VCO voltage-regulator control output | |
| 16 | GND_VCO | VCO ground | |
| 17 | VTUNE | VCO tuning voltage input | |
| 18 | GND1 | Ground | |

Pin Description (continued)

| Pin | Symbol | Function | Configuration |
|-----|-------------|--|---------------|
| 19 | DEMOD_TANK1 | Demodulator tank circuit | |
| 20 | DEMOD_TANK2 | Demodulator tank circuit | |
| 21 | DAC_DEC | Decoupling PIN for VCO_DAC | |
| 22 | REG_DEC | Decoupling PIN for VCO_REG | |
| 23 | BB_CF | Baseband filter corner-frequency control input | |

Pin Description (continued)

| Pin | Symbol | Function | Configuration |
|-----|----------|---|---------------|
| 24 | BB_OUT | Baseband filter output | |
| 25 | RSSI | Received signal-strength indicator output | |
| 26 | IF_TANK1 | IF tank circuit | |
| 27 | IF_TANK2 | IF tank circuit | |
| 28 | GND2 | Ground | |

Pin Description (continued)

| Pin | Symbol | Function | Configuration |
|-----|--------|-----------------------------------|---------------|
| 29 | RF_IN1 | RF input of image reject mixer | |
| 30 | RF_IN2 | RF input of image reject mixer | |
| 31 | GND3 | Ground | |
| 32 | TX_OUT | TX driver amplifier output for PA | |

Pin Description (continued)

| Pin | Symbol | Function | Configuration |
|-----|----------|--|---------------|
| 33 | VS_IF | IF amplifier supply voltage | |
| 34 | IF_IN1 | IF input of IF amplifier | |
| 35 | IF_IN2 | IF input of IF amplifier | |
| 36 | RAMP_OUT | Ramp-generator output for PA power ramping | |

Pin Description (continued)

| Pin | Symbol | Function | Configuration |
|-----|------------|-------------------------------------|---------------|
| 37 | RAMP_SET | Slew-rate setting of ramping signal | |
| 38 | RX_ON | RX control input | |
| 39 | TX_ON | TX control input | |
| 40 | MIXER_OUT1 | Mixer output to SAW filter | |
| 41 | MIXER_OUT2 | Mixer output to SAW filter | |

Pin Description (continued)

| Pin | Symbol | Function | Configuration |
|-----|----------|----------------------|---------------|
| 42 | VS_MIXER | Mixer supply voltage | |
| 43 | GND_PLL | PLL ground | |
| 44 | PU_VCO | VCO power-up input | |
| 45 | PU_RX/TX | RX/TX power-up input | |

Pin Description (continued)

| Pin | Symbol | Function | Configuration |
|-----|---------|--|---------------|
| 46 | PU_PLL | PLL power-up input | |
| 47 | TX_DATA | TX data input of Gaussian filter and modulation-compensation circuit | |
| 48 | I_CPSW | Charge pump switch input controls charge pump current | |

Functional Description

Receiver

The RF signal at RF_IN is fed to an image rejection mixer IR_MIXER with its differential outputs MIXER_OUT1 and MIXER_OUT2 driving an IF-SAW filter at 110.592 MHz or 112.32 MHz. The IF amplifiers IF_AMP1 and IF_AMP2 with an external IF_TANK and an integrated RSSI function feed the signal to the demodulator DEMOD working at $f = f_{IF}/2$ (≈ 55 MHz) and finally to an integrated baseband filter BB. For demodulator tuning in production an integrated 5-bit digital-to-analog (D/A) converter is provided to control the on-chip varicap diode.

Transmitter

The transmit data at TX_DATA is filtered by an integrated Gaussian Filter GF and fed to the fully integrated VCO operating at twice the output frequency. After modulation the signal is frequency-divided by 2 and fed via a TX/RX SWITCH to the TX_DRIVER. This bus-controlled driver amplifier supplies typical +3 dBm output power at TX_OUT. A ramp-signal generator RAMP_GEN, provides a ramp signal at RAMP_OUT for the external power amplifier, is integrated. The slope of the ramp signal is controlled by a capacitor at the RAMP_SET pin.

Synthesizer

The IR_MIXER, the TX_DRIVER and the programmable counter PC are driven by the fully integrated VCO (including on-chip inductors and varactors). An 3-bit digital-to-analog converter is used to pretune the frequency. The output signal is frequency-divided to supply the desired frequency to the TX_DRIVER, 0/90 degree phase shifter for the IR_MIXER and to be used by the PC for the phase detector PD ($f_{PD} = 3.456$ MHz). Unlimited multislot operation is possible by using the integrated advanced closed-loop modulation concept based on the modulation compensation circuit MCC.

Power Supply

An integrated bandgap-stabilized voltage regulator for use with an external low-cost PNP transistor is implemented. Multiple power-down and current saving modes are provided.

PLL Principle

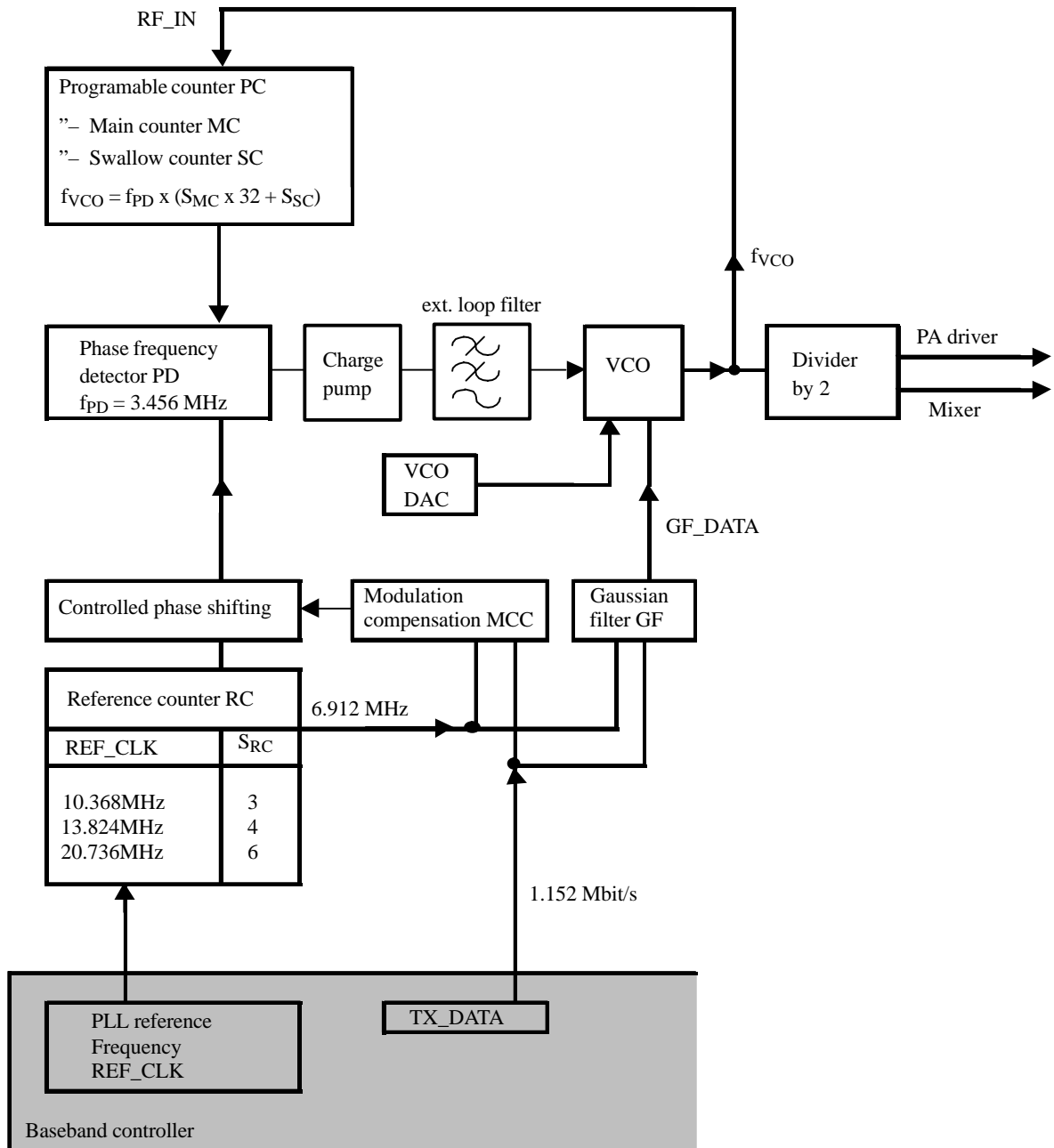


Figure 3.

The following table shows the LO frequencies for RX and TX for the DECT band plus additional channels for the extended DECT band. Intermediate frequencies of 110.592 MHz and 112.32 MHz are supported.

Table 1 LO frequencies

| Mode | f_{IF}/MHz | Channel | f_{ANT}/MHz | f_{VCO}/MHz | S_{MC} | S_{SC} |
|------|---------------------|---------|----------------------|----------------------|----------|----------|
| TX | | C9 | 1881.792 | 1881.792 | 34 | 1 |
| | | C8 | 1883.520 | 1883.520 | 34 | 2 |
| | | ... | ... | ... | ... | ... |
| | | C1 | 1895.616 | 1895.616 | 34 | 9 |
| | | C0 | 1897.344 | 1897.344 | 34 | 10 |
| | | C10 | 1899.072 | 1899.072 | 34 | 11 |
| | | C11 | 1900.800 | 1900.800 | 34 | 12 |
| | | ... | ... | ... | ... | ... |
| | | C29 | 1931.904 | 1931.904 | 34 | 30 |
| | | C30 | 1933.632 | 1933.632 | 34 | 31 |
| | | RX | 110.592 | C9 | 1881.792 | 1771.200 |
| C8 | 1883.520 | | | 1772.928 | 32 | 2 |
| ... | ... | | | ... | ... | ... |
| C1 | 1895.616 | | | 1785.024 | 32 | 9 |
| C0 | 1897.344 | | | 1786.752 | 32 | 10 |
| C10 | 1899.072 | | | 1788.480 | 32 | 11 |
| C11 | 1900.800 | | | 1790.208 | 32 | 12 |
| ... | ... | | | ... | ... | ... |
| C29 | 1931.904 | | | 1821.312 | 32 | 30 |
| C30 | 1933.632 | | | 1823.040 | 32 | 31 |
| RX | 112.320 | | | C9 | 1881.792 | 1769.472 |
| | | C8 | 1883.520 | 1771.200 | 32 | 1 |
| | | ... | ... | ... | ... | ... |
| | | C1 | 1895.616 | 1783.296 | 32 | 8 |
| | | C0 | 1897.344 | 1785.024 | 32 | 9 |
| | | C10 | 1899.072 | 1786.752 | 32 | 10 |
| | | C11 | 1900.800 | 1788.480 | 32 | 11 |
| | | ... | ... | ... | ... | ... |
| | | C29 | 1931.904 | 1819.584 | 32 | 29 |
| | | C30 | 1933.632 | 1821.312 | 32 | 30 |

Formula

$$\text{TX: } f_{ANT} = f_{VCO} = 1.728 \text{ MHz} \times (32 \times S_{MC} + S_{SC})$$

$$\text{RX: } f_{ANT} = 1.728 \text{ MHz} \times (32 \times S_{MC} + S_{SC}) + f_{IF}$$

Control Signals

Table 2

| Signal | Function |
|------------------------|---|
| I_CPSW | Controls the charge pump current |
| PU_REG | Activates AUX voltage regulator supplying the complete transceiver. |
| PU_VCO | Activates VCO voltage regulator which supplies only the VCO. |
| PU_RX/TX | Activates RX/TX switch. |
| PU_PLL | Activates PLL circuits: PC, PD, CP, RC |
| RX_ON | Activates RX circuits: BBF, DEMOD, IF AMP, IR MIXER |
| TX_ON | Activates TX circuits: TX-DRIVER, RAMP GEN. Starts RAMP SIGNAL at RAMP OUT. |
| Data Word 1 Bit D10 | Activates GF in TX mode. |
| Data Word 1 Bit D9 | Activates MCC in TX mode. |

Table 3

| Mode | TX Mode | RX Mode | RSSI Only |
|---|---------|---------|-----------|
| PU_REG | 1 | 1 | 1 |
| PU_VCO | 1 | 1 | 1 |
| PU_RX/TX | 1 | 1 | 1 |
| PU_PLL | 1 | 1 | 1 |
| RX_ON | 0 | 1 | 1 |
| TX_ON | 1 | 0 | 1 |
| BB filter | OFF | ON | OFF |
| Demodulator | OFF | ON | OFF |
| IF amplifiers and RSSI | OFF | ON | ON |
| IR mixer | OFF | ON | ON |
| RX switch | OFF | ON | ON |
| TX switch | ON | OFF | OFF |
| TX driver | ON | OFF | OFF |
| Ramp generator | ON | OFF | OFF |
| Programmable counter | ON | ON | ON |
| Voltage-controlled oscillator | ON | ON | ON |
| Gaussian filter | ON | OFF | OFF |
| Phase detector / charge pump | ON | ON | ON |
| Modulation compensation circuit | ON | OFF | OFF |
| Reference counter | ON | ON | ON |
| Typ. current consumption / mA @ $V_S = 3.2$ V | 54 | 85 | 80 |

Serial Programming Bus

The transceiver is programmed by the 3-wire bus (CLOCK, DATA and ENABLE).

After setting enable signal to low condition, on the rising edge of the clock signal, the data is transferred bit by bit into the shift register, starting with the MSB-bit. After enable returning to high condition the programmed information is loaded into the addressed latches, according to the addressbit condition (last bit). Additional leading bits are ignored and there is no check made how

many pulses arrived during enable-low condition. During enable low condition the bus current is increased to speed up the bus logic.

The programming of the transceiver is separated into two data words. Data word 1 controls mainly the channel information together with settings, which are closely related with the channel. Dataword 2 holds setup information, which is adjusted during production.

Data Word 1

| MSB | | | | | | | | | | | | | | | | | | | | | | LSB | |
|-----------|-----|-----|-----|-----|-----|-----|-----|-----|------|-----|-----|-----|-----|------|----|----|--------|----|----|------|----|-------------|----|
| Data bits | | | | | | | | | | | | | | | | | | | | | | Address bit | |
| D22 | D21 | D20 | D19 | D18 | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | A0 |
| RC | | SC | | | | | MC | | VCOS | 1 | 1 | GF | MCC | GFCS | | | VCODAC | | | CPCS | | | 1 |

Data Word 2

| E10 | E9 | E8 | E7 | E6 | E5 | E4 | E3 | E2 | E1 | E0 | A0 |
|----------|----|----|----|----|------|----|----|------|----|----|----|
| DEMOSDAC | | | | | MCCS | | | TEST | | | 0 |

Data Word 1 Programs

PLL Settings

With the Reference Counter bits D21 – D22

| RC (Reference Counter) | | | |
|------------------------|-----|-----------------|------------|
| D22 | D21 | S _{RC} | REF_CLK |
| 0 | 0 | 3 | 10.368 MHz |
| 0 | 1 | 4 | 13.824 MHz |
| 1 | 0 | 6 | 20.736 MHz |

With the Main Counter bits D14 – D15

| MC (Main Counter) | | |
|-------------------|-----|-----------------|
| D15 | D14 | S _{MC} |
| 0 | 0 | 32 |
| 0 | 1 | 33 |
| 1 | 0 | 34 |
| 1 | 1 | 35 |

With the Swallow Counter bits D16 – D20

| SC (Swallow Counter) | | | | | |
|----------------------|-----|-----|-----|-----|-----------------|
| D20 | D19 | D18 | D17 | D16 | S _{SC} |
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | 1 | 0 | 2 |
| ... | | | | | ... |
| 1 | 1 | 1 | 0 | 1 | 29 |
| 1 | 1 | 1 | 1 | 0 | 30 |
| 1 | 1 | 1 | 1 | 1 | 31 |

VCO Select (RX/TX VCO)

With bit D13

Used to switch between RX/TX VCO

| D13 | VCOS (VCO Select) |
|-----|-------------------|
| 0 | RX-VCO |
| 1 | TX-VCO |

Gaussian Filter on/off

With bit D10

GF is used only in TX mode

| D10 | GF (Gaussian Filter) |
|-----|----------------------|
| 0 | OFF |
| 1 | ON |

Modulation Compensation Circuit on/off

With bit D9

MCC is used only in TX mode

| D9 | MCC (Modulation Compensation Circuit) |
|----|---------------------------------------|
| 0 | OFF |
| 1 | ON |

GFCS Adjustment

With bit D6 – D8

Only in TX mode effective for setting the frequency deviation of the modulation

| GFCS (Gaussian Filter Settings) | | | |
|---------------------------------|----|----|------|
| D8 | D7 | D6 | GFCS |
| 0 | 0 | 0 | 60% |
| 0 | 0 | 1 | 70% |
| 0 | 1 | 0 | 80% |
| 0 | 1 | 1 | 90% |
| 1 | 0 | 0 | 100% |
| 1 | 0 | 1 | 110% |
| 1 | 1 | 0 | 120% |
| 1 | 1 | 1 | 130% |

VCO_DAC Adjustment

With bit D3 – D5

Used to pretune the VCO frequency in case of production tolerances of the device. Tuning voltage in locked condition should be around 1.8 V at room temperature. This gives margin for ambient temperature changes.

| Pretune DAC Voltage | | | |
|---------------------|----|----|---------------------|
| D5 | D4 | D3 | f _{VCO} /% |
| 0 | 0 | 0 | -5 |
| 0 | 0 | 1 | ... |
| 0 | 1 | 0 | ... |
| 0 | 1 | 1 | ... |
| 1 | 0 | 0 | ... |
| 1 | 0 | 1 | ... |
| 1 | 1 | 0 | ... |
| 1 | 1 | 1 | 5 |

CPCS Adjustment

With bit D0 – D2

Used to adjust the charge pump current. This can be used to compensate the change of the tuning sensitivity over frequency and device tolerances.

| CPCS (Charge-Pump Current Settings) | | | |
|-------------------------------------|----|----|------|
| D2 | D1 | D0 | CPCS |
| 0 | 0 | 0 | -4 |
| 0 | 0 | 1 | -3 |
| 0 | 1 | 0 | -2 |
| 0 | 1 | 1 | -1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 2 |
| 1 | 1 | 1 | 3 |

Data Word 2 Programs

DEMODODAC Adjustment

With bits E6 – E10

Only in RX mode effective. Used to tune the demodulator center frequency and allows to compensate tolerances of external components and the T2801.

| Demod DAC Voltage | | | | | |
|-------------------|----|----|----|----|-------------------------|
| E10 | E9 | E8 | E7 | E6 | f _{IFcenter} % |
| 0 | 0 | 0 | 0 | 0 | -5 |
| 0 | 0 | 0 | 0 | 1 | ... |
| 0 | 0 | 0 | 1 | 0 | ... |
| | | | | | ... |
| 1 | 1 | 1 | 0 | 1 | ... |
| 1 | 1 | 1 | 1 | 0 | ... |
| 1 | 1 | 1 | 1 | 1 | 5 |

MCCS Adjustment

With bits E3 – E5

Only in TX mode effective. Adjusts the modulation compensation circuit for closed loop modulation. This adjustment is done with a test sequence of a long stream of ,1' – ,0'. The correct setting is achieved, if the modulation is not affected by the PLL.

| MCCS (Modulation Compensation Settings) | | | |
|---|----|----|------|
| E5 | E4 | E3 | MCCS |
| 0 | 0 | 0 | 60% |
| 0 | 0 | 1 | 70% |
| 0 | 1 | 0 | 80% |
| 0 | 1 | 1 | 90% |
| 1 | 0 | 0 | 100% |
| 1 | 0 | 1 | 110% |
| 1 | 1 | 0 | 120% |
| 1 | 1 | 1 | 130% |

TEST Mode Settings

With bit E0 – E2 and D11

In normal operation Lock detect output is used. All other settings are for test only.

| D11 | E2 | E1 | E0 | Signal at lock detect output | CP mode |
|-----|----|----|----|------------------------------------|-----------|
| 1 | 0 | 0 | 0 | Lock detect | Active |
| 0 | 0 | 0 | 1 | RC out | Active |
| 1 | 0 | 1 | 0 | PC out | Active |
| X | 0 | 1 | 1 | MCCTEST: RC out divided by 2048 | Active |
| 1 | 1 | 0 | 0 | Lock detect | High imp. |
| 0 | 1 | 0 | 1 | RC out | High imp. |
| 1 | 1 | 1 | 0 | PC out | High imp. |
| X | 1 | 1 | 1 | GFTEST: RC out divided by 2 | High imp. |

3-Wire Bus Protocol Timing Diagram

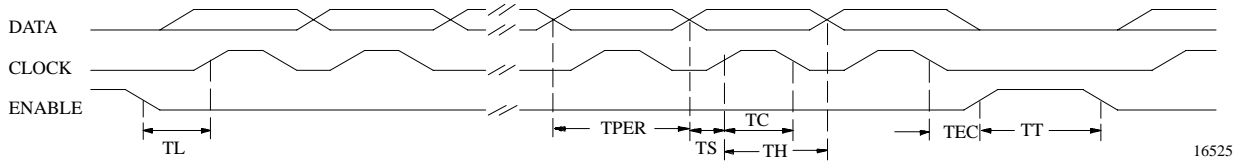
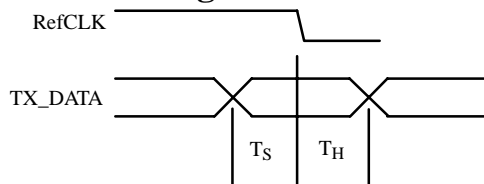


Figure 4.

| Description | Symbol | Min. Value | Unit |
|----------------------------|--------|------------|------|
| Clock period | TPER | 125 | ns |
| Set time data to clock | TS | 60 | ns |
| Hold time data to clock | TH | 60 | ns |
| Clock pulse width | TC | 60 | ns |
| Set time enable to clock | TL | 200 | ns |
| Hold time enable to data | TEC | 0 | ns |
| Time between two protocols | TT | 250 | ns |

TX DATA Timing



| | | |
|---------------------|----|-------|
| Set-up time TX DATA | TS | 10 ns |
| Hold time TX DATA | TH | 10 ns |

TS and TH must be considered for both (falling and rising) edges of RefCLK when using REF_CLK = 10.368 MHz.

Figure 5. TX DATA timing

Absolute Maximum Ratings

All voltages refer to GND

| Parameter | Symbol | Min. | Max. | Unit |
|---|--------------|------|-------|------|
| Supply voltage regulator Pin 10 | V_{S_REG} | 3.2 | 4.7 | V |
| Supply voltage Pins 7, 12, 14, 33 and 42 | V_S | 3.0 | 4.7 | V |
| Logic input voltage Pins 1, 2, 3, 38, 39, 44, 45, 46, 47 and 48 | V_{IN} | -0.3 | V_S | V |
| Junction temperature | T_{jmax} | | 150 | °C |
| Storage temperature | T_{stg} | -40 | 150 | °C |

Thermal Resistance

| Parameter | Symbol | Value | Unit |
|------------------|------------|--------|------|
| Junction ambient | R_{thJA} | t.b.d. | K/W |

Operating Range

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|--|--------------|------|------|------|------|
| Supply voltage regulator Pins 10 | V_{S_REG} | 3.2 | 3.6 | 4.6 | V |
| Supply voltage Pins 7, 12, 14, 33 and 42 | V_S | 3.0 | 3.0 | 4.6 | V |
| Ambient temperature | T_{amb} | -25 | | +85 | °C |

Electrical Characteristics

Test conditions (unless otherwise specified): $V_{S_REG} = 3.2$ V, $T_{amb} = 25^\circ\text{C}$

| Parameter | Test Conditions / Pins | Symbol | Min. | Typ. | Max. | Unit |
|--|--|-----------------|------|---------|------|------------|
| IR mixer Pins 29, 30, 40 and 41 | | | | | | |
| Input impedance | Pins 29 and 30 | Z_{in} | | 50 | | Ω |
| Input matching | Pins 29 and 30 | $V_{SWR_{in}}$ | | <2:1 | | |
| Image rejection ratio | Pins 40 and 41 | IRR | | 20 | | dB |
| DSB noise figure | Pins 40 and 41 | NFDSB= NFSSB | | 10 | | dB |
| Conversion gain | $R_{load} = 200 \Omega$ | G_{conv} | | 11 | | dB |
| Input interception point | Pins 40 and 41 | IIP3 | | -10 | | dBm |
| IF amplifier Pins 26, 27, 34 and 35 | | | | | | |
| Input impedance | Pins 34 and 35 | Z_{in} | 200 | | 400 | Ω |
| Lower cut-off frequency | | f_{l3dB} | | 90 | | MHz |
| Upper cut-off frequency | | f_{u3dB} | | 130 | | MHz |
| Power gain | | G_p | | 85 | | dB |
| Bandwidth of external tank circuit | Pins 26 and 27 | BW3dB | | 10 | | MHz |
| Noise figure | | NF | | 9 | | dB |
| RSSI Pins 25, 34 and 35 | | | | | | |
| RSSI sensitivity | at IF_IN1, IF_IN2 Pins 34 and 35 | P_{min} | | 20 | | dB μ V |
| RSSI compression | at IF_IN1, IF_IN2 Pins 34 and 35 | P_{max} | | 100 | | dB μ V |
| RSSI dynamic range | | DR | | 80 | | dB |
| RSSI resolution | Slope of the RSSI has to be steady | Acc | | ± 2 | | dB |
| RSSI rise time | $P_{in} = 30$ to 100 dB μ V, Pin 25 | t_r | | 1 | | μ s |
| RSSI fall time | $P_{in} = 100$ to 30 dB μ V, Pin 25 | t_f | | 1 | | μ s |
| Quiescent output current | @ $P_{in} < 20$ dB μ V at IF_IN1, IF_IN2 Pin 25 | I_{out} | | 30 | | μ A |
| Maximum output current | @ $P_{in} = 100$ dB μ V at IF_IN1, IF_IN2 Pin 25 | I_{out} | | 150 | | μ A |

Electrical Characteristics (continued)

Test conditions (unless otherwise specified): $V_{S_REG} = 3.2\text{ V}$, $T_{amb} = 25^\circ\text{C}$

| Parameter | Test Conditions / Pins | Symbol | Min. | Typ. | Max. | Unit |
|---|---|-----------------------|------|----------------------------|-----------|-------------------|
| FM demodulator, BB-Filter Pins 19, 20, 23 and 24 | | | | | | |
| Co-channel rejection ratio | @ $P_{in} = -75\text{ dBm}$ at IR-mixer input | CCRR | | 10 | | dB |
| Sensitivity | Quality factor of external tank circuit approx. 20, $f_{res} = F_{IF}/2$, Pin 24 | S | | 0.5 | | V/MHz |
| Amplitude of recovered signal | Nominal deviation of signal $\pm 288\text{ kHz}$, Pin 24 | A | | 450 | | mV _{SS} |
| Corner frequency | Pin 23: C = 68 pF | f_c | | 680 | | kHz |
| Output voltage DC range | Pin 24 | V_{outDC} | 1 | | $V_S - 1$ | V |
| DAC for FM demodulator (internally connected) | | | | | | |
| DEMOD_DAC range | (see bus protocol E6 ... E10) | $\Delta f_{IFcenter}$ | | ± 5 | | % |
| VCO | | | | | | |
| RX-VCO frequency range | VCOS = '0' Bit D13 | f_{vco} | 1750 | | 1840 | MHz |
| TX-VCO frequency range | VCOS = '1' Bit D13 | f_{vco} | 1860 | | 1950 | MHz |
| Tuning gain | | G_{tune} | | 40 | | MHz/V |
| Frequency control voltage range | Pin 17 | V_{tune} | 0.4 | | 2.8 | V |
| VCO_DAC range | (see bus protocol D3 ... D5) | $\Delta f_{vco,DAC}$ | | ± 5 | | % |
| PLL | | | | | | |
| Scaling factor prescaler | | S_{PSC} | | 32 / 33 | | |
| Scaling factor main counter | | S_{MC} | | 32 / 33 / 34 / 35 | | |
| Scaling factor swallow counter | | S_{SC} | 0 | | 31 | |
| External reference input frequency | AC coupled sinewave Pin 4 | f_{REF_CLK} | | 10.368 13.824 20.736 | | MHz MHz MHz |
| External reference input voltage | AC coupled sinewave Pin 4 | V_{REF_CLK} | 50 | | 250 | mV _{RMS} |
| Scaling factor reference counter | | S_{RC} | | 3 / 4 / 6 / 8 | | |
| Charge pump Pin 13 | | | | | | |
| Output current | $V_{CP} = V_{VS_CP} / 2$, $I_{CPSW} = '1'$ Pin 48 | I_{CP_nom} | | ± 6.5 | | mA |
| Output current | $V_{CP} = V_{VS_CP} / 2$, $I_{CPSW} = '0'$ Pin 48 | I_{CP_nom} | | ± 1.2 | | mA |
| Current scaling | $I_{CP} = I_{CP_nom} + CPCS * I_{CP_step}$ (see bus protocol D0 ... D2) | I_{CP_step} | | 0.2 | | mA |
| Leakage current | | I_L | | ± 100 | | pA |

Electrical Characteristics (continued)

 Test conditions (unless otherwise specified): $V_{S_REG} = 3.2\text{ V}$, $T_{amb} = 25^{\circ}\text{C}$

| Parameter | Test Conditions / Pins | Symbol | Min. | Typ. | Max. | Unit |
|--|---|----------------|------|-----------|-------|---------------|
| Gaussian transmit filter (Gaussian shape B*T = 0.5) | | | | | | |
| Tx data filter clock | 12 taps in filter | f_{TXFCLK} | | 13.824 | | MHz |
| Frequency deviation | | GF_{FM_nom} | | ± 350 | | kHz |
| Frequency deviation scaling | $GF_{FM} = GF_{FM_nom} * GFCS$ (see bus protocol D6 ... D8) | GFCS | 60 | | 130 | % |
| Modulation compensation circuit | | | | | | |
| Oversampling | | OVS | | 6 | | |
| Digital sum variation | | DSV | | | 85 | |
| Current scaling factor | (see bus protocol E3 ... E5) | MCCS | 60 | | 130 | % |
| VCO switch and TX driver Pin 32 | | | | | | |
| Power gain | @ $P_{in} = -40\text{ dBm}$ | G_p | | 30 | | dB |
| Output impedance | Pin 32 | Z_{out} | | 100 | | Ω |
| Maximum output power | Pin 32 | P_{max} | 0 | 3 | | dBm |
| Gain compression | @ TX_RF_OUT, Pin 32 | P_{1dB} | | 1 | | dBm |
| Output interception point | Pin 32 | OIP3 | | 10 | | dBm |
| Ramp generator Pins 36 and 37 | | | | | | |
| Minimum output voltage | According to RAMP_SET input | V_{min} | | 0.2 | | V |
| Maximum output voltage | According to RAMP_SET input | V_{max} | | 1.95 | | V |
| Rise time | $C_{ramp} = 270\text{ pF}$ at Pin 37 | t_r | | 5 | | μs |
| Fall time | $C_{ramp} = 270\text{ pF}$ at Pin 37 | t_f | | 5 | | μs |
| Lock detect and test mode output Pin 5 | | | | | | |
| Lock detect output, test mode output | locked = '1', unlocked = '0' test modes (see bus protocol E0 ... E2) | LD | | | | |
| Leakage current | $V_{OH} = 4.6\text{ V}$ | I_L | | | 5 | μA |
| Saturation voltage | $I_{OL} = 0.5\text{ mA}$ | V_{SL} | | | 0.4 | V |
| Auxiliary regulator Pins 8, 9 and 10 | | | | | | |
| Output voltage | $V_{SREG} = 3\text{ V}$ Pin 8 | V_{REG} | 2.9 | 3.0 | 3.1 | V |
| Supply voltage rejection | $V_{Pin10} = V_{DC} + 0.1\text{ V}_{pp}$ $f_{Pin10} = 0.1\text{ to }10\text{ kHz}$ $C_{Pin8} = 100\text{ nF}$ | SVR | | t.b.d. | | dB |
| VCO regulator Pins 14, 15 and 12 | | | | | | |
| Output voltage | $V_{SVCO} = 3\text{ V}$ Pin 15 | V_{REG_VCO} | 2.6 | 2.7 | 2.8 | V |
| 3-wire bus | | | | | | |
| Clock | | f_{Clock} | | | 6.912 | MHz |

Electrical Characteristics (continued)

Test conditions (unless otherwise specified): $V_{S_REG} = 3.2\text{ V}$, $T_{amb} = 25^\circ\text{C}$

| Parameter | Test Conditions / Pins | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|------------|------------|------------|--------------------------------|
| Logic input levels (CLOCK, DATA, ENABLE, RX_ON, TX_ON, PU_VCO, TX_DATA, I_CPSW) Pins 1, 2, 3, 38, 39, 44, 47 and 48 | | | | | | |
| High input level | = '1' | V_{iH} | 1.5 | | | V |
| Low input level | = '0' | V_{iL} | | | 0.5 | V |
| High input current | = '1' | I_{iH} | -5 | | 5 | μA |
| Low input current | = '0' | I_{iL} | -5 | | 5 | μA |
| Standby control Pins 6, 45 and 46 | | | | | | |
| Power up PU_REG = '1' PU_RX/TX = '1' PU_PLL = '1' High input level | Pin 6 Pin 45 Pin 46 | V_{PU_REG} $V_{PU_RX/TX}$ V_{PU_PLL} | 2.0 | | | V |
| Standby PU_REG = '0' PU_RX/TX = '0' PU_PLL = '0' Low input level | Pin 6 Pin 45 Pin 46 | $V_{PU_REG,OFF}$ $V_{PU_RX/TX,OFF}$ $V_{PU_PLL,OFF}$ | | | 0.7 | V |
| Power up PU_REG = '1' PU_RX/TX = '1' | $V_{PU} = 3\text{ V}$ Pin 6 $V_{PU} = 5.5\text{ V}$ Pin 45 | I_{PU_REG} $I_{PU_RX/TX}$ | 20 60 | 30 80 | 40 100 | μA μA |
| PU_PLL = '1' High input current | $V_{PU} = 3\text{ V}$ Pin 46 $V_{PU} = 5.5\text{ V}$ | I_{PU_PLL} | 100 200 | 125 300 | 150 400 | μA μA |
| Standby PU_xxxx = '0' Low input current | $V_{PU} = 0\text{ V}$ Pin 6, $V_{PU} = 0.5\text{ V}$ Pins 45, 46 | $I_{PU,OFF}$ | | | 0.1 1 | μA μA |
| Settling time $V_S = 0 \rightarrow$ active operation | Switched from $V_S = 0$ to $V_S = 3\text{ V}$ | t_{soa} | | < 10 | | μs |
| Settling time standby \rightarrow active operation | Switched from PU = '0' to PU = '1' | t_{ssa} | | < 10 | | μs |
| Settling time active operation \rightarrow standby | Switched from PU = '1' to standby | t_{sas} | | < 2 | | μs |
| Power supply Pins 7, 10, 12, 14, 33 and 42 | | | | | | |
| Total supply current | RX | I_S | | 85 | | mA |
| | RSSI only | I_S | | 82 | | mA |
| | TX | I_S | | 54 | | mA |
| | TX (MCC, GF active) | I_S | | 58 | | mA |
| Standby current | PU_RX/TX = GND | I_S | | 1 | 10 | μA |
| Supply current CP | $V_{VS_CP} = 3\text{ V}$, PLL in lock condition Pin 13 | I_{CP} | | 1 | | μA |

Application Circuit

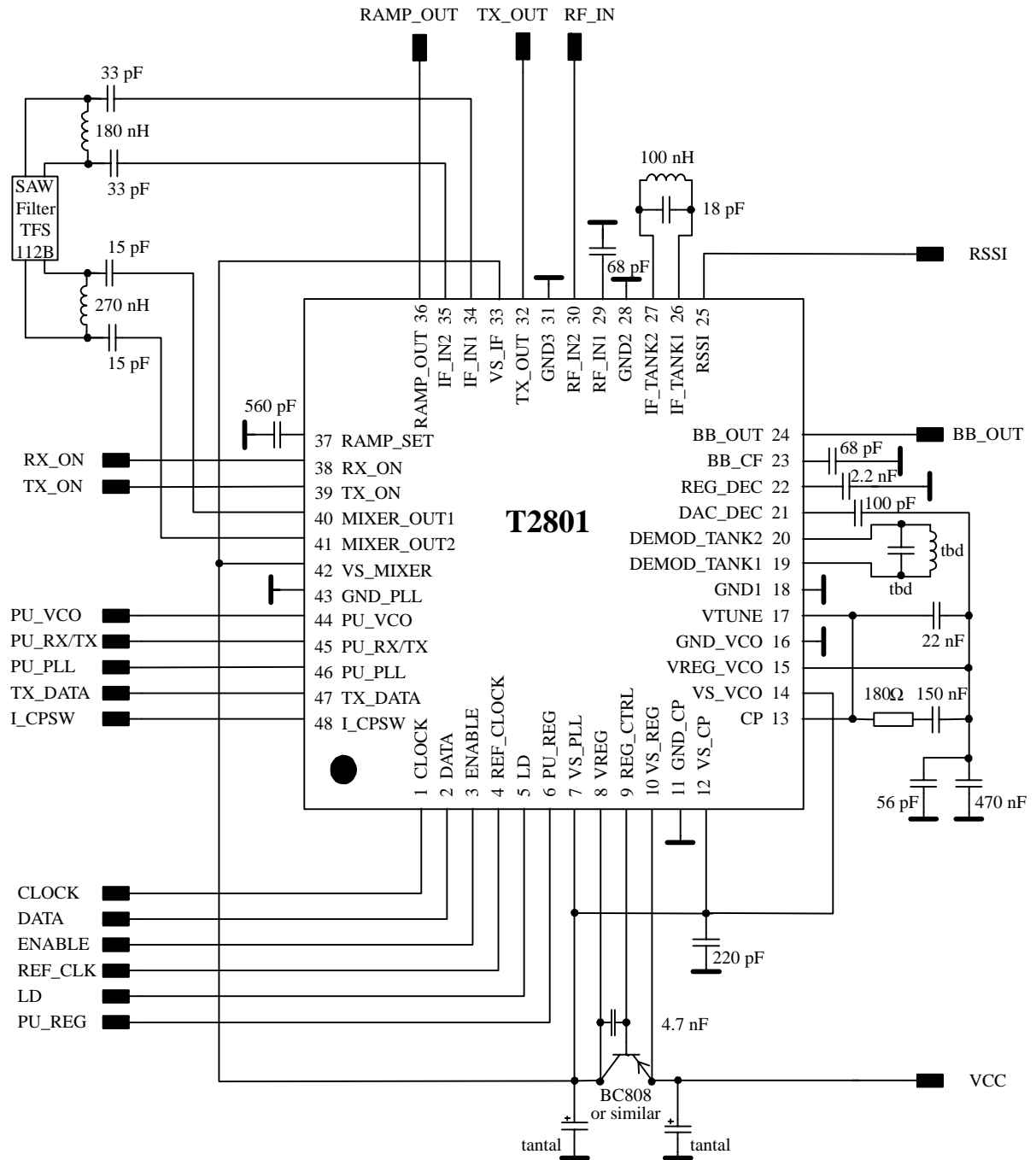
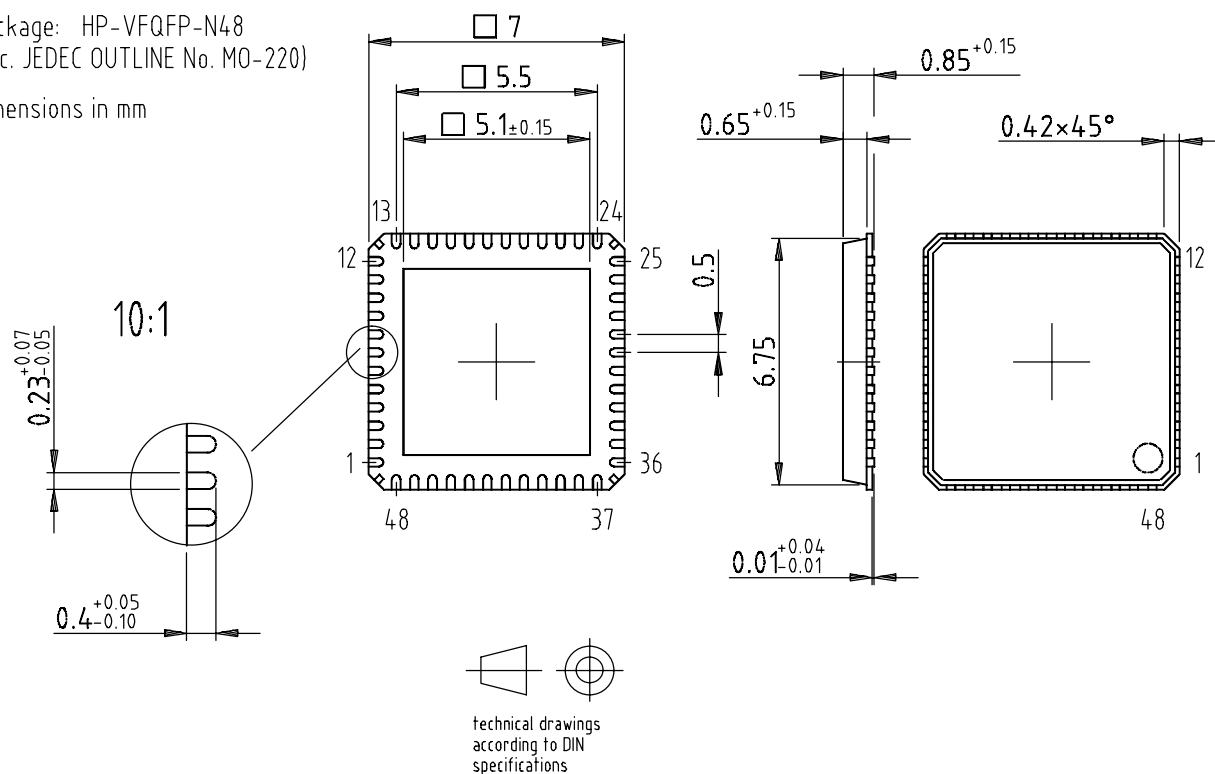


Figure 6. Application circuit

Package Information

Package: HP-VFQFP-N48
(acc. JEDEC OUTLINE No. MO-220)

Dimensions in mm



Ozone Depleting Substances Policy Statement

It is the policy of **Atmel Germany GmbH** to

1. Meet all present and future national and international statutory requirements.
2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

Atmel Germany GmbH has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively
2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA
3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

Atmel Germany GmbH can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

We reserve the right to make changes to improve technical design and may do so without further notice.

Parameters can vary in different applications. All operating parameters must be validated for each customer application by the customer. Should the buyer use Atmel products for any unintended or unauthorized application, the buyer shall indemnify Atmel against all claims, costs, damages, and expenses, arising out of, directly or indirectly, any claim of personal damage, injury or death associated with such unintended or unauthorized use.

Data sheets can also be retrieved from the Internet: <http://www.atmel-wm.com>

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