



## 128K x 8 EEPROM

EEPROM Memory

### AVAILABLE AS MILITARY SPECIFICATIONS

- SMD 5962-38267
- MIL-STD-883

### FEATURES

- High speed: 150, 200, and 250ns
- Data Retention: 10 Years
- Low power dissipation, active current (20mW/MHz (TYP)), standby current (100µW(MAX))
- Single +5V (±10%) power supply
- Data Polling and Ready/Busy Signals
- Erase/Write Endurance (10,000 cycles in a page mode)
- Software Data protection Algorithm
- Data Protection Circuitry during power on/off
- Hardware Data Protection with RES pin
- Automatic Programming:  
Automatic Page Write: 10ms (MAX)  
128 Byte page size

### OPTIONS

- Timing
 

150ns access	-15
200ns access	-20
250ns access	-25
- Packages
 

Ceramic Flat Pack	F	No. 306
Radiation Shielded Ceramic FP*	SF	No. 305
Ceramic SOJ	DCJ	No. 508
- Operating Temperature Ranges
 

-Military (-55°C to +125°C)	XT
-Industrial (-40°C to +85°C)	IT

\*NOTE: Package lid is connected to ground (Vss).

PIN NAME	FUNCTION
A0 to A16	Address input
I/O0 to I/O7	Data input/output
OE\	Output enable
CE\	Chip enable
WE\	Write enable
Vcc	Power supply
Vss	Ground
RDY/Busy\	Ready busy
RES\	Reset

### PIN ASSIGNMENT

(Top View)

32-Pin CFP (F & SF), 32-Pin CSOJ (DCJ)

RDY/BUSY\	1	32	Vcc
A16	2	31	A15
A14	3	30	RES\
A12	4	29	WE\
A7	5	28	A13
A6	6	27	A8
A5	7	26	A9
A4	8	25	A11
A3	9	24	OE\
A2	10	23	A10
A1	11	22	CE\
A0	12	21	I/O 7
I/O 0	13	20	I/O 6
I/O 1	14	19	I/O 5
I/O 2	15	18	I/O 4
Vss	16	17	I/O 3

### GENERAL DESCRIPTION

The Austin Semiconductor, Inc. AS58C1001 is a 1 Megabit CMOS Electrically Erasable Programmable Read Only Memory (EEPROM) organized as 131, 072 x 8 bits. The AS58C1001 is capable or in system electrical Byte and Page reprogrammability.

The AS58C1001 achieves high speed access, low power consumption, and a high level of reliability by employing advanced MNOS memory technology and CMOS process and circuitry technology and CMOS process and circuitry technology.

This device has a 128-Byte Page Programming function to make its erase and write operations faster. The AS58C1001 features Data Polling and a Ready/Busy signal to indicate completion of erase and programming operations.

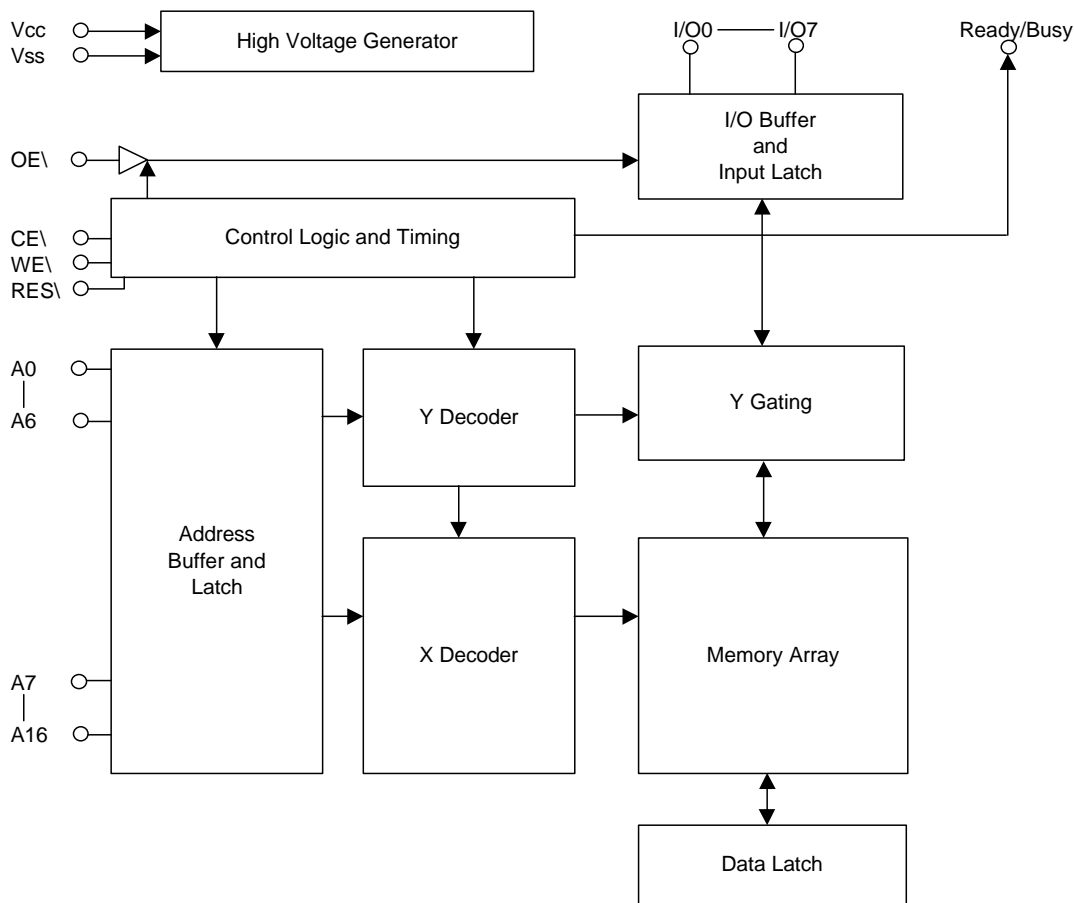
This EEPROM provides several levels of data protection. Hardware data protection is provided with the RES pin, in addition to noise protection on the WE signal and write inhibit during power on and off. Software data protection is implemented using JEDEC Optional Standard algorithm.

The AS58C1001 is designed for high reliability in the most demanding applications. Data retention is specified for 10 years and erase/write endurance is guaranteed to a minimum of 10,000 cycles in the Page Mode.

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## FUNCTIONAL BLOCK DIAGRAM



### MODE SELECTION

MODE	CE\ $\backslash$	OE\ $\backslash$	WE\ $\backslash$	RES\ $\backslash$	RDY/BUSY $\backslash$ <sup>1</sup>	I/O
READ	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>H</sub>	High-Z	D <sub>OUT</sub>
STANDBY	V <sub>IH</sub>	X	X	X	High-Z	High-Z
WRITE	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>H</sub>	High-Z to V <sub>OL</sub>	D <sub>IN</sub>
DESELECT	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IH</sub>	V <sub>H</sub>	High-Z	High-Z
WRITE INHIBIT	X	X	V <sub>IH</sub>	X	---	---
	X	V <sub>IL</sub>	X	X	---	---
DATA POLLING	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>H</sub>	V <sub>OL</sub>	Data Out (I/O7)
PROGRAM	X	X	X	V <sub>IL</sub>	High-Z	High-Z

#### Notes:

1. RDY/Busy\ $\backslash$  output has only active LOW V<sub>OL</sub> and HIGH impedance state. It can not go to HIGH (V<sub>OH</sub>) state.



## FUNCTIONAL DESCRIPTION

### AUTOMATIC PAGE WRITE

The Page Write feature allows 1 to 128 Bytes of data to be written into the EEPROM in a single cycle and allows the undefined data within 128 Bytes to be written corresponding to the undefined address ( $A_0$  to  $A_6$ ). Loading the first Byte of data, the data load window of 30 $\mu$ s opens for the second. In the same manner each additional Byte of data can be loaded within 30 $\mu$ s. In case  $CE\backslash$  and  $WE\backslash$  are kept high for 100 $\mu$ s after data input, the EEPROM enters erase and write automatically and only the input data can be written into the EEPROM. In Page mode the data can be written and accessed  $10^4$  times per page, and in Byte mode  $10^3$  times per Byte.

### DATA\ POLLING

Data\ Polling allows the status of the EEPROM to be determined. If the EEPROM is set to Read mode during a Write cycle, and inversion of the last Byte of data to be loaded outputs from I/O, to indicate that the EEPROM is performing a Write operation.

### WRITE PROTECTION

- (1) Noise protection: Noise on a write cycle will not act as a trigger with a  $WE\backslash$  pulse of less than 20ns.
- (2) Write inhibit: Holding  $OE\backslash$  low,  $WE\backslash$  high or  $CE\backslash$  high, inhibits a write cycle during power on/off.

### $WE\backslash$ AND $CE\backslash$ PIN OPERATION

During a write cycle, addresses are latched by the falling edge of  $WE\backslash$  or  $CE\backslash$ , and data is latched by the rising edge of  $WE\backslash$  or  $CE\backslash$ .

### WRITE/ERASE ENDURANCE AND DATA RETENTION

The endurance with page programming is  $10^4$  cycles (1% cumulative failure rate) and the data retention time is more than 10 years when a device is programmed less than  $10^4$  cycles.

### RDY/Busy\ SIGNAL

RDY/Busy\ signal also allows status of the EEPROM to be determined. The RDY/Busy\ signal has high impedance except in write cycle and is lowered to  $V_{OL}$  after the first write signal. At the end of the write cycle, the RDY/Busy\ signal changes state to high impedance. This allows many 58C1001 devices RDY/Busy\ signal lines to be wired-OR together.

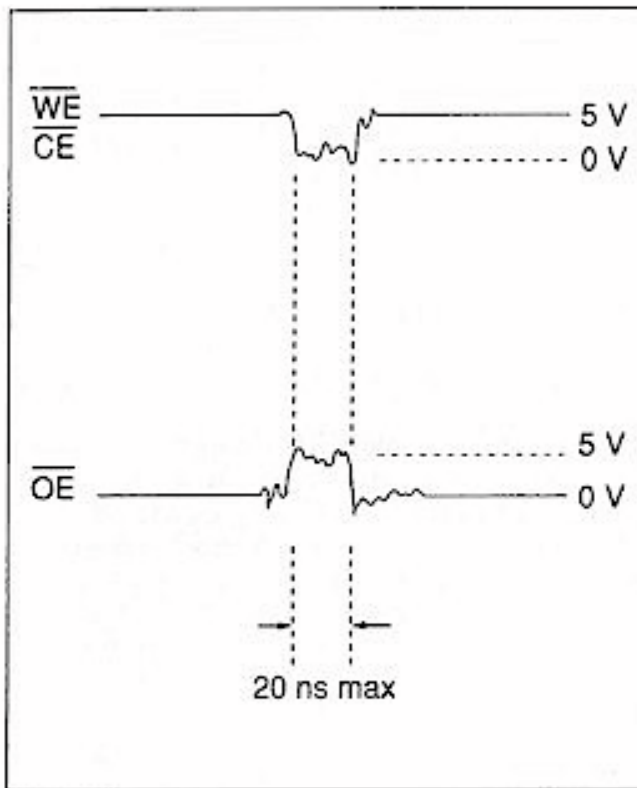
## PROGRAMMING/ERASE

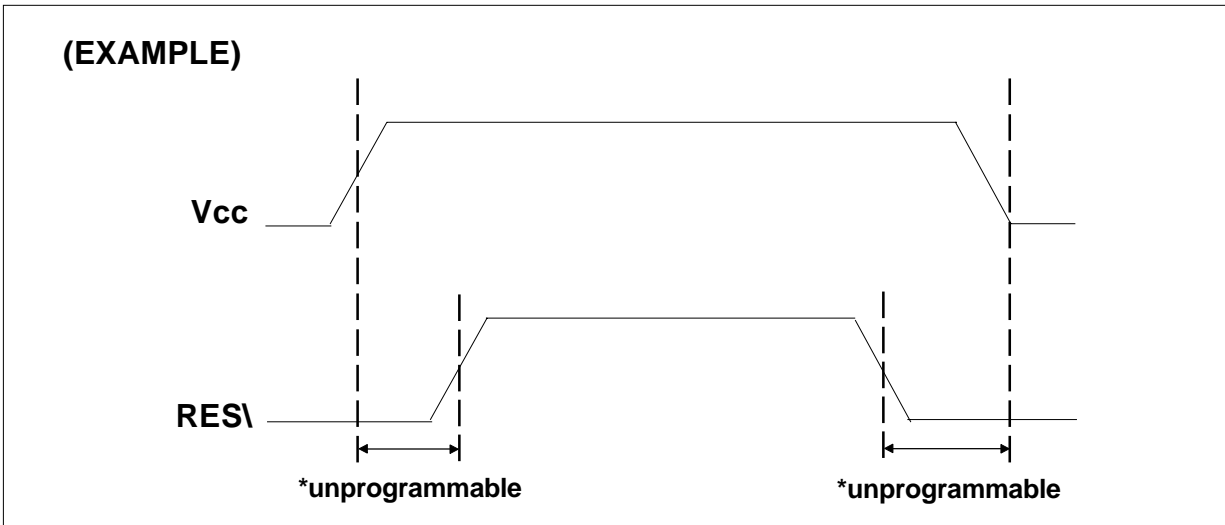
The 58C1001 does **NOT** employ a BULK-erase function. The memory cells can be programmed '0' or '1'. A write cycle performs the function of erase & write on every cycle with the erase being transparent to the user. The internal erase data state is considered to be '1'. To program the memory array with background of ALL 0's or All 1's, the user would program this data using the page mode write operation to program all 1024 128-byte pages.

## DATA PROTECTION

To protect the data during operation and power on/off, the AS58C1001 has:

- 1. Data protection against Noise on Control Pins ( $CE\backslash$ ,  $OE\backslash$ ,  $WE\backslash$ ) during Operation. During readout or standby, noise on the control pins may act as a trigger and turn the EEPROM to programming mode by mistake. To prevent this phenomenon, the AS58C1001 has a noise cancellation function that cuts noise if its width is 20ns or less in programming mode. Be careful not to allow noise of a width of more than 20ns on the control pins.





**FUNCTIONAL DESCRIPTION (continued)**

**DATA PROTECTION (continued)**

2. Data protection at Vcc on/off.

When RES\ is low, the EEPROM cannot be erased and programmed. Therefore, data can be protected by keeping RES\ low when Vcc is switched. RES\ should be high during programming because it does not provide a latch function. When Vcc is turned on or off, noise on the control pins generated by external circuits (CPU, etc.) may turn the EEPROM to programming mode by mistake. To prevent this unintentional programming, the EEPROM must be kept in an unprogrammable, standby or readout state by using a CPU reset signal to RES\ pin.

In addition, when RES\ is kept high at Vcc on/off timing, the input level of control pins (CE\, OE\, WE\ ) must be held as CE\=Vcc or OE\=LOW or WE\=Vcc level.

3. Software Data Protection

To protect against unintentional programming caused by noise generated by external circuits, AS58C1001 has a Software data protection function. To initiate Software data protection mode, 3 bytes of data must be input, followed by a dummy write cycle of any address and any data byte. This exact sequence switches the device into protection mode. This 4th cycle during write is required to initiate the SDP and physically writes the address and data. While in SDP the entire array is protected in which writes can only occur if the exact SDP sequence is re-executed or the unprotect sequence is executed.

**Write Address**      **Write Data**  
**(Normal Data Input)**

5555	AA
↓	↓
2AAA	55
↓	↓
5555	A0

The Software data protection mode can be cancelled by inputting the following 6 Bytes. This changes the AS58C1001 to the Non-Protection mode, for normal operation.

<b>Address</b>	<b>Data</b>
5555	AA
↓	↓
2AAA	55
↓	↓
5555	80
↓	↓
5555	AA
↓	↓
2AAA	55
↓	↓
5555	20



**ABSOLUTE MAXIMUM RATINGS\***

Voltage on Vcc Supply Relative to Vss.....	-0.5V to +7.0V <sup>1</sup>
Voltage on any pin Relative to Vss.....	-0.6V to +7.0V <sup>1</sup>
Storage Temperature .....	-65°C to +150°C
Operating Temperature Range.....	-55°C to +125°C
Soldering Temperature Range.....	260°C
Maximum Junction Temperature**.....	+150°C
Power Dissipation.....	1.0W

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

\*\* Junction temperature depends upon package type, cycle time, loading, ambient temperature and airflow.

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS**

(-55°C ≤ T<sub>A</sub> ≤ 125°C; V<sub>CC</sub> = 5V ±10%)

PARAMETER	CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V <sub>IH</sub>	2.2	V <sub>CC</sub> + 0.3V	V	9
Input Low (Logic 0) Voltage <sup>3</sup>		V <sub>IL</sub>	-0.3	0.8	V	2
Input Voltage (RES\ Pin)		V <sub>H</sub>	V <sub>CC</sub> -0.5	V <sub>CC</sub> +1.0	V	
Input Leakage Current <sup>4</sup>	0V ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>	I <sub>LI</sub>	-2	2	μA	4
Output Leakage Current	Output(s) disabled, 0V ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub>	I <sub>LO</sub>	-2	2	μA	
Output High Voltage	I <sub>OH</sub> = -400 μA	V <sub>OH</sub>	2.4		V	
Output Low Voltage	I <sub>OL</sub> = 2.1 mA	V <sub>OL</sub>		0.4	V	

PARAMETER	CONDITIONS	SYM	MAX			UNITS	NOTES
			-15	-20	-25		
Power Supply Current: Operating	I <sub>OUT</sub> =0mA, V <sub>CC</sub> = 5.5V Cycle=1μS, Duty=100%	I <sub>CC3</sub>	20	20	20	mA	
	I <sub>OUT</sub> =0mA, V <sub>CC</sub> = 5.5V Cycle=MIN, Duty=100%		65	55	50		
Power Supply Current: Standby	CE\=V <sub>CC</sub> , V <sub>CC</sub> = 5.5V	I <sub>CC1</sub>	350	350	350	μA	
	CE\=V <sub>IH</sub> , V <sub>CC</sub> = 5.5V	I <sub>CC2</sub>	3	3	3	mA	

**CAPACITANCE**

PARAMETER	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T <sub>A</sub> = 25°C, f = 1MHz V <sub>IN</sub> = 0	C <sub>IN</sub>	6	pF	
Output Capacitance		C <sub>O</sub>	12	pF	



**AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION**

( $-55^{\circ}\text{C} \leq T_c \leq 125^{\circ}\text{C}$ ;  $V_{cc} = 5V \pm 10\%$ )

Test Conditions

- Input Pulse Levels: 0.0V to 3.0V
- Input rise and fall times:  $\leq 20\text{ns}$
- Output Load: 1 TTL Gate + 100pF (including scope and jig)
- Reference levels for measuring timing: 1.5V, 1.5V

ITEM DESCRIPTION	TEST CONDITION	SYMBOL	-15		-20		-25		UNITS
			MIN	MAX	MIN	MAX	MIN	MAX	
Address Access Time	$CE\backslash=OE\backslash=V_{IL} WE\backslash=V_{IH}$	$t_{ACC}$	---	150	---	200	---	250	ns
Chip Enable Access Time	$OE\backslash=V_{IL} WE\backslash=V_{IH}$	$t_{CE}$	---	150	---	200	---	250	ns
Output Enable Access Time	$CE\backslash=V_{IL} WE\backslash=V_{IH}$	$t_{OE}$	10	75	10	75	10	75	ns
Output Hold to Address Change	$CE\backslash=OE\backslash=V_{IL} WE\backslash=V_{IH}$	$t_{OH}$	0	---	0	---	0	---	ns
Output Disable to High-Z	$CE\backslash=V_{IL} WE\backslash=V_{IH}$	$t_{DF}$	0	50	0	50	0	50	ns
	$CE\backslash=OE\backslash=V_{IL} WE\backslash=V_{IH}$	$t_{DFR}$	0	350	0	350	0	350	ns
RES\ to Output Delay	$CE\backslash=OE\backslash=V_{IL} WE\backslash=V_{IH}$	$t_{RR}$	0	450	0	450	0	450	ns

**AC ELECTRICAL CHARACTERISTICS FOR SOFTWARE DATA PROTECTION CYCLE OPERATION**

PARAMETER	SYMBOL	MIN	MAX	UNITS
Byte Load Cycle Time	$t_{BLC}$	0.55	30	$\mu\text{S}$
Write Cycle Time	$t_{WC}$	10	---	mS

**AC ELECTRICAL CHARACTERISTICS FOR DATA\ POLLING OPERATION**

PARAMETER	SYMBOL	MIN	MAX	UNITS
Output Enable Hold Time	$t_{OE\backslash H}$	0	---	ns
Output Enable to Write Setup Time	$t_{OE\backslash S}$	0	---	ns
Write Start Time	$t_{DW}$	150	---	ns
Write Cycle Time	$t_{WC}$	---	10	ms

**AC ELECTRICAL CHARACTERISTICS FOR PAGE ERASE AND PAGE WRITE OPERATIONS**

PARAMETER	SYMBOL	MIN	MAX	UNITS
Address Setup Time	$t_{AS}$	0	---	ns
Write Enable to Write Setup Time	$t_{WS}^8$	0	---	ns
Chip Enable to Write Setup Time	$t_{CS}^7$	0	---	ns
Write Pulse Width	$t_{WP}^7$	250	---	ns
	$t_{CW}^9$	250	---	ns
Address Hold Time	$t_{AH}$	150	---	ns
Data Setup Time	$t_{DS}$	100	---	ns
Data Hold Time	$t_{DH}$	10	---	ns
Write Enable Hold Time	$t_{WH}^8$	0	---	ns
Chip Enable Hold Time	$t_{CH}^7$	0	---	ns
Out Enable to Write Setup Time	$t_{OES}$	0	---	ns
Output Enable Hold Time	$t_{OEH}$	0	---	ns
Data Latch Time	$t_{DL}$	200	---	ns
Write Cycle Time	$t_{WC}$	10	---	ms
Byte Load Window	$t_{BL}$	100	---	$\mu s$
Byte Load Cycle	$t_{BLC}$	0.55	30	$\mu s$
Time to Device Busy	$t_{DB}$	120	---	ns
RES\ to Write Setup Time	$t_{RP}$	100	---	$\mu s$
Vcc to RES\ Setup Time	$t_{RES}^{11}$	1	---	$\mu s$



**AC ELECTRICAL CHARACTERISTICS FOR BYTE ERASE AND BYTE WRITE OPERATIONS**

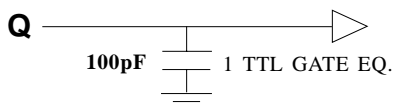
PARAMETER	SYMBOL	MIN	MAX	UNITS
Address Setup Time	$t_{AS}$	0	---	ns
Chip Enable to Write Setup Time	$t_{CS}^7$	0	---	ns
Write Pulse Width	$t_{CW}^8$	250	---	ns
	$t_{WP}^7$	250	---	ns
Address Hold Time	$t_{AH}$	150	---	ns
Data Setup Time	$t_{DS}$	100	---	ns
Data Hold Time	$t_{DH}$	10	---	ns
Chip Enable Hold Time	$t_{CH}^7$	0	---	ns
Out Enable to Write Setup Time	$t_{OES}$	0	---	ns
Output Enable Hold Time	$t_{OEH}$	0	---	ns
Write Cycle Time	$t_{WC}$	10	---	ms
Byte Load Window	$t_{BL}$	100	---	$\mu s$
Time to Device Busy	$t_{DB}$	120	---	ns
RES\ to Write Setup Time	$t_{RP}$	100	---	$\mu s$
Vcc to RES\ Setup Time	$t_{RES}^{10}$	1	---	$\mu s$

**AC TEST CONDITIONS**

Input Pulse Levels.....	0V to 3V
Input Rise and Fall Times.....	$\leq 20ns$
Input Timing Reference Level.....	1.5V
Output Reference Level.....	1.5V
Output Load.....	See Figure 1

**NOTES:**

1. Relative to V<sub>SS</sub>
2. V<sub>IN</sub> min = -3.0V for pulse widths  $\leq 50ns$
3. V<sub>IL</sub> min = -1.0V for pulse widths  $\leq 50ns$
4. I<sub>IL</sub> on RES\ = 100ua MAX
5. t<sub>OF</sub> is defined as the time at which E the output becomes and open circuit and data is no longer driven.
6. Use this device in longer cycle than this value
7. WE\ controlled operation
8. CE\ controlled operation
9. RES\ pin V<sub>IH</sub> is V<sub>H</sub>
10. Reference only, not tested

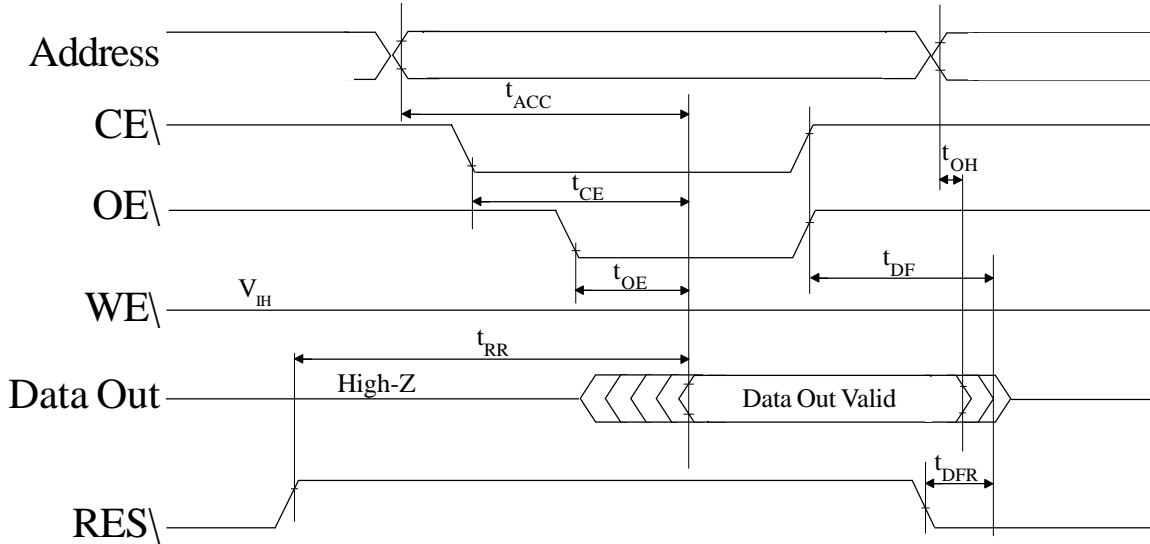


**Figure 1**  
**OUTPUT LOAD EQUIVALENT**

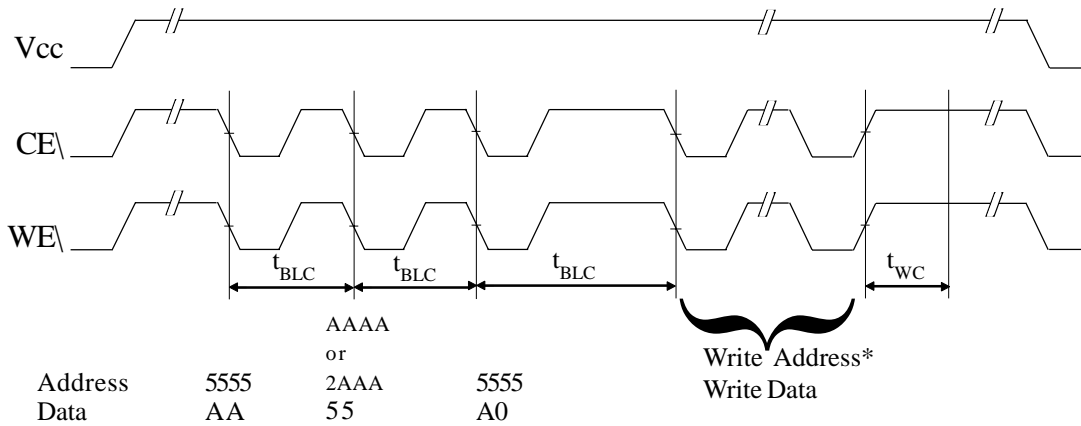




**READ TIMING WAVEFORM**

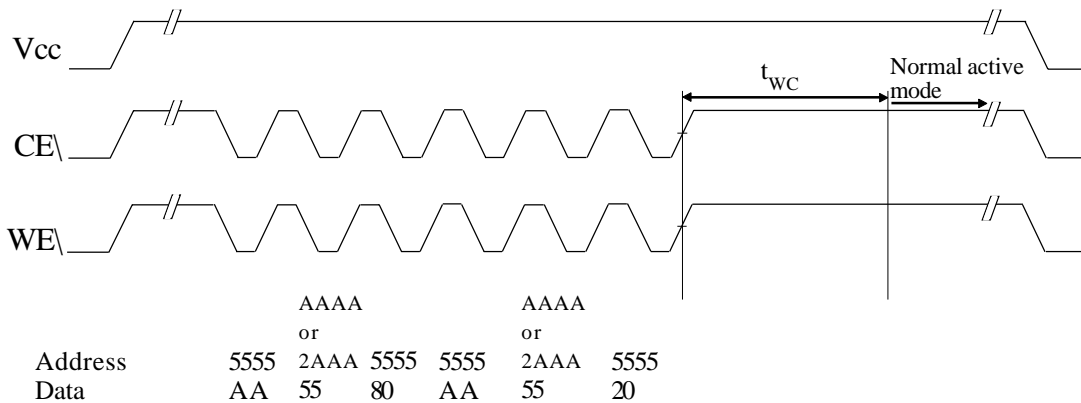


**SOFTWARE DATA PROTECTION TIMING WAVEFORM (protection mode)**



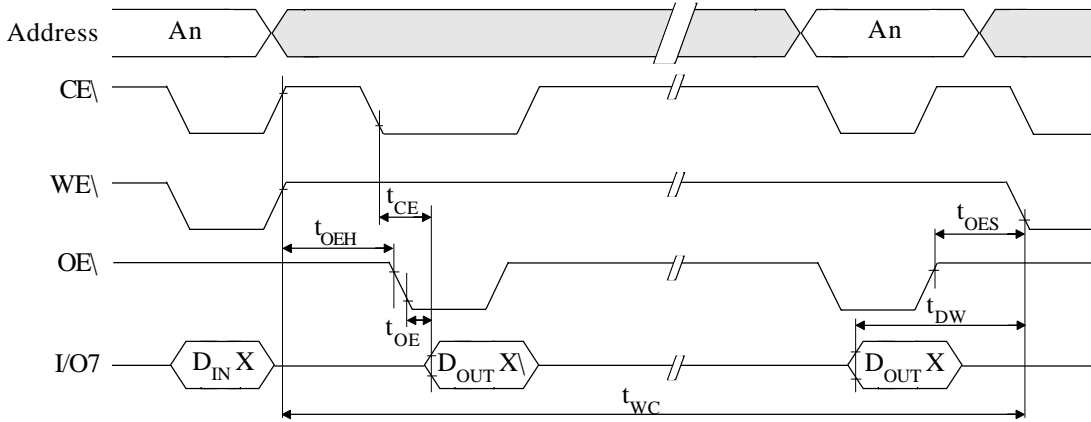
\* During this write cycle, data is physically written to address provided.

**SOFTWARE DATA PROTECTION TIMING WAVEFORM (non-protection mode)**

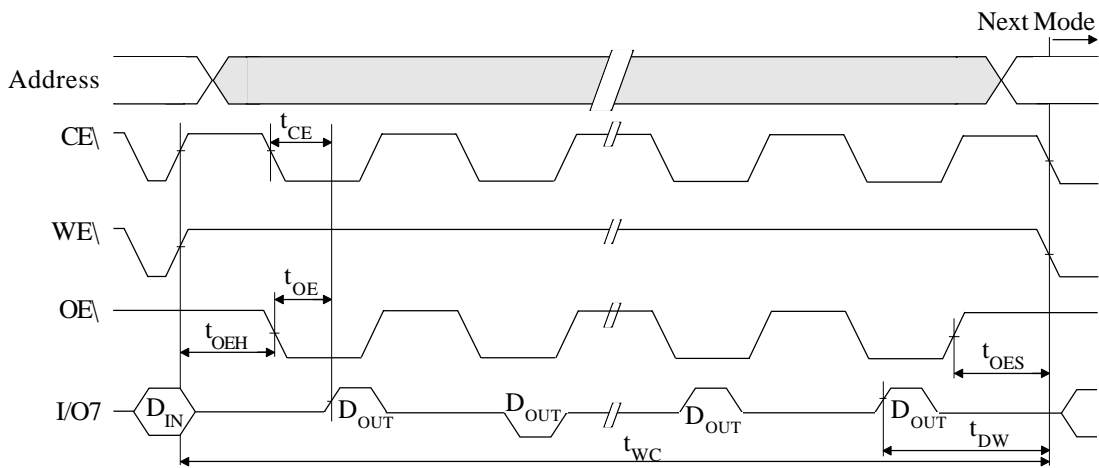




### DATA\ POLLING TIMING WAVEFORM



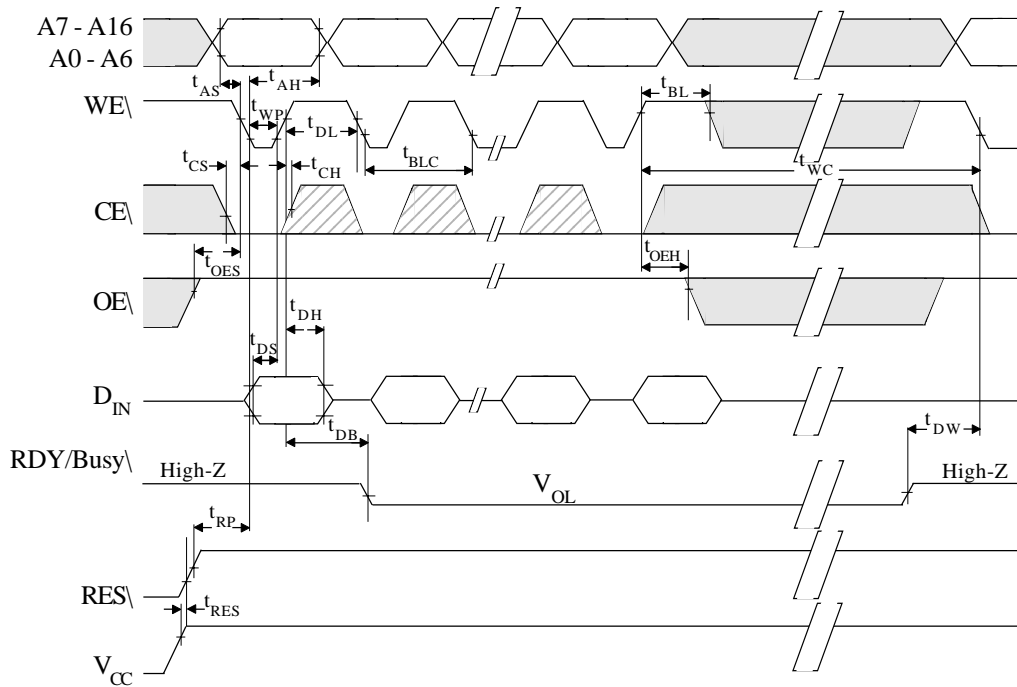
### TOGGLE BIT WAVEFORM



 In transition from HI to LOW or LOW to HI.



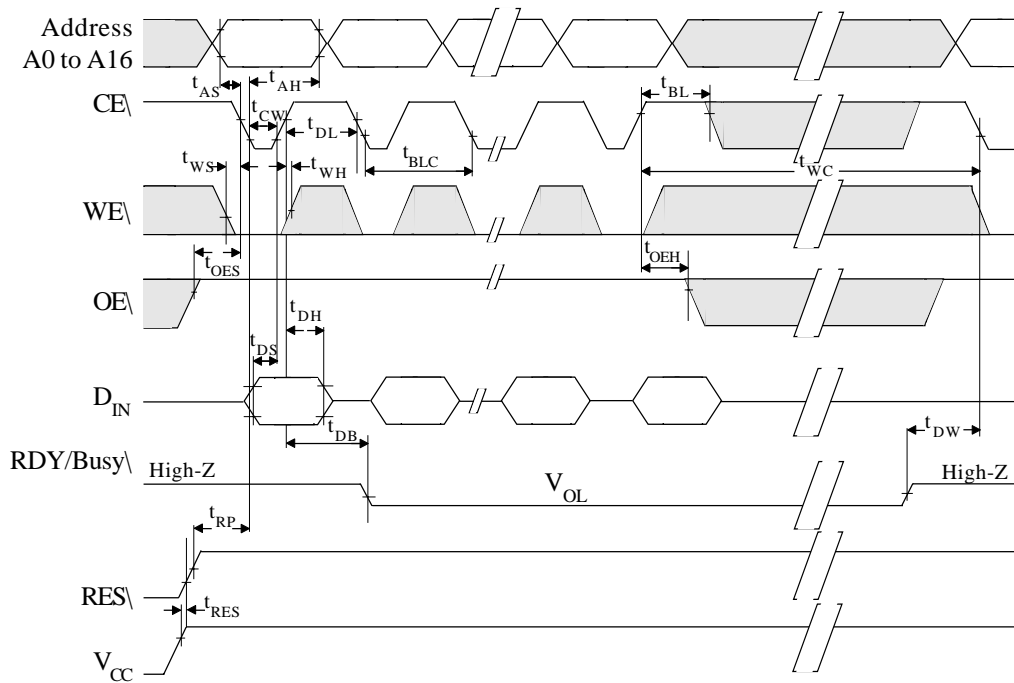
### PAGE WRITE TIMING WAVEFORM (WE\ CONTROLLED)



 In transition from HI to LOW or LOW to HI.



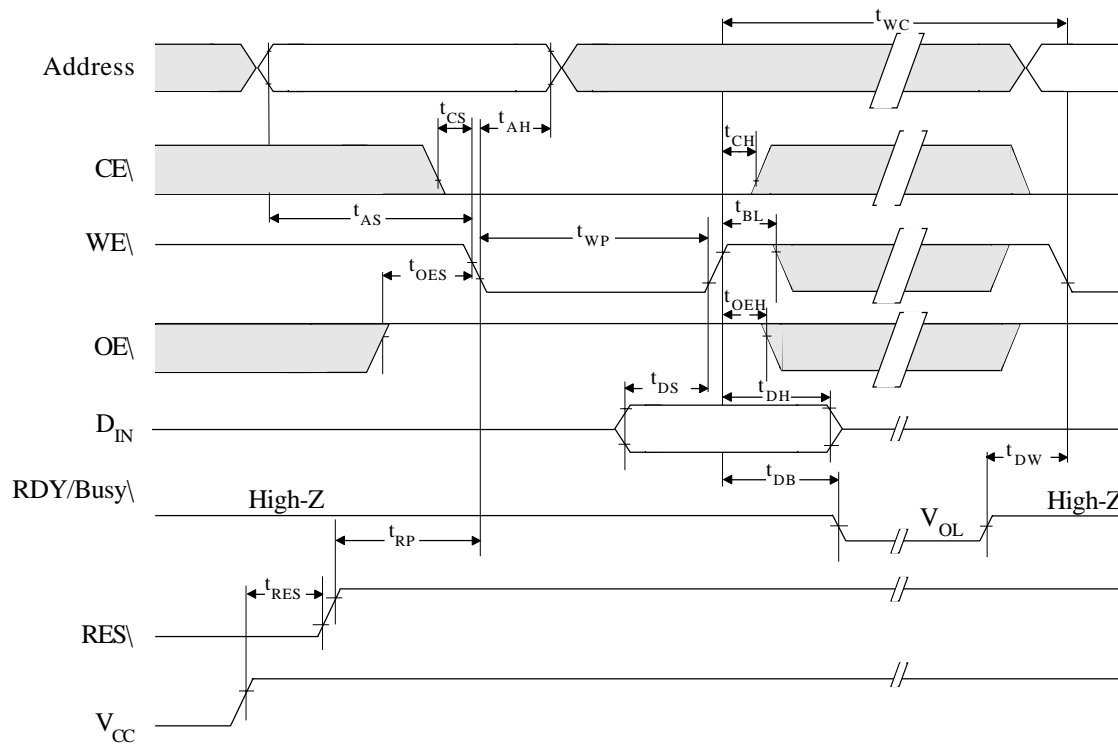
### PAGE WRITE TIMING WAVEFORM (CE\ CONTROLLED)




 In transition from HI to LOW or LOW to HI.



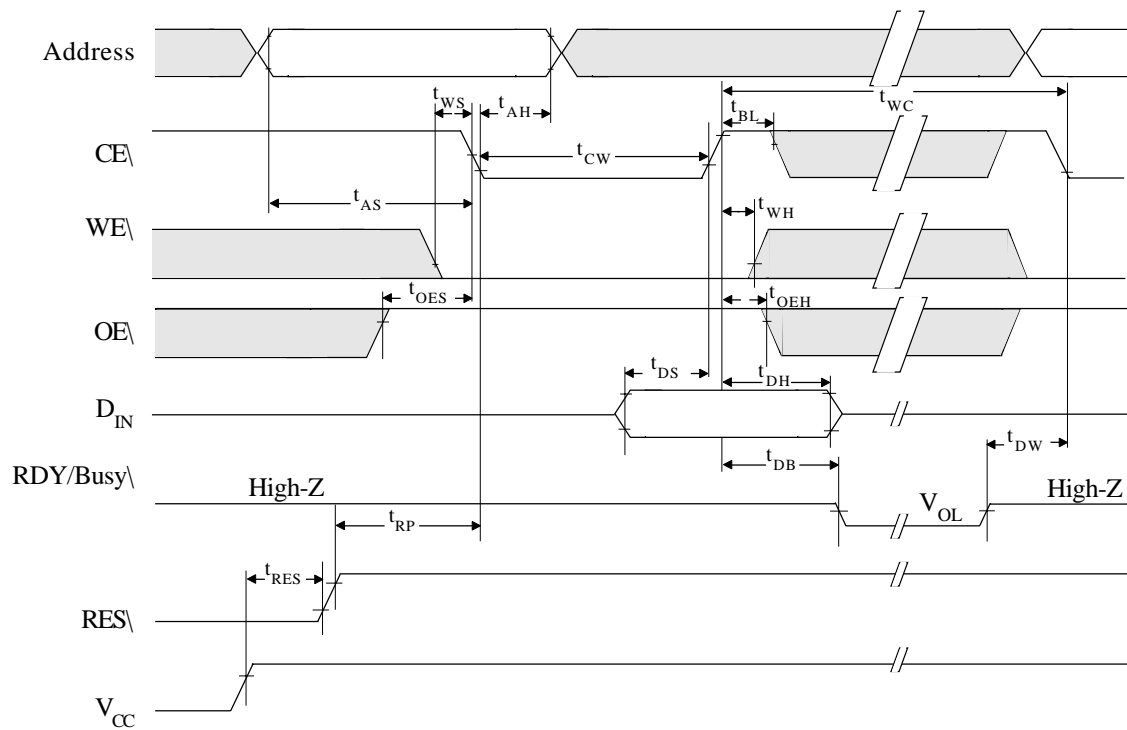
### BYTE WRITE TIMING WAVEFORM (WE\ CONTROLLED)



 In transition from HI to LOW or LOW to HI.



### BYTE WRITE TIMING WAVEFORM (CE\ CONTROLLED)

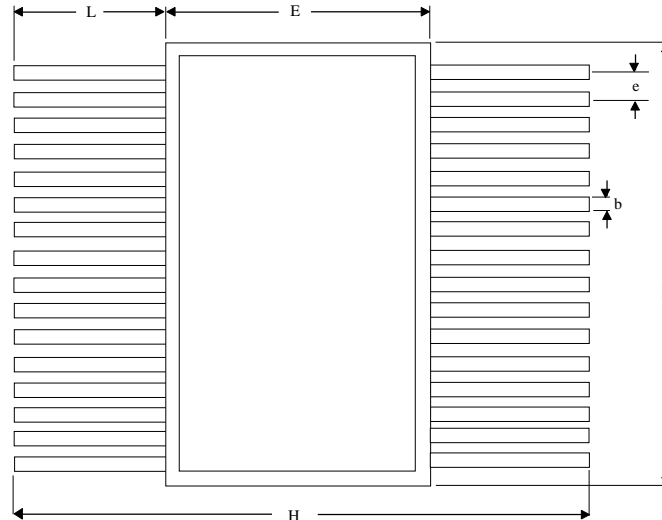


 In transition from HI to LOW or LOW to HI.

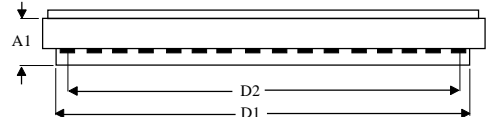


**MECHANICAL DEFINITIONS\***

ASI Case #305 (Package Designator SF)  
SMD 5962-38267, Case Outline N



**Top View**



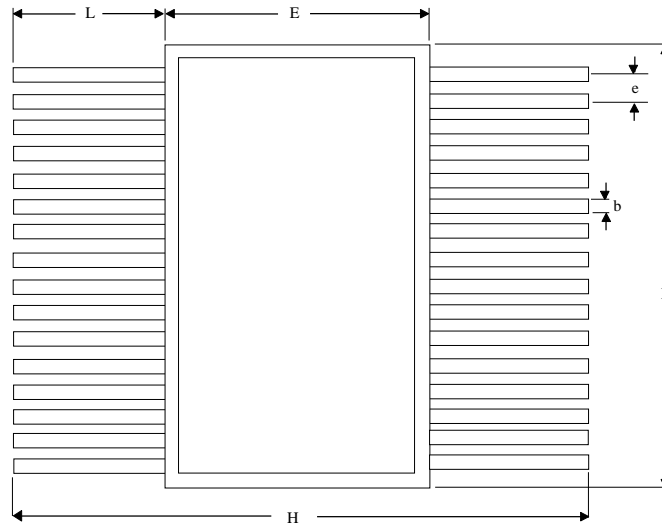
SYMBOL	SMD SPECIFICATIONS	
	MIN	MAX
A	0.125	0.150
A1	0.090	0.110
b	0.015	0.019
c	0.003	0.007
D	0.810	0.830
D1	0.775	0.785
D2	0.745	0.755
E	0.425	0.445
E1	0.290	0.310
e	0.045	0.055
H	1.000	1.100
L	0.290	0.310
Q	0.026	0.037

\*All measurements are in inches.

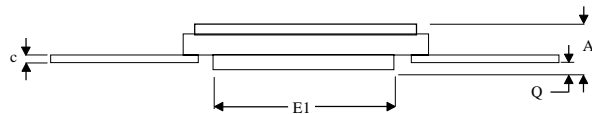
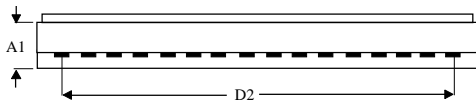


**MECHANICAL DEFINITIONS\***

**ASI Case #306 (Package Designator F)**  
**SMD 5962-38267, Case Outline M**



**Top View**



SYMBOL	SMD SPECIFICATIONS	
	MIN	MAX
A	0.097	0.123
A1	0.090	0.110
b	0.015	0.019
c	0.003	0.007
D	0.810	0.830
D2	0.745	0.755
E	0.425	0.445
E1	0.330	0.356
e	0.045	0.055
H	1.000	1.100
L	0.290	0.310
Q	0.026	0.037

**NOTE:** All drawings are per the SMD. ASI's package dimensional limits may differ, but they will be within the SMD limits.

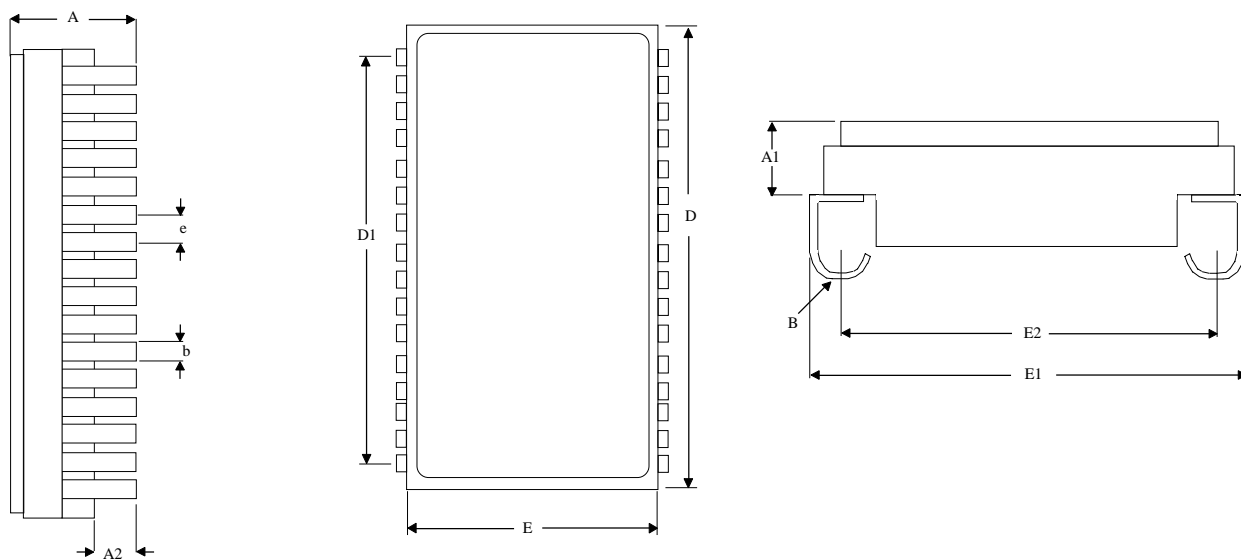
\*All measurements are in inches.





### MECHANICAL DEFINITIONS\*

ASI Case #508 (Package Designator DCJ)



SYMBOL	ASI PACKAGE SPECIFICATIONS	
	MIN	MAX
A	0.132	0.142
A1	0.076	0.086
A2	0.018	0.028
B	0.018	0.032
b	0.015	0.019
D	0.816	0.834
D1	0.745	0.755
E	0.430	0.440
E1	0.465	0.485
E2	0.415	0.425
e	0.045	0.055

\*All measurements are in inches.



## ORDERING INFORMATION

**EXAMPLE:** AS58C1001F-25/XT

Device Number	Package Type	Speed ns	Process
AS58C1001	F	-15	/*
AS58C1001	F	-20	/*
AS58C1001	F	-25	/*

**EXAMPLE:** AS58C1001SF-15/IT

Device Number	Package Type	Speed ns	Process
AS58C1001	SF	-15	/*
AS58C1001	SF	-20	/*
AS58C1001	SF	-25	/*

**EXAMPLE:** AS58C1001DCJ-20/IT

Device Number	Package Type	Speed ns	Process
AS58C1001	DCJ	-15	/*
AS58C1001	DCJ	-20	/*
AS58C1001	DCJ	-25	/*

### **\*AVAILABLE PROCESSES**

IT = Industrial Temperature Range      -40°C to +85°C  
 XT = Extended Temperature Range      -55°C to +125°C  
 883C = Full Military Processing      -55°C to +125°C



**ASI TO DSCC PART NUMBER  
CROSS REFERENCE\***

**Package Designator F**

<u>ASI Part #</u>	<u>SMD Part#</u>
AS58C1001F-25/883C	5962-3826716QMA
AS58C1001F-20/883C	5962-3826717QMA
AS58C1001F-15/883C	5962-3826718QMA

**Package Designator SF**

<u>ASI Part #</u>	<u>SMD Part#</u>
AS58C1001SF-25/883C	5962-3826716QNA
AS58C1001SF-20/883C	5962-3826717QNA
AS58C1001SF-15/883C	5962-3826718QNA

*Package Designator DCJ not currently available  
on the SMD.*

\* ASI part number is for reference only. Orders received referencing the SMD part number will be processed per the SMD.