# EEPROM

## AVAILABLE AS MILITARY SPECIFICATIONS

- SMD 5962-94614: AS8E32K32
- MIL-STD-883

## FEATURES

- Access times of 90, 120, 150 ns
- Built in decoupling caps for low noise operation
- Organized as 32K x 32; User configurable as 64K x 16 or 128K x 8
- Operation with single 5 volt supply
- Low power CMOS
- TTL Compatible Inputs and Outputs

## OPTIONS MARKINGS

- Timing

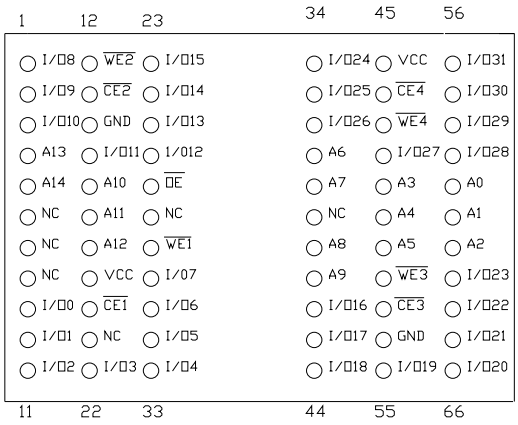
| | |
|---|---|
| 90 ns | -9 |
| 120 ns | -12 |
| 150 ns | -15 |

- Package

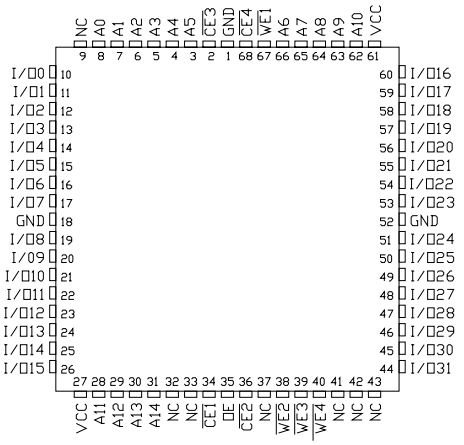
| | | |
|---|---|---|
| Ceramic Quad Flatpack | Q | No. 705 |
| Pin Grid Array | P | No. 805 |

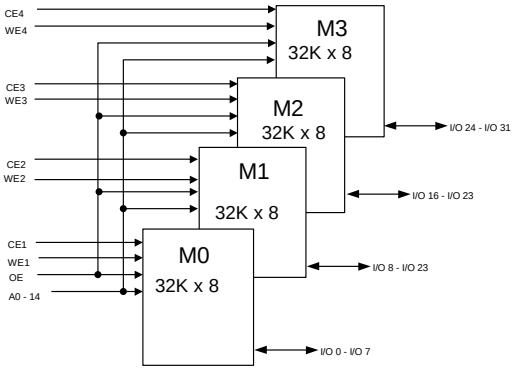
## PIN ASSIGNMENT (Top View)

66 Lead PGA




68 Lead CQFP




## GENERAL DESCRIPTION

The Austin Semiconductor, Inc. AS8E32K32 is a 1 Megabit EEPROM Modules organized as 32K x 32 bit. User configurable to 64K x16 or 128Kx 8. The module achieves high speed access, low power consumption and high reliability by employing advanced CMOS memory technology.

The military grade product is manufactured in compliance to the SMD and MIL-STD 883, making the AS8E32K32 ideally suited for military or space applications.

The module is offered in a 1.090 sq inch ceramic pin grid array substrate. This package design provides the optimum space saving solution for boards that accept through hole packaging.

The module is also offered as a 68 lead 0.990 sq. inch ceramic quad flatpack. It has a max. height of 0.200 inch. This package design is targeted for those applications which require low profile SMT Packaging.

### DEVICE IDENTIFICATION

An extra 64 bytes of EEPROM memory is available on each die for user identification. By raising A9 to 12 V +/- 0.5V and using address locations 7FC0H to 7FFFH the bytes may be written to or read from in the same manner as the regular memory array.

## DEVICE OPERATION

The 32Kx 32 EEPROM memory soultion is an electricaly erasable and programmable memory module that is accessed like a Static RAM for the read or write cycle without the need for external components. The device contains a 64-byte-page register to allow writing of up to 64 bytes of data simultaneously. During a write cycle, the address and 1 to 64 bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by DATA polling of I/O7. Once the end of a write cycle has been detected a new access for a read or write can begin.

## READ

The memory module is accessed like a Static RAM. When CE\ and OE\ are low and WE\ is High, the data stored at the memory location determined by the address pins is asserted on the outputs. The module can be read as a 32 bit, 16 bit or 8 bit device. The outputs are put in the high impedance state when either CE\ or OE\ is high. This dual-line control gives designers flexibility in preventing bus contention in their system.

## BYTE WRITE

A low pulse on the WE\ or CE\ input with CE\ or WE\ low (respectively) and OE\ high initiates a write cycle. The address is latched on the falling edge of CE\ or WE\, whichever occurs last. The data is latched by the first rising edge of CE\ or WE\. Once a BWDW (byte, word or double word) write has been started it will automatically time itself to completion.

## PAGE WRITE

The page write operation of the 32K x 32 EEPROM allows 1 to 64 BWDWs of data to be written into the device during a single internal programming period. Each new BWDW must be written within 150-µs (tBLC) of the previous BWDW. If the tBLC limit is exceeded the device will cease accepting data and commence the internal programming operation. For each WE high to low transition during the page write operation, A6-A14 must be the same.

The A0-A5 inputs are used to specify which bytes within the page are to be written. The bytes may be loaded in any order and may be altered within the same load period. Only bytes which are specified for writing will be written; unnecessary cycling of other bytes within the page does not occur.

## DATA POLLING

this memory module features DATA Polling to indicate the end of a write cycle. During a byte or page write cycle an attempted read of the last byte written will result in the complement of the written data to be presented on I/O7. Once the write cycle has been completed, true data is valid on all outputs, and the next write cycle may begin. DATA Polling may begin at anytime during the write cycle.

## TOGGLE BIT

In addition to DATA Polling the module provides another method for determining the end of a write cycle. During the write operation, successive attempts to read data from the device will result in I/O6 of the accessed die toggling between one and zero. Once the write has completed, I/O6 will stop toggling and valid data will be read. Reading the toggle bit may begin at any time during the write cycle.

## DATA PROTECTION

If precautions are not taken, inadvertent writes may occur during transitions of the host power supply. The $E^2$ module has incorporated both hardware and software features that will protect the memory against inadvertent writes.

## HARDWARE PROTECTION

Hardware features protect against inadvertent writes to the module in the following ways: (a) VCC sense - if VCC is below 3.8 V (typical) the write function is inhibited; (b) VCC power-on delay - once VCC has reached 3.8 V the device will automatically time out 5 ms (typical) before allowing a write; (c) write inhibit - holding any one of OE\ low, CE\ high or WE\ high inhibits write cycles; (d) noise filter - pulses of less than 15 ns (typical) on the WE\ or CE\ inputs will not initiate a write cycle.

## SOFTWARE DATA PROTECTION

A software controlled data protection feature has been implemented on the memory module. When enabled, the software data protection (SDP), will prevent inadvertent writes. The SDP feature may be enabled or disabled by the user and is shipped with SDP disabled.

SDP is enabled by the host system issuing a series of thre e write commands; three specific bytes of data are written to three specific addresses (refer to Software Data Protection Algorithm). After writing the three byte command sequence and after tWC the entire module will be protected from inadvertent write operations. It should be noted, that once protected the host may still perform a byte of page write to the module. This is done by preceding the data to be written by the same three byte command sequence used to enable SDP.

Once set, SDP will remain active unless the disable command sequence is issued. Power transitions do not disable SDP and SDP will protect the 32K x 32 EEPROM module during power-up and Power-down conditions. All command sequences must conform to the page write timing specifications. The data in the enable and disable command sequences is not written to the device and the memory addresses used in the sequence may be written with data in either a byte of page write operation.

After setting SDP, any attempt to write to the device without the three byte command sequence will start the internal write timers. No data will be written to the device; however, for the duration of tWC, read operations will effectively be polling operations.

**ABSOLUTE MAXIMUM RATINGS***

Voltage on Vcc Supply Relative to Vss
Vcc .....-.6V to +6.5V
Storage Temperature .....-65°C to +150°C
Short Circuit Output Current (per I/O)….....20mA
Voltage on any Pin Relative to Vss.....-.5V to Vcc+1 mA
Junction Temperature**.....+150°C
Thermal Resistance junction to case ($\theta_{JC}$):
Package Type Q.....11.3° C/W
Package Type P.....2.8° C/W

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
** Maximum junction temperature depends upon package type, cycle time, loading, ambient temperature and airflow, and humidity.

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($-55°C \le T_A \le 125°C$; $V_{CC}$ = 5V ±10%)

| DESCRIPTION | CONDITIONS | SYMBOL | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Input High (Logic 1) Voltage | | $V_{IH}$ | 2 | $V_{CC}$+.3 | V | 1 |
| Input Low (Logic 0) Voltage | | $V_{IL}$ | -0.5 | 0.8 | V | 1, 2 |
| Input Leakage Current | $0V \le V_{IN} \le V_{CC}$ | $I_{LI}$ | -10 | 10 | µA | |
| Input Leakage Current $_{WE\backslash, CE\backslash}$ | | | -10 | 10 | µA | |
| Output Leakage Current | Output(s) disabled $0V \le V_{OUT} \le V_{CC}$ | $I_{LO}$ | -10 | 10 | µA | |
| Output High Voltage | $I_{OH}$ = -.4 mA | $V_{OH}$ | 2.4 | | V | 1 |
| Output Low Voltage | $I_{OL}$ = 2.1mA | $V_{OL}$ | | 0.45 | V | 1 |
| Supply Voltage | | $V_{CC}$ | 4.5 | 5.5 | V | 1 |

| | | | MAX | | | | |
|---|---|---|---|---|---|---|---|
| DESCRIPTION | CONDITIONS | SYMBOL | -90 | -120 | -150 | UNITS | NOTES |
| Power Supply Current: Operating | $CE\backslash \le V_{IL}$; $V_{CC}$ = MAX f = 5 MHz OUTPUTS OPEN | $I_{CC}$ | 340 | 340 | 340 | mA | |
| Power Supply Current: Standby | $CE\backslash \ge V_{IH}$; All Other Inputs $\le V_{IL}$ or $\ge V_{IH}$; $V_{CC}$ = MAX f = 5 MHz | $I_{SBT1}$ | 12 | 12 | 12 | mA | |
| | $CE\backslash \ge V_{CC}$ -0.2V; $V_{CC}$ = MAX $V_{IL} \le V_{SS}$ +0.2V or $V_{IH} \ge V_{CC}$ -0.2V; f = 0 Hz | $I_{SBC1}$ | 1.3 | 1.3 | 1.3 | mA | |

## CAPACITANCE TABLE (1)

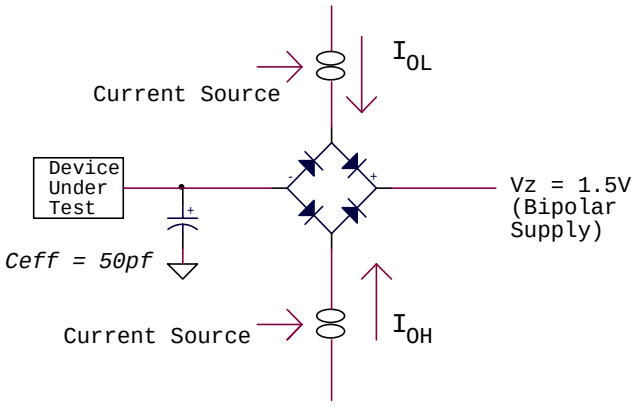
$V_{IN}$ = 0V, f = 1MHz, TA =25ºC

| Symbol | Parameter | Maximum | Units | Notes |
|---|---|---|---|---|
| $C_{ADD}$ | A0-A14 Capactiance | 24 | pF | 4, 14 |
| $C_{OE}$ | OE\ Capactiance | 24 | pF | 4, 14 |
| $C_{WE}$, $C_{CE}$ | WE\ and CE\ Capactiance | 6 | pF | 4, 14 |
| $C_{IO}$ | I/O 0 - I/O 31 Capactiance | 12 | pF | 4, 14 |

1. This parameter is guaranteed but not tesed

| TRUTH TABLE | | | | |
|---|---|---|---|---|
| **MODE** | **CE** | **OE** | **WE** | **I/O** |
| Read | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | $D_{OUT}$ |
| Write (2) | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | $D_{IN}$ |
| Standby/Write | $V_{IH}$ | X (1) | X | High Z |
| Write Inhibit | X | X | $V_{IH}$ | |
| Write Inhibit | X | $V_{IL}$ | X | |
| Output Disable | X | $V_{IH}$ | X | High Z |

## AC TEST CONDITIONS




**Test Specifications**

Input pulse levels.....VSS to 3V
Input rise and fall times.....5ns
Input timing reference levels.....1.5V
Output reference levels.....1.5V
Output load.....See Figures 1 and 2

**Notes:**

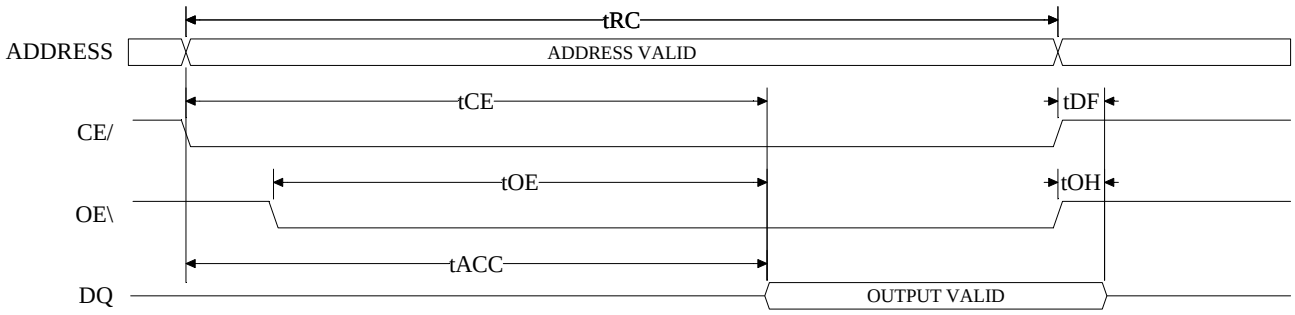
Vz is programable from -2V to + 7V.
$I_{OL}$ and $I_{OH}$ programmable from 0 to 16 mA.
Vz is typically the midpoint of $V_{OH}$ and $V_{OL}$.
$I_{OL}$ and $I_{OH}$ are adjusted to simulate a typical resistive load circuit.

## AC READ CHARACTERISTICS

(-55°C ≤ $T_A$ ≤ 125°C; $V_{CC}$ = 5V ±10%)

| | | -90 | | -120 | | -150 | | |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | **Units** |
| $t_{RC}$ | Read Cycle Time | 90 | | 120 | | 150 | | ns |
| $t_{ACC}$ | Address to Output Delay | | 90 | | 120 | | 150 | ns |
| $t_{ACS}$ | CE\ Access Time | | 90 | | 120 | | 150 | ns |
| $t_{CE}$ (1) | CE\ to Output Delay | | 90 | | 120 | | 150 | ns |
| $t_{OE}$ (2) | OE\ to Output Delay | | 50 | | 60 | | 70 | ns |
| $t_{DF}$ (3,4) | CE\ or OE\ to Output High-Z | | 50 | | 60 | | 70 | ns |
| $t_{OH}$ | Output Hold from OE\, CE\ or Address, whichever occurs first | 0 | | 0 | | 0 | | ns |

## A.C. Read Waveforms(1,2,3)




**Notes:**

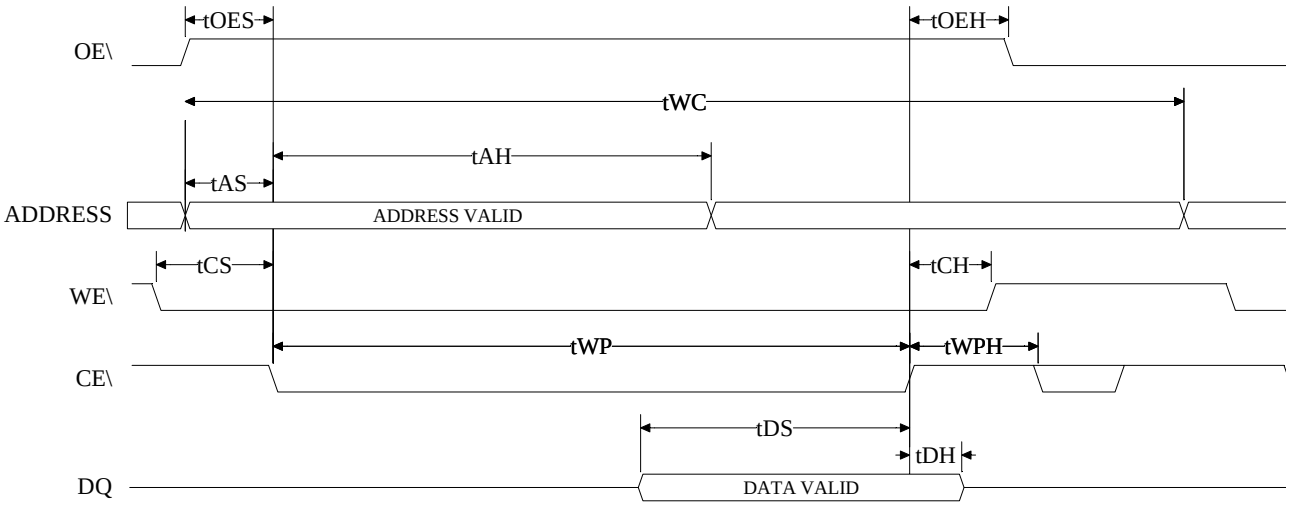
1. CE\ may be delayed to $t_{ACC}$-$t_{CE}$ after the address transition without inpact on $t_{ACC}$.
2. OE\ may be delayed to $t_{CE}$-$t_{OE}$ after the falling edge of CE\ without inpact on $t_{CE}$ or by $t_{ACC}$-$t_{OE}$ after an address change without inpact on $t_{ACC}$.
3. $t_{DF}$ is specified from OE\ or CE\ whichever occurs first ($C_L$ = 5pF).

## AC WRITE CHARACTERISTICS

(-55°C ≤ $T_A$ ≤ 125°C; $V_{CC}$ = 5V ±10%)

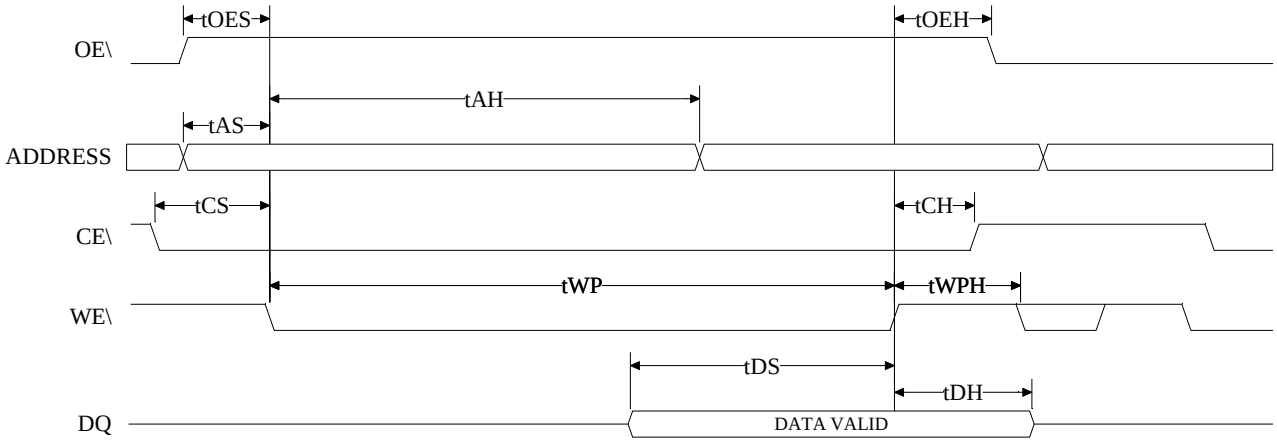
| | | -90 | | -120 | | -150 | | |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| $t_{wc}$ | Write Cycle Time | | 10 | | 10 | | 10 | ms |
| $t_{AS}$ | Address, OE\ Set-Up time | 0 | | 0 | | 0 | | ns |
| $t_{AH}$ | Address, Hold time | 50 | | 50 | | 50 | | ns |
| $t_{CS}$ | Chip Select Set-up Time | 0 | | 0 | | 0 | | ns |
| $t_{CH}$ | Chip Select Hold Time | 0 | | 0 | | 0 | | ns |
| $t_{WP}$ | Write Pulse Width (WE\ or CE\) | 100 | | 100 | | 100 | | ns |
| $t_{DS}$ | Data Set-up Time | 50 | | 50 | | 50 | | ns |
| $t_{DH}$ | Data Hold Time | 0 | | 0 | | 0 | | ns |
| $t_{OEH}$ | OE\ Hold time | 0 | | 0 | | 0 | | ns |
| $t_{OES}$ | OE\ Set-up time | 0 | | 0 | | 0 | | ns |
| $t_{WPH}$ | Write Pulse Width High | 50 | | 50 | | 50 | | ns |

**WRITE CYCLE NO 1.**
(Chip Enable Controlled)



## WRITE CYCLE NO 2.

(Write Enable Controlled)

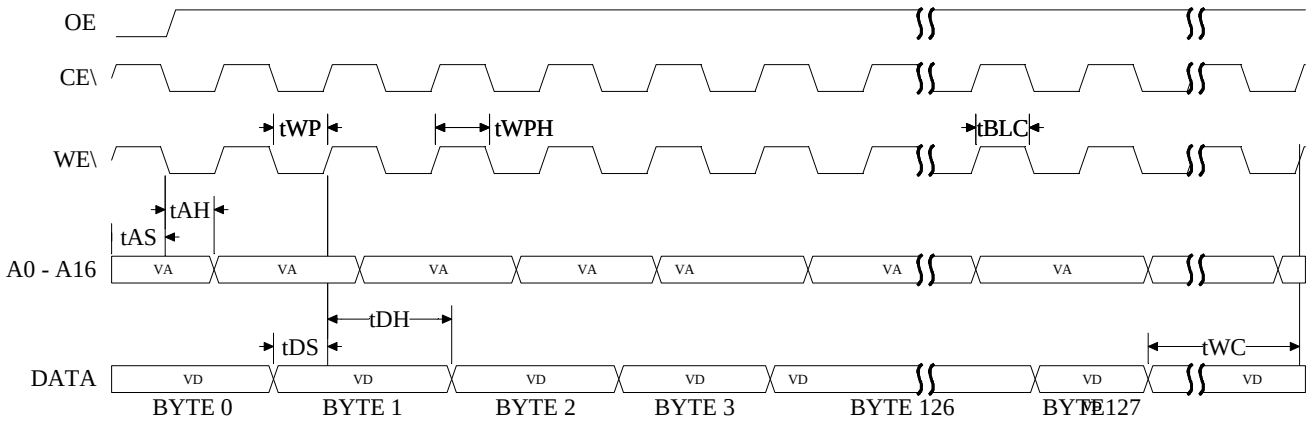


## PAGE MODE CHARACTERISTICS

(-55°C ≤ $T_A$ ≤ 125°C; $V_{CC}$ = 5V ±10%)

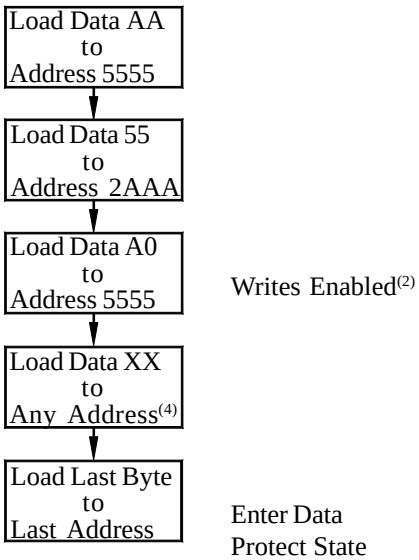
| | | -90 | | -120 | | -150 | | |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| $t_{wc}$ | Write Cycle Time | | 0 | | 0 | | 0 | ms |
| $t_{WP}$ | Write Pulse Width (WE\ or CE\) | 100 | | 100 | | 100 | | ns |
| $t_{DS}$ | Data Set-up Time | 50 | | 50 | | 50 | | ns |
| $t_{DH}$ | Data Hold Time | 0 | | 0 | | 0 | | ns |
| $t_{BLC}$ | Byte Load Cycle Time | | 150 | | 150 | | 150 | µs |
| $t_{WPH}$ | Write Pulse Width High | 50 | | 50 | | 50 | | ns |

## Page Mode Write Waveforms(1,2)

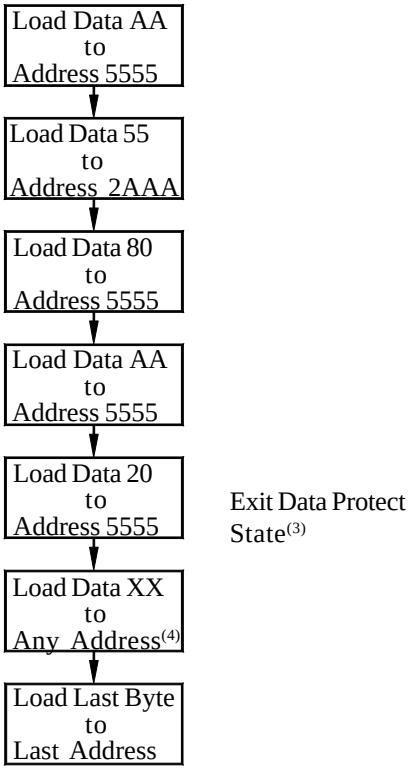



**Notes:** 1. A7 through A16 must specify the page address during each high to low transition of WE\ (or CE\).
2. OE\ must be high only when WE\ and CE\ are both low.
3. VD - Valid Data
4. VA - Valid Address

## Software Data Protection Enable Algorithm[1]




## Software Data Protection Disable Algorithm[1]




**Notes:**

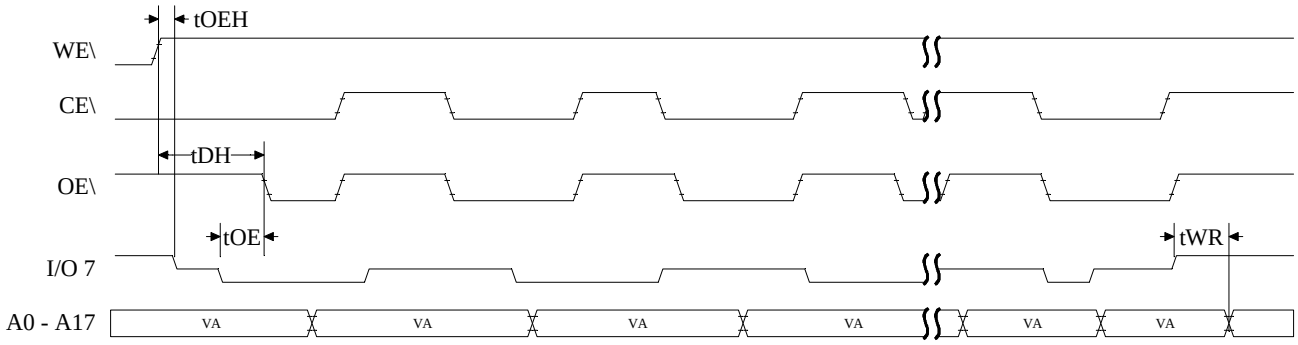
1. Data Format: I/O 7 - I/O 0, I/O 15 - I/O 8, I/O 23 - I/O 16, and I/O 31 - I/O 24, (Hex)
2. Write Protect state will be active at end of write even if no other data is loaded.
3. Write Protect state will be deactivated at end of period even if no other data is loaded.
4. 1 to 64 bytes of data are loaded.
5. A0-A12 of the selected I/O bytes must conform to the addressing sequence for the first three bytes as shown above.
6. After the command sequence has been issued and a page write operation follows, the page address inputs (A5-A14) of the selected I/O bytes must be the same for each high to low transition of WE\ (or CE\).
7. OE Must be high only when WE\ and CE\ are both low.

## Data Polling Characteristics[1]

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $t_{DH}$ | Data Hold Time | 10 | | ns |
| $t_{OEH}$ | OE\ Hold Time | 10 | | ns |
| $t_{OE}$ | OE\ to Output Delay [2] | | 100 | ns |
| $t_{WR}$ | Write Recovery Time | 0 | | ns |

**Notes**: 1. These parameters are characterized and not 100% tested.
2. See A.C. Read Characteristics.

## Data Polling Waveforms

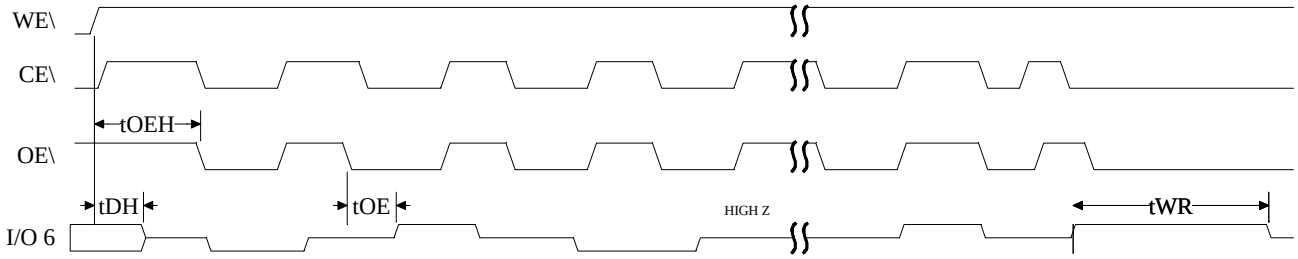



## Toggle Bit Characteristics[1]

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $t_{DH}$ | Data Hold Time | 10 | | ns |
| $t_{OEH}$ | OE\ Hold Time | 10 | | ns |
| $t_{OE}$ | OE\ to Output Delay[2] | | 100 | ns |
| $t_{OEPH}$ | OE\ High Pulse | 150 | | ns |
| $I_{CC}$ | Write Recovery Time | 0 | | ns |

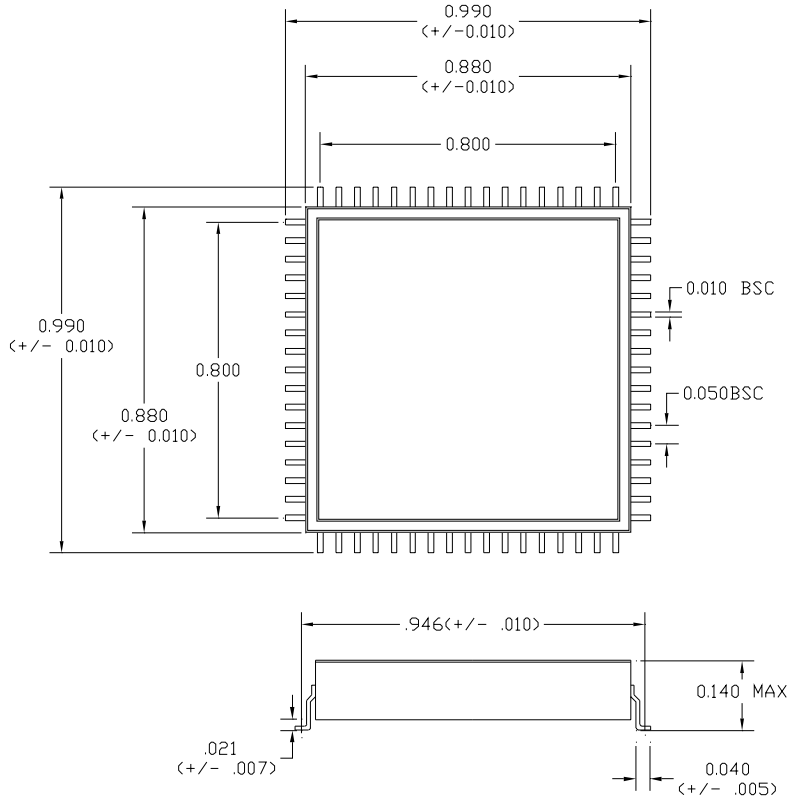
**Notes**: 1. These parameters are characterized and not 100% tested.
2. See A.C. Read Characteristics.

## Toggle Bit Waveforms[1,2,3]




**Notes:** 1. Toggling either OE or CE or Both OE and CE will operate toggle bit.
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

# MECHANICAL DEFINITION
# AS8E32K32
# (ASI Case #705, Package Designator Q)



# MECHANICAL DEFINITION
# AS8E32K32
# (ASI Case #805, Package Designator P)