Austin Semiconductor, Inc.

EEPROM
AS8E512K8

512K x 8 EEPROM
EEPROM Module

AVAILABLE AS MILITARY SPECIFICATIONS
- SMD 5962-93091
- MIL-STD-883

FEATURES
- Access times of 150, 200, 250, and 300 ns
- JEDEC Compatible Pinout
- 10,000 Write Endurance Cycles
- 10 year Data Retention
- Organized as 512Kx8
- Operation with single 5 volt supply
- Low power CMOS
- TTL Compatible Inputs and Outputs

OPTIONS — MARKING

- Packaging

32 pin 600 MIL DIP	CW	No. 112

- Timing

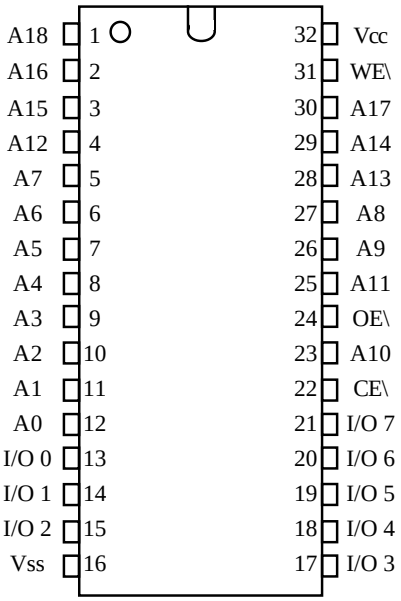
150ns	-150
200ns	-200
250ns	-250
300ns	-300

- Operating Temperature Range

-Military (-55°C to +125°C)	XT
-Industrial (-40°C to +85°C)	IT

PIN ASSIGNMENT
(Top View)

32-Pin DIP & 32-Pin SOJ (CW)

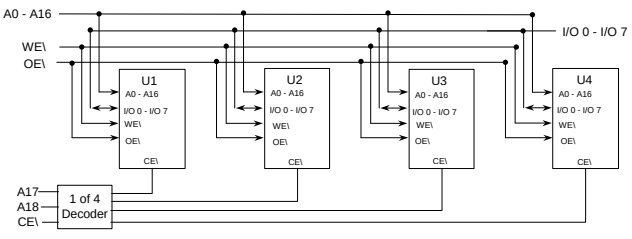


PIN DESCRIPTION	
A0 - A18	Address Inputs
I/O 0 - I/O 7	Data Inputs/Outputs
CE\	Chip Select
OE\	Output Enable
WE\	Write Enable
Vcc	+5.0V Power

GENERAL DESCRIPTION

The Austin Semiconductor, Inc. AS8E512K8 is a 4 Megabit CMOS EEPROM Module organized as 512K x 8-bits. It is built with four 128K x 8 components and a single decoder. The AS8E512K8 achieves high speed access, low power consumption and high reliability by employing advanced CMOS memory technology. Software data protection is implemented using the JEDEC Optional Standard algorithm.

This military temperature grade product is ideally suited for military and space applications requiring high reliability.



For more products and information please visit our web site at
www.austinsemiconductor.com

DEVICE OPERATION:

The AS8E512K8 is an electricaly erasable and programmable memory module that is accessed like a Static RAM for the read or write cycle without the need for external components. The device contains a 128-byte-page register to allow writing of up to 128 bytes of data simultaneously. During a write cycle, the address and 1 to 128 bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by DATA\ polling of I/O7. Once the end of a write cycle has been detected a new access for a read or write can begin.

READ:

The AS8E512K8 is accessed like a Static RAM. When C/E\ and OE\ are low and WE\ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state when either CE\ or OE\ is high. This dual-line control gives designers flexibility in preventing bus contention in their system.

BYTE WRITE:

A low pulse on the WE\ or CE\ input with CE\ or WE\ low (respectively) and OE\ high initiates a write cycle. The address is latched on the falling edge of CE\ or WE\, whichever occurs last. The data is latched by the first rising edge of CE\ or WE\. Once a byte, word or double word write has been started it will automatically time itself to completion.

PAGE WRITE:

The page write operation of the AS8E512K8 allows 1 to 128 BWDWs of data to be written into the device during a single internal programming period. Each new BWDW must be written within 150us (t_{BLC}) of the previous BWDW. If the t_{BLC} limit is exceeded the AS8E512K8 will cease accepting data and commence the internal programming operation. For each WE\ high to low transition during the page write operation, A7-A18 must be the same.

The A0-A6 inputs are used to specify which bytes within the page are to be written. The bytes may be loaded in any order and may be altered within the same load period. Only bytes which are specified for writing will be written; unnecessary cycling of other bytes within the page does not occur.

DATA\ POLLING:

The AS8E512K8 features DATA\ Polling to indicate the end of a write cycle. During a byte or page write cycle an attempted read of the last byte written will result in the complement of the written data to be presented on I/O 7. Once the write cycle has been completed, true data is valid on all outputs, and the next write cycle may begin. DATA\ Polling may begin at anytime during the write cycle.

TOGGLE BIT:

In addition to DATA\ Polling the AS8E512K8 provides another method for determining the end of a write cycle. During the write operation, successive attempts to read data from the device will result in I/O 6 toggling between one and zero. Once the write has completed, I/O 6 will stop toggling and valid data will be read. Reading the toggle bit may begin at any time during the write cycle.

DATA PROTECTION:

If precautions are not taken, inadvertent writes may occur during transitions of the host power supply. The E^2 module has incorporated both hardware and software features that will protect the memory against inadvertent writes.

HARDWARE PROTECTION:

Hardware features protect against inadvertent writes to the AS8E512K8 in the following ways: (a) Vcc sense - if Vcc is below 3.8V (typical) the write function is inhibited; (b) Vcc power-on delay - once Vcc has reached 3.8V the device will automatically time out 5ms (typical) before allowing a write; (c) write inhibit - holding any one of OE\ low, CE\ high or WE\ high inhibits write cycles; (d) noise filter - pulses of less than 15 ns (typical) on the WE\ or CE\ inputs will not initiate a write cycle.

SOFTWARE DATA PROTECTION:

A software controlled data protection feature has been implemented on theAS8E512K8. When enabled, the software data protection (SDP), will prevent inadvertent writes. The SDP feature may be enabled or disabled by the user and is shipped with SDP disabled, SDP is enabled by the host system issuing a series of three write commands; three specific bytes of data are written to three specific addresses (refer to Software Data Protection Algorithm). After writing the three byte command sequence and after t_{WC} the entire AS8E512K8 will be protected from inadvertent write operations. It should be noted, that once protected the host may still perform a byte of page write to the AS8E512K8. This is done by preceding the data to be written by the same three byte command sequence used to enable SDP. Once set, SDP will remain active unless the disable command sequence is issued. Power transitions do not disable SDP and SDP will protect the AS8E512K8 during power-up and power-down conditions. All command sequences must conform to the page write timing specifications. The data in the enable and disable command sequences is not written to the device and the memory addresses used in the sequence may be written with data in either a byte or page write operation.

After setting SDP, any attempt to write to the device without the three byte command sequence will start the internal write timers. No data will be written to the device; however, for the duration of t_{WC}, read operations will effectively be polling operations.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss
Supply/Input Voltage Range[1].....-0.6V to +6.25V DC
Voltage on OE\ and A9.....-0.6V to +13.5V DC
Voltage on all other pins.....-0.6V to +6.25V DC
Storage Temperature.....-65°C to +150°C
Operating Temperature, T_A (Ambient).....-55°C to +125°C
Lead Temperature (soldering 10 seconds).....+300°C
Maximum Junction Temperature**.....+165°C

NOTE: 1. Including NC pins, with respect to ground.

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

** Junction temperature depends upon package type, cycle time, loading, ambient temperature and airflow.

PIN CAPACITANCE (f= 1MHz, T = 25° C)(1)

SYMBOL	CONDITIONS	MAX	UNIT
$C_{ADD, OE\backslash, WE\backslash}$	V_{IN} = 0V, f = 1MHz	45	pF
$C_{I/O}$	V_{OUT} = 0V, f = 1MHz	50	pF
$C_{CE\backslash}$	V_{IN} = 0V, f = 1MHz	10	pF

OPERATING MODES

MODE	CE\	OE\	WE\	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write[2]	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X[1]	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z

NOTE: 1. X can be V_{IL} or V_{IH}.
2. Refer to AC Programming Waveforms.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

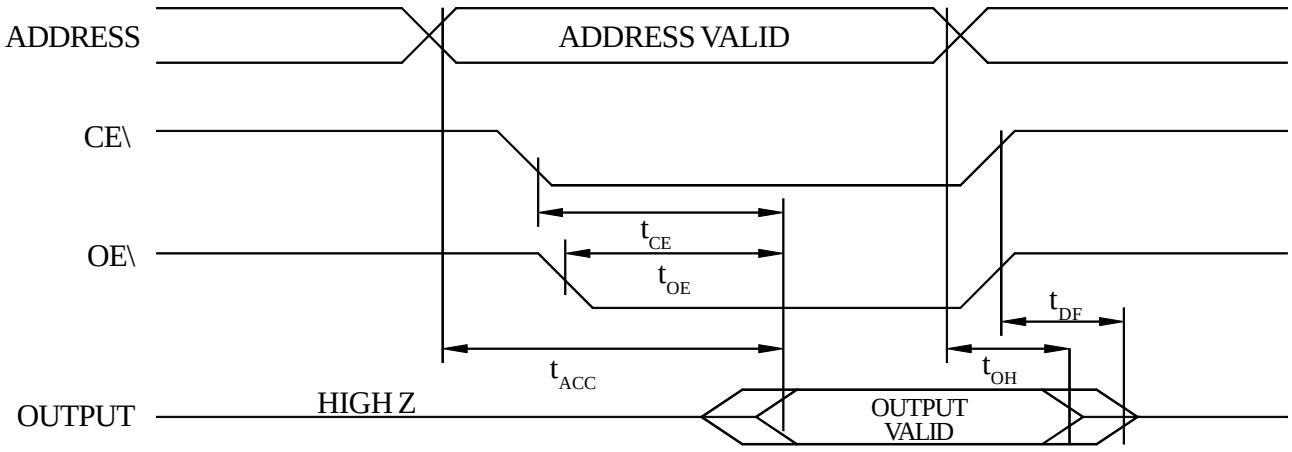
($-55°C \leq T_A \leq +125°C$; Vcc = 5V ±10%)

PARAMETER	CONDITION	SYMBOL	MIN	MAX	UNITS
Input Load Current	V_{IN} = OV to Vcc + 1V	I_{LI}	-20	20	µA
Output Leakage Current	$V_{I/O}$ = OV to Vcc	I_{LO}	-20	20	µA
Vcc Standby Current CMOS	CE\ = Vcc -0.2V to Vcc + 1	I_{SB1}			mA
Vcc Standby Current TTL	CE\ = 2.2V to Vcc + 1	I_{SB2}		20	mA
Vcc Active Current	F = 5 MHz; I_{OUT} = 0 mA	I_{CC}		120	mA
Input Low Voltage		V_{IL}		0.8	V
Input High Voltage		V_{IH}	2		V
Output Low Voltage	I_{OL} = 2.1 mA	V_{OL}		0.45	V
Output High Voltage	I_{OH} = -400 µA	V_{OH1}	2.4		V
Output High Voltage CMOS	I_{OH} = -100 µA; Vcc = 4.5V	V_{OH2}	4.2		V

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC READ OPERATING CONDITIONS ($-55^oC \leq T_A \leq +125^oC$; Vcc = 5V +10%)

DESCRIPTION	SYMBOL	-150		-200		-250		-300		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Address to Output Delay	t_{ACC}		150		200		250		300	ns
CE\ to Output Delay	t_{CE} [1]		150		200		250		300	ns
OE\ to Output Delay	t_{OE} [2]	0	50	0	55	0	55	0	65	ns
CE\ or OE\ to Output Float	t_{DF} [3,4]	0	50	0	55	0	55	0	65	ns
Output Hold from OE\, CE\ or Address, whichever occurred first	t_{OH}	0		0		0		0		ns

A.C. READ WAVEFORMS(1,2,3,4)



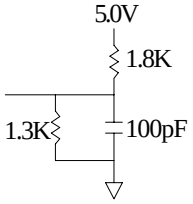
NOTES:

1. CE\ may be delayed up to t_{ACC}-t_{CE} after the address transition without inpact on t_{ACC}.
2. OE\ may be delayed up to t_{CE}-t_{OE} after the falling edge of CE\ without inpact on t_{CE} or by t_{ACC}-t_{OE} after an address change without inpact on t_{ACC}.
3. t_{DF} is specified from OE\ or CE\ whichever occurs first (C_L = 5pF).
4. This parameter is characterized and is not 100% tested.
5. A17 and A18 must remain valid through the WE\ and CE\ low pulse.

INPUT TEST WAVEFORMS AND MEASUREMENT LEVEL FOR AC TEST CONDITIONS

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	5nS
Input and Output Timing Reference Levels	1.5V

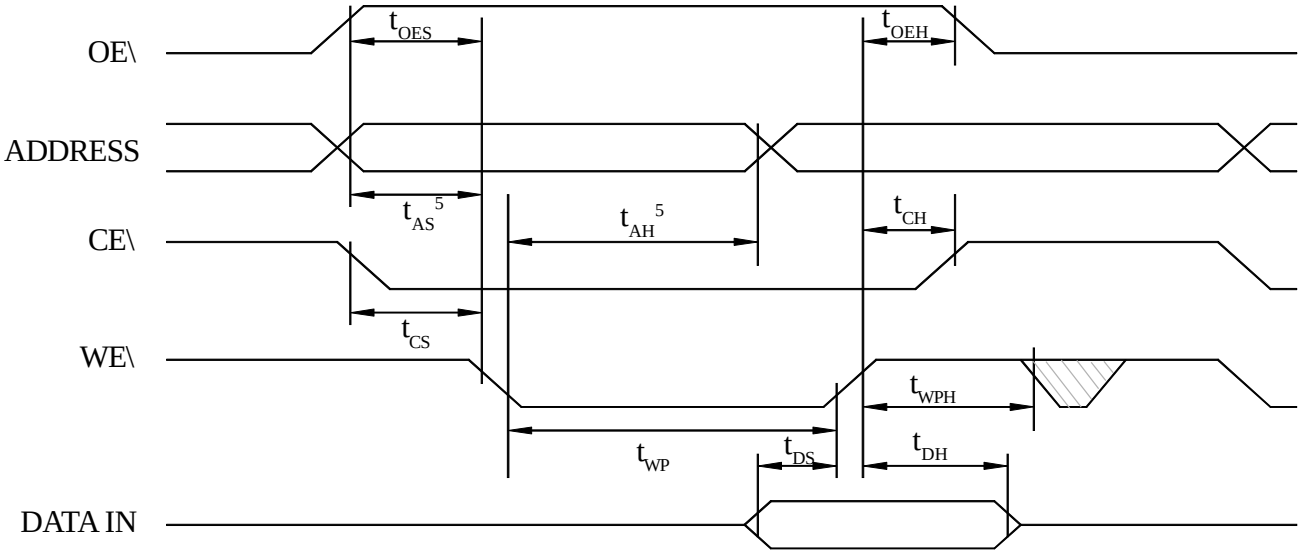
OUTPUT TEST LOAD



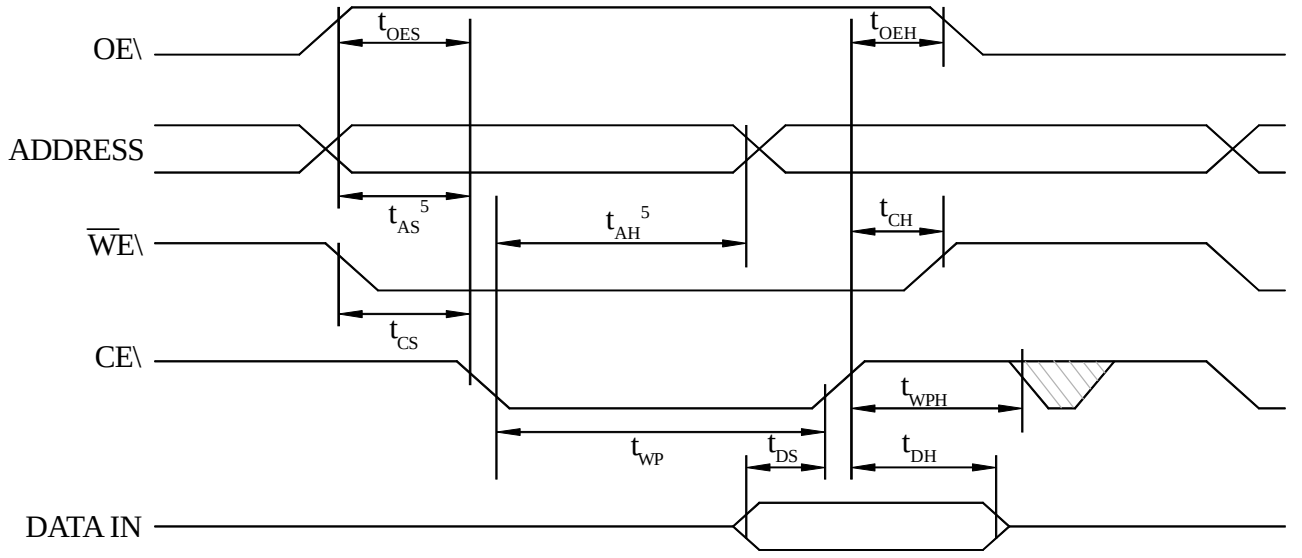
ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC WRITE OPERATING CONDITIONS ($-55^oC \leq T_A \leq +125^oC$; Vcc = 5V +10%)

SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{WC}	Write Cycle Time		10	ms
t_{AS}	Address Set-up time	10		ns
t_{AH}	Address Hold Time[5]	50		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}	Data Hold Time	0		ns
t_{WP}	Write Pulse Width	100		ns
t_{BLC}	Byte Load Cycle Time		150	µs
t_{WPH}	Write Pulse Width High	50		ns

AC WRITE WAVEFORMS - WE\ CONTROLLED[5]



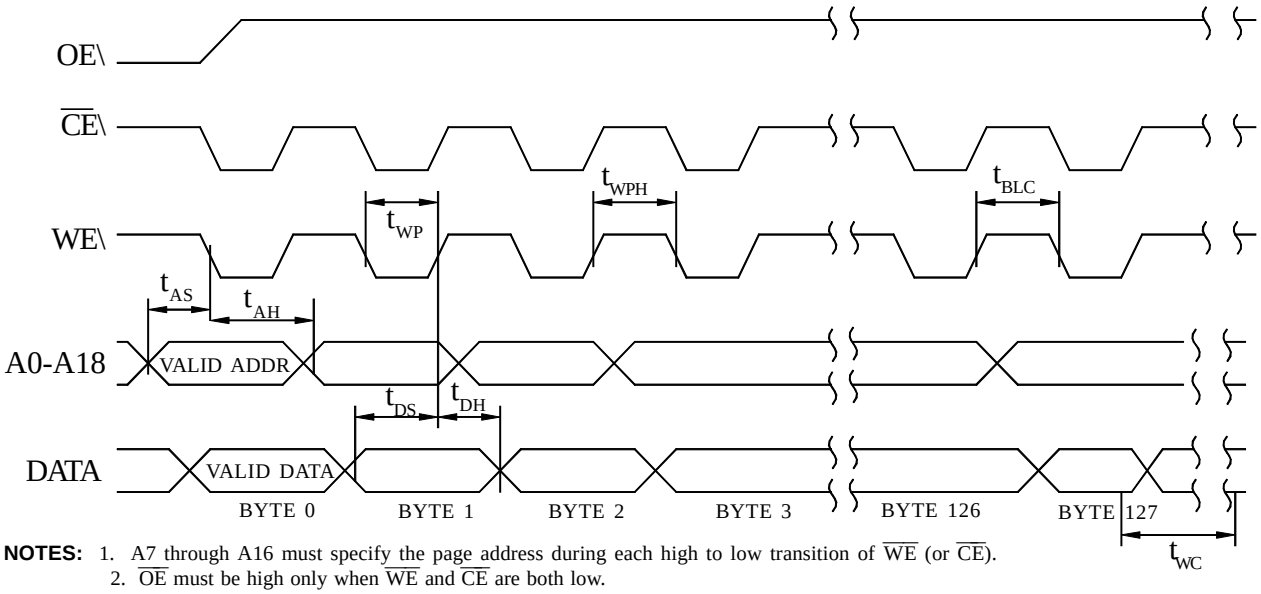
AC WRITE WAVEFORMS - CE\ CONTROLLED[5]



PAGE MODE CHARACTERISTICS

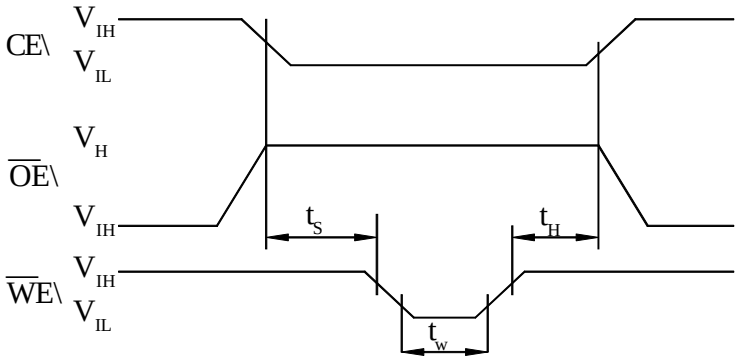
PARAMETER	SYMBOL	MIN	MAX	UNITS
Address, OE\ Setup Time	t_{AS}, t_{OES}	10		ns
Address Hold Time	t_{AH}	50		ns
Chip Select Setup Time	t_{CS}	0		ns
Chip Select Hold Time	t_{CH}	0		ns
Write Pulse Width (WE\ or CE\)	t_{WP}	100		ns
Data Setup Time	t_{DS}	50		ns
Data, OE\ Hold Time	t_{DH}, t_{OEH}	10		ns

PAGE MODE WRITE WAVEFORMS(1,2,3)



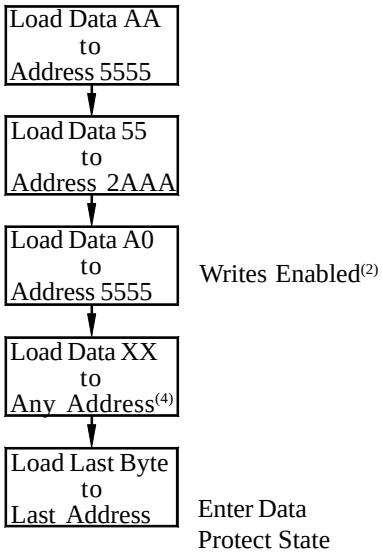
NOTES: 1. A7 through A16 must specify the page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
2. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.
3. A17 and A18 must remain valid throughout the WE\ and CE\ low.

CHIP ERASE WAVEFORMS

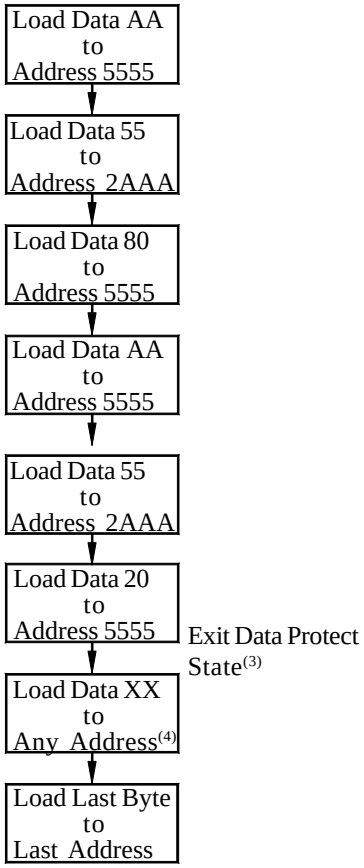


NOTES:
t_S = 5µsec (min)
$t_W = t_H$ = 10 msec (min)
V_H=12.0 V +/- 0.5 V

SOFTWARE DATA PROTECTION ENABLE ALGORITHM(1)

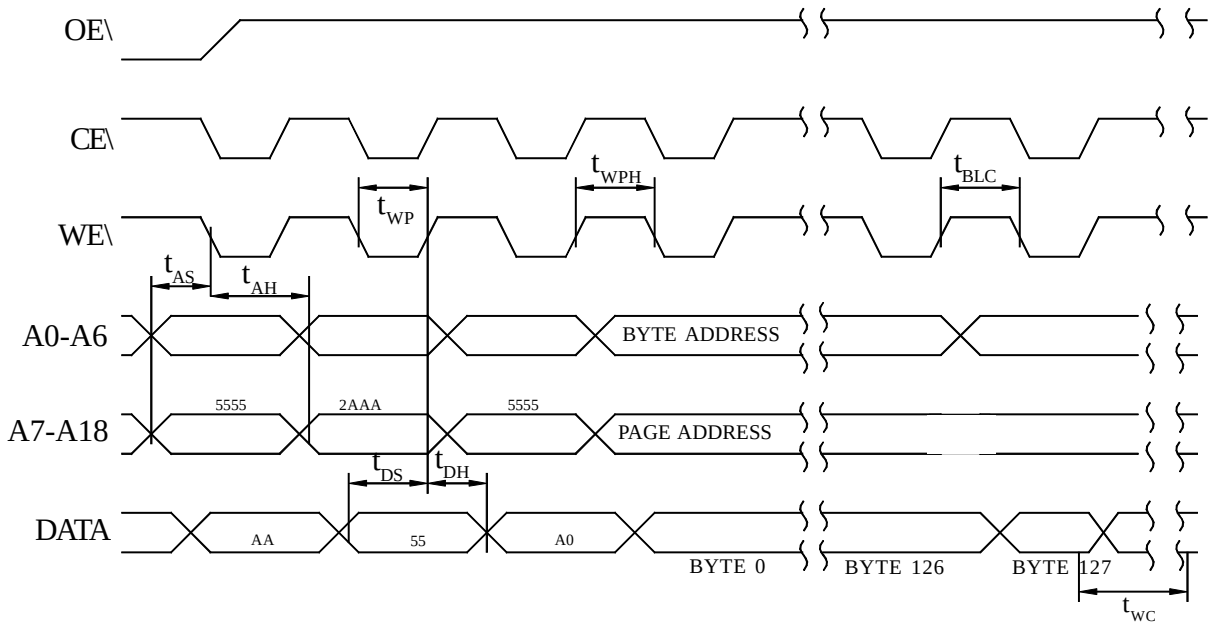


SOFTWARE DATA PROTECTION DISABLE ALGORITHM(1)



NOTES:
1. Data Format: I/O 7 - I/O0 (Hex)
2. Write Protect state will be active at end of write even if no other data is loaded.
3. Write Protect state will be deactivated at end of period even if no other data is loaded.
4. 1 to 128 bytes of data are loaded.

SOFTWARE PROTECTED PROGRAM CYCLE WAVEFORM(1,2,3,4)



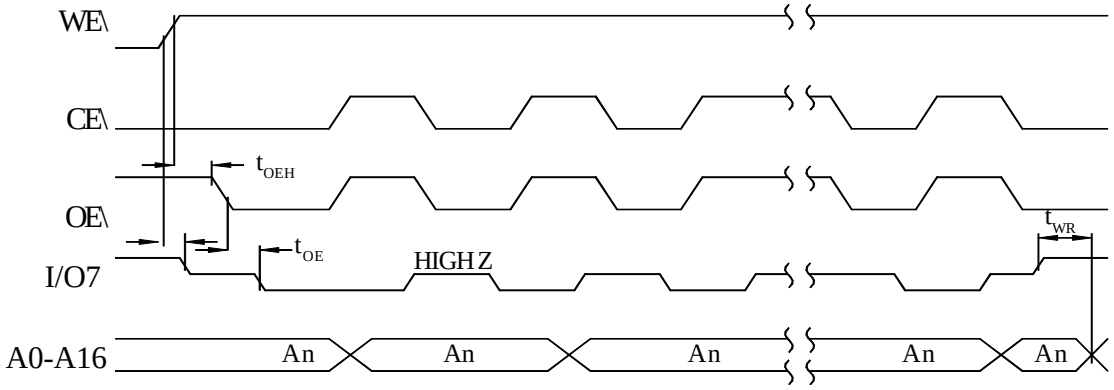
NOTES: 1. A0-A14 must conform to the addressing sequence for the first three bytes as shown above.
2. After the command sequence has been issued and a page write operation follows, the page address inputs (A7-A18) must be the same for each high to low transition of WE\ (or CE\).
3. OE\ Must be high only when WE\ and CE\ are both low.
4. A17 and A18 must remain valid throughout the WE\ and CE\ low cycle.

DATA POLLING CHARACTERISTICS[1]

PARAMETER	SYMBOL	MIN	MAX	UNITS
Data Hold Time	t_{DH}	10		ns
OE\ Hold Time	t_{OEH}	10		ns
OE\ to Output Delay[2]	t_{OE}			ns
Write Recovery Time	t_{WR}	0		ns

NOTES: 1. These parameters are characterized and not 100% tested.
2. See A.C. Read Characteristics.

DATA POLLING WAVEFORMS

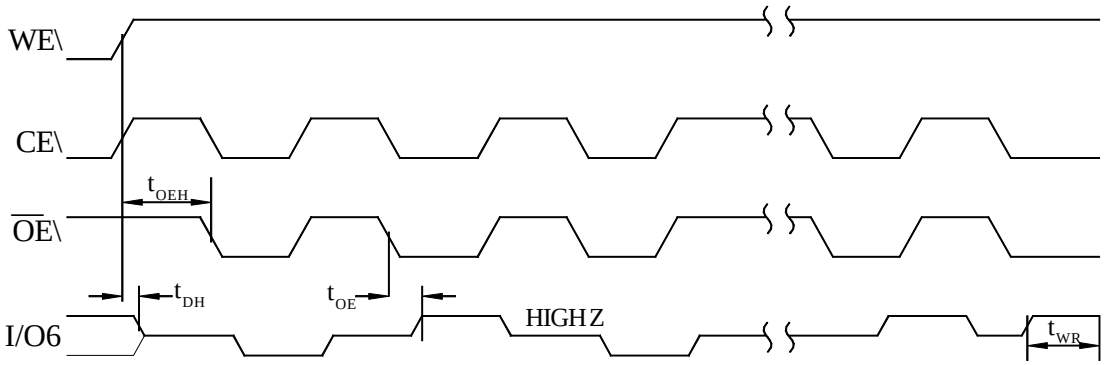


TOGGLE BIT CHARACTERISTICS(1)

PARAMETER	SYMBOL	MIN	MAX	UNITS
Data Hold Time	t_{DH}	10		ns
OE\ Hold Time	t_{OEH}	10		ns
OE\ to Output Delay[2]	t_{OE}			ns
OE\ High Pulse	t_{OEHP}	150		
Write Recovery Time	t_{WR}	0		ns

NOTES: 1. These parameters are characterized and not 100% tested.
2. See A.C. Read Characteristics.

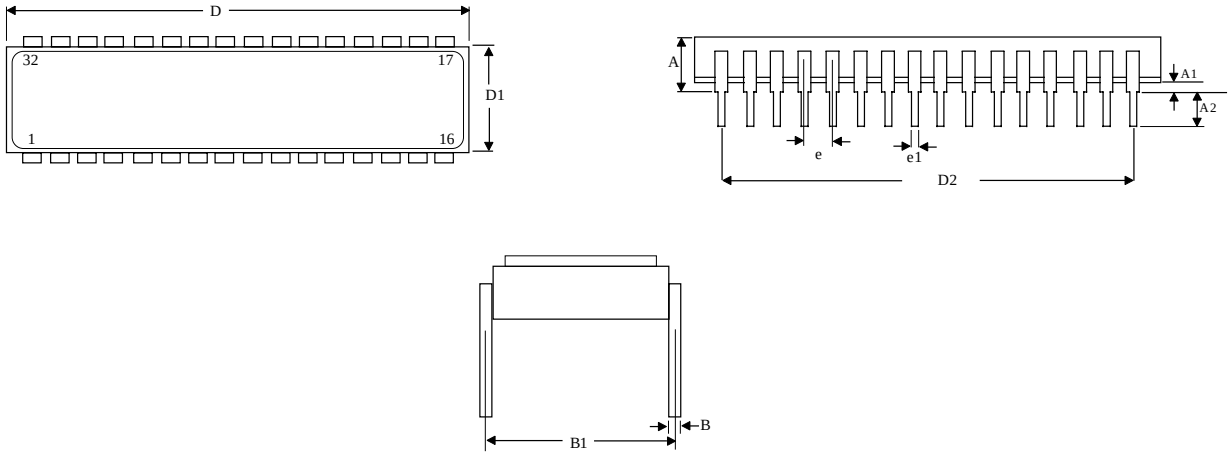
TOGGLE BIT WAVEFORMS(1,2,3)



NOTES: 1. Toggling either OE\ or CE\ or Both OE\ and CE\ will operate toggle bit.
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

MECHANICAL DEFINITIONS*

ASI Case #112 (Package Designator CW)
SMD 5962-93091, Case Outline Y



SYMBOL	SMD Specifications	
	MIN	MAX
A	0.161	0.181
A1	0.027	0.047
A2	0.125 MIN	
B	0.009	0.012
B1	0.590	0.610
D	1.654	1.686
D1	0.580	0.600
D2	1.492	1.508
e	0.100 TYP	
e1	0.016	0.02

NOTE: *These dimensions are per the SMD. ASI's package dimensional limits may differ, but they will be within the SMD limits.*

All measurements are in inches.

ORDERING INFORMATION

EXAMPLE: AS8E512K8CW-250/XT

Device Number	Package Type	Speed ns	Process
AS8E512K8	CW	-150	/*
AS8E512K8	CW	-200	/*
AS8E512K8	CW	-250	/*
AS8E512K8	CW	-300	/*

***AVAILABLE PROCESSES**

IT = Industrial Temperature Range	-40°C to +85°C
XT = Extended Temperature Range	-55°C to +125°C
HQ = MIL-PRF-38534	-55°C to +125°C

ASI TO DSCC PART NUMBER CROSS REFERENCE*

ASI Package Designator CW

ASI Part #	SMD Part #
AS8E512K8CW-150/HQ	5962-9309101HYC
AS8E512K8CW-150/HQ	5962-9309101HYA
AS8E512K8CW-200/HQ	5962-9309104HYC
AS8E512K8CW-200/HQ	5962-9309104HYA
AS8E512K8CW-250/HQ	5962-9309103HYC
AS8E512K8CW-250/HQ	5962-9309103HYA
AS8E512K8CW-300/HQ	5962-9309102HYC
AS8E512K8CW-300/HQ	5962-9309102HYA

** ASI part number is for reference only. Orders received referencing the SMD part number will be processed per the SMD.*