



Austin Semiconductor, Inc.

# SRAM AS8S512K32 & AS8S512K32A

## 512K x 32 SRAM SRAM MEMORY ARRAY

### AVAILABLE AS MILITARY SPECIFICATIONS

- SMD 5962-94611 (Military Pinout)
- MIL-STD-883

### FEATURES

- Operation with single 5V supply
- High speed: 17, 20, 25 and 35ns
- Built in decoupling caps for low noise
- Organized as 512Kx32, byte selectable
- Low power CMOS
- TTL Compatible Inputs and Outputs
- **Future offerings**
  - 3.3V Power Supply
  - 15 ns Ultra High Speed

### OPTIONS

- Operating Temperature Ranges
  - Military (-55°C to +125°C)
  - Industrial (-40°C to +85°C)
- Timing
  - 17ns
  - 20ns
  - 25ns
  - 35ns
  - 45ns
  - 55ns

### MARKINGS

- |    |        |
|----|--------|
| XT |        |
| IT |        |
| Q  | No.702 |
| P  | No.904 |
| L  |        |

- Package
  - Ceramic Quad Flatpack
  - Pin Grid Array
- Low Power Data Retention Mode
- Pinout
  - Military (no indicator)
  - Commercial A

### GENERAL DESCRIPTION

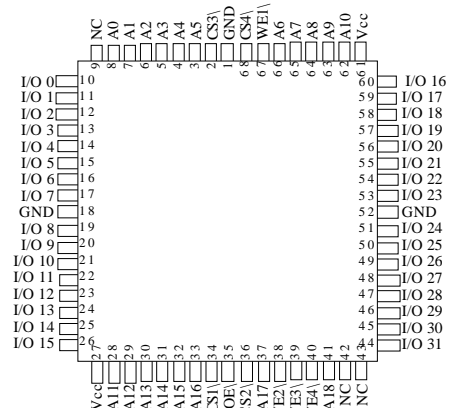
The Austin Semiconductor, Inc. AS8S512K32 and AS8S512K32A are 16 Megabit CMOS SRAM Modules organized as 512Kx32 bits. These devices achieve high speed access, low power consumption and high reliability by employing advanced CMOS memory technology.

This military temperature grade product is ideally suited for military and space applications.

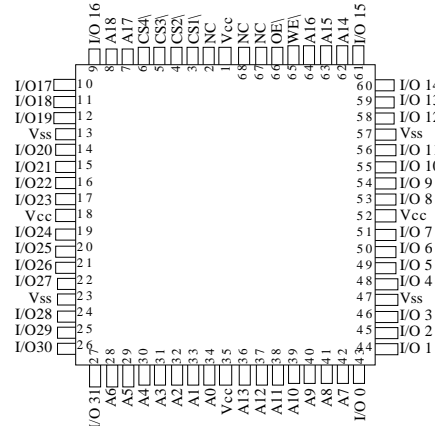
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[www.austinsemiconductor.com](http://www.austinsemiconductor.com)

### PIN ASSIGNMENT (Top View)

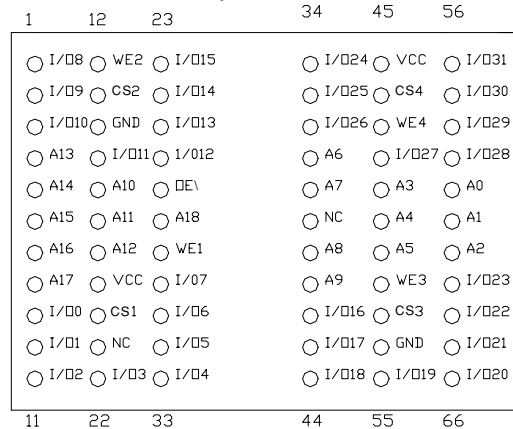
68 Lead CQFP (Q)  
Military SMD Pinout Option



68 Lead CQFP  
Commercial Pinout Option (A)



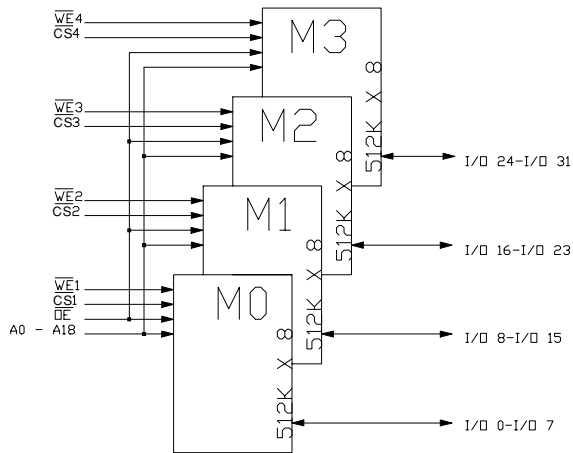
66 Lead PGA (P)  
Military SMD Pinout



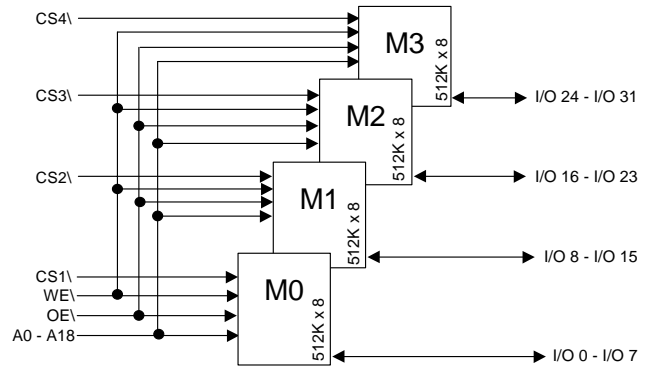


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# SRAM AS8S512K32 & AS8S512K32A



MILITARY PINOUT/BLOCK DIAGRAM



COMMERCIAL PINOUT/BLOCK DIAGRAM

### TRUTH TABLE

MODE	OE <sub>1</sub>	CS <sub>1</sub>	WE <sub>1</sub>	I/O	POWER
Read	L	L	H	D <sub>OUT</sub>	ACTIVE
Write	X	L	L	D <sub>IN</sub>	ACTIVE
Standby	X	H	X	High Z	STANDBY



**ABSOLUTE MAXIMUM RATINGS\***

Voltage of Vcc Supply Relative to Vss.....-5V to +7V  
 Storage Temperature.....-65°C to +150°C  
 Short Circuit Output Current(per I/O).....20mA  
 Voltage on Any Pin Relative to Vss.....-5V to Vcc+1V  
 Maximum Junction Temperature\*\*.....+150°C

\*Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device.

This is a stress rating only and functional operation on the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

\*\*Junction temperature depends upon package type, cycle time, loading, ambient temperature and airflow. See the Application Information section at the end of this datasheet for more information.

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS**

(-55°C ≤ T<sub>A</sub> ≤ 125°C and -40°C to +85°C; Vcc = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (logic 1) Voltage		V <sub>IH</sub>	2.2	V <sub>CC</sub> +0.5	V	1
Input Low (logic 0) Voltage		V <sub>IL</sub>	-0.5	0.8	V	1,2
Input Leakage Current <sub>ADD,OE</sub>	0V < V <sub>IN</sub> < V <sub>CC</sub>	I <sub>LI1</sub>	-10	10	μA	
Input Leakage Current <sub>WE,CE</sub>		I <sub>LI2</sub>	-10	10	μA	
Output Leakage Current <sub>I/O</sub>	Output(s) Disabled 0V < V <sub>OUT</sub> < V <sub>CC</sub>	I <sub>LO</sub>	-10	10	μA	
Output High Voltage	I <sub>OH</sub> = -4.0mA	V <sub>OH</sub>	2.4		V	1
Output Low Voltage	I <sub>OL</sub> = 8.0mA	V <sub>OL</sub>		0.4	V	1
Supply Voltage		V <sub>CC</sub>	4.5	5.5	V	1

DESCRIPTION	CONDITIONS	SYMBOL	MAX						UNITS	NOTES
			-17	-20	-25	-35	-45	-55		
Power Supply Current: Operating	CS\<V <sub>IL</sub> ; VCC = MAX f = MAX = 1/ tRC (MIN) Outputs Open	I <sub>CC</sub>	700	650	600	570	570	550	mA	3,13
Power Supply Current: Standby	CS\>V <sub>IH</sub> ; VCC = MAX f = MAX = 1/ tRC (MIN) Outputs Open	I <sub>SBT1</sub>	240	240	190	190	150	150	mA	3, 13
CMOS Standby	V <sub>IN</sub> = VCC - 0.2V, or VSS +0.2V VCC=Max; f = 0Hz	I <sub>SBT2</sub>	80	80	80	80	80	80	mA	



**CAPACITANCE** ( $V_{IN} = 0V, f = 1MHz, T_A = 25^{\circ}C$ )<sup>1</sup>

SYMBOL	PARAMETER	MAX	UNITS
$C_{ADD}$	A0 - A18 Capacitance	50	pF
$C_{OE}$	OE\ Capacitance	50	pF
$C_{WE}, C_{CS}$	WE\ and CS\ Capacitance	20	pF
$C_{IO}$	I/O 0- I/O 31 Capacitance	20	pF
$C_{WE}$ ("A" version)	WE\ Capacitance	50	pF

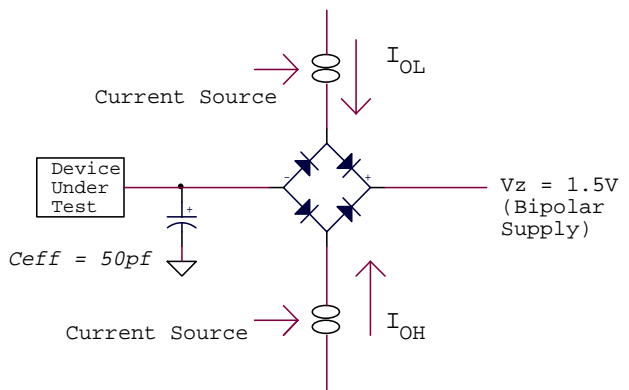
**NOTE:**

1. This parameter is sampled.

**AC TEST CONDITIONS**

**Test Specifications**

Input pulse levels.....VSS to 3V  
 Input rise and fall times.....5ns  
 Input timing reference levels.....1.5V  
 Output reference levels.....1.5V  
 Output load.....See Figure 1



**Figure 1**

**NOTES:**

- Vz is programmable from -2V to +7V.
- $I_{OL}$  and  $I_{OH}$  programmable from 0 to 16 mA.
- Vz is typically the midpoint of  $V_{OH}$  and  $V_{OL}$ .
- $I_{OL}$  and  $I_{OH}$  are adjusted to simulate a typical resistive load circuit.



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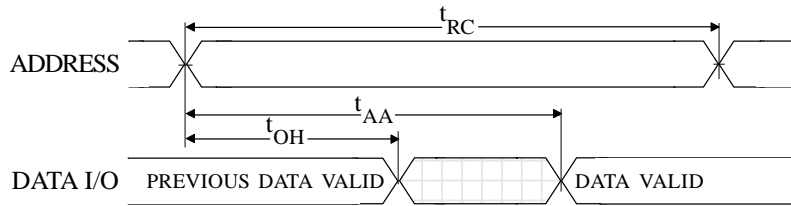
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**AS8S512K32**  
**& AS8S512K32A**

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS**  
 (NOTE 5) ( $-55^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$  and  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ;  $V_{CC} = 5\text{V} \pm 10\%$ )

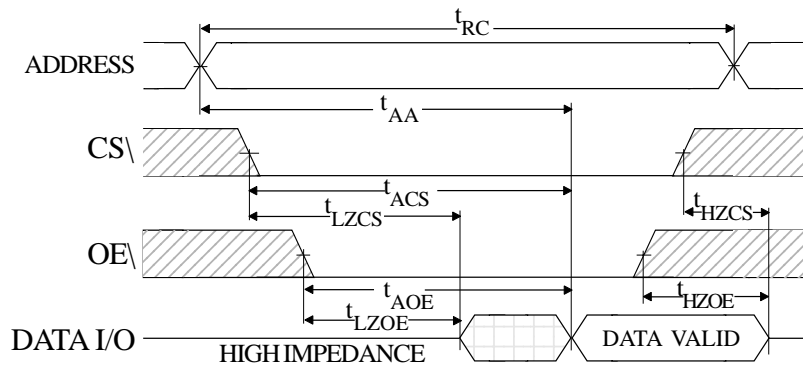
DESCRIPTION	SYMBOL	-17		-20		-25		-35		-45		-55		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
<b>READ CYCLE</b>															
READ cycle time	<sup>1</sup> RC	17		20		25		35		45		55		ns	
Address access time	<sup>1</sup> AA		17		20		25		35		45		55	ns	
Chip select access time	<sup>1</sup> ACS		17		20		25		35		45		55	ns	
Output hold from address change	<sup>1</sup> OH	2		2		2		2		2		2		ns	
Chip select to output in Low-Z	<sup>1</sup> LZCS	2		2		2		2		2		2		ns	4,6,7
Chip select to output in High-Z	<sup>1</sup> HZCS		9		10		12		15		20		20	ns	4,6,7
Output enable access time	<sup>1</sup> AOE		9		10		12		15		20		20	ns	
Output enable to output in Low-Z	<sup>1</sup> LZOE	0		0		0		0		0		0		ns	4,6
Output disable to output in High-Z	<sup>1</sup> HZOE		12		12		12		15		20		20	ns	4,6
<b>WRITE CYCLE</b>															
WRITE cycle time	<sup>1</sup> WC	17		20		25		35		45		55		ns	
Chip select to end of write	<sup>1</sup> CW	15		15		17		20		25		25		ns	
Address valid to end of write	<sup>1</sup> AW	15		15		17		20		25		25		ns	
Address setup time	<sup>1</sup> AS	2		2		2		2		2		2		ns	
Address hold from end of write	<sup>1</sup> AH	1		1		1		1		1		1		ns	
WRITE pulse width	<sup>1</sup> WP1	15		15		17		20		25		25		ns	
WRITE pulse width	<sup>1</sup> WP2	15		15		17		20		25		25		ns	
Data setup time	<sup>1</sup> DS	12		10		12		15		20		20		ns	
Data hold time	<sup>1</sup> DH	0		0		0		0		0		0		ns	
Write disable to output in Low-z	<sup>1</sup> LZWE	2		2		2		2		2		2		ns	4,6,7
Write enable to output in High-Z	<sup>1</sup> HZWE		9		11		13		15		15		15	ns	4,6,7



### READ CYCLE NO. 1

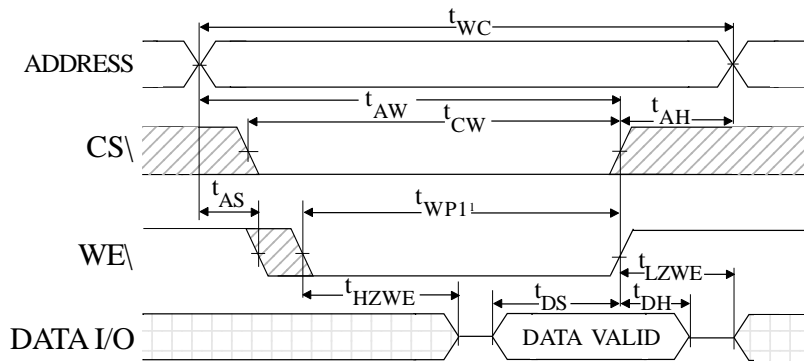


### READ CYCLE NO. 2

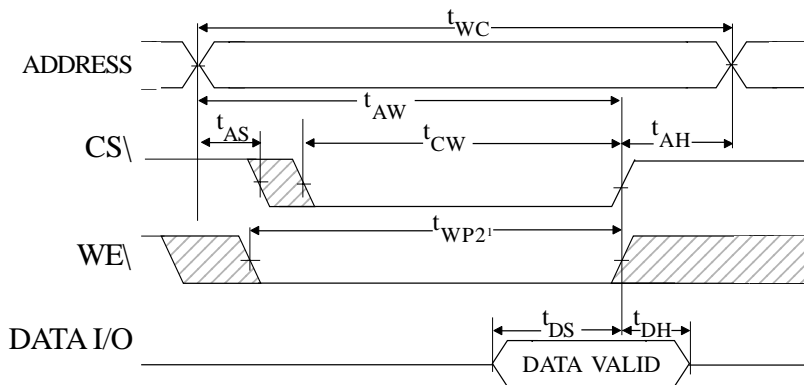




**WRITE CYCLE NO. 1**  
(Chip Select Controlled)



**WRITE CYCLE NO. 2**  
(Write Enable Controlled)





**NOTES**

1. All voltages referenced to  $V_{SS}$  (GND).
2. -2V for pulse width <20ns.
3.  $I_{CC}$  is dependent on output loading and cycle rates.

unloaded, and  $f = \frac{1}{t_{RC(MIN)}} \text{ Hz}$

The specified value applies with the outputs

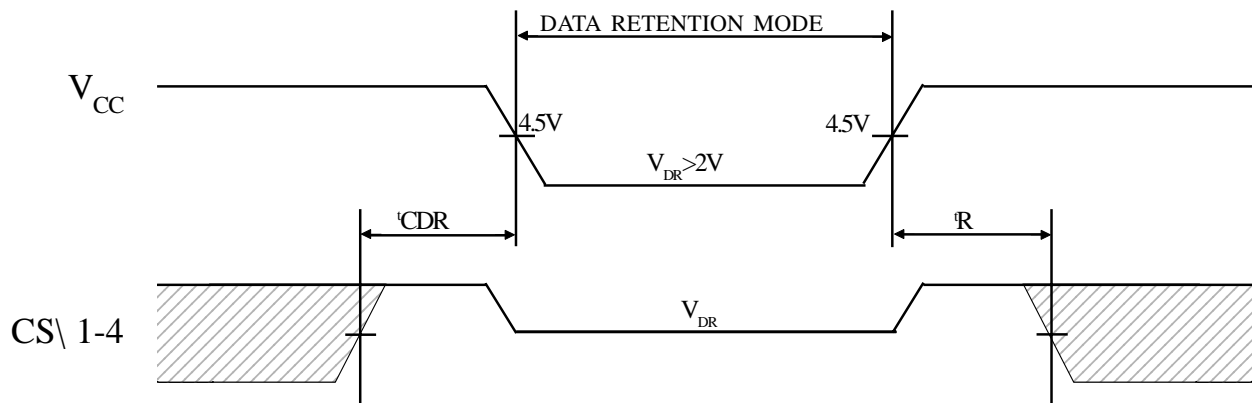
4. This parameter guaranteed but not tested.
5. Test conditions as specified with output loading as shown in Fig. 1 unless otherwise noted.
6.  $t_{HZCS}$ ,  $t_{HZOE}$  and  $t_{HZWE}$  are specified with  $C_L = 5\text{pF}$  as in Fig. 2. Transition is measured +/- 200 mV typical from steady state voltage, allowing for actual tester RC time constant.

7. At any given temperature and voltage condition,  $t_{HZCS}$ , is less than  $t_{LZCS}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$ .
8.  $WE\backslash$  is HIGH for READ cycle.
9. Device is continuously selected. Chip selects and output enable are held in their active state.
10. Address valid prior to or coincident with latest occurring chip enable.
11.  $t_{RC}$  = READ cycle time.
12. Chip enable ( $CS\backslash$ ) and write enable ( $WE\backslash$ ) can initiate and terminate a WRITE cycle.
13.  $I_{CC}$  is for 32 bit mode.

**LOW POWER CHARACTERISTICS (L Version Only)**

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
$V_{CC}$ for Retention Data		$V_{DR}$	2		V	
Data Retention Current	All Inputs @ $V_{CC} \pm 0.2V$ or $V_{SS} \pm 0.2V$ , $CS\backslash = V_{CC} \pm 0.2V$	$V_{CC} = 2V$	$I_{CCDR}$	20	mA	
		$V_{CC} = 3V$	$I_{CCDR}$	28	mA	
Chip Deselect to Data Retention Time		$t_{CDR}$	0		ns	4
Operation Recovery Time		$t_R$	$t_{RC}$		ns	4, 11

**LOW  $V_{CC}$  DATA RETENTION WAVEFORM**





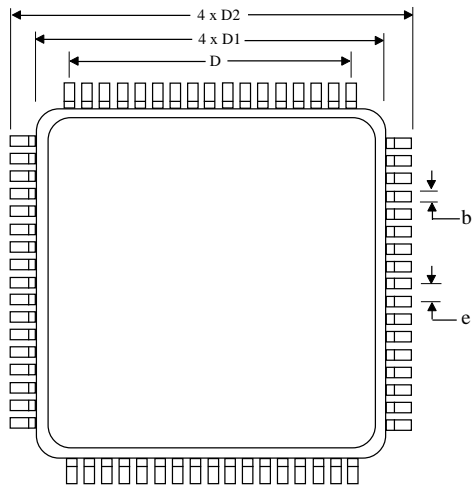


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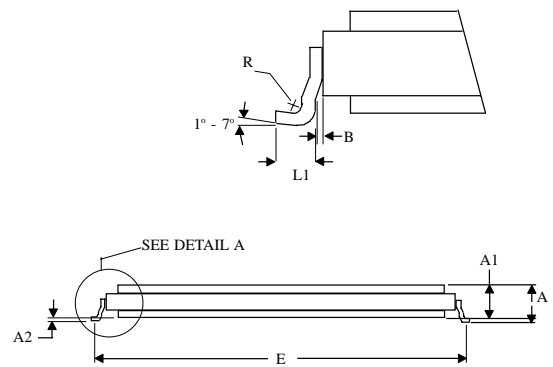
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**AS8S512K32**  
**& AS8S512K32A**

**MECHANICAL DEFINITIONS\***

ASI Case #702 (Package Designator Q)  
 SMD 5962-94611, Case Outline M



DETAIL A



SYMBOL	SMD SPECIFICATIONS	
	MIN	MAX
A	0.123	0.200
A1	0.118	0.186
A2	0.000	0.020
B	0.010 REF	
b	0.013	0.017
D	0.800 BSC	
D1	0.870	0.890
D2	0.980	1.000
E	0.936	0.956
e	0.050 BSC	
R	0.005	---
L1	0.035	0.045

\*All measurements are in inches.

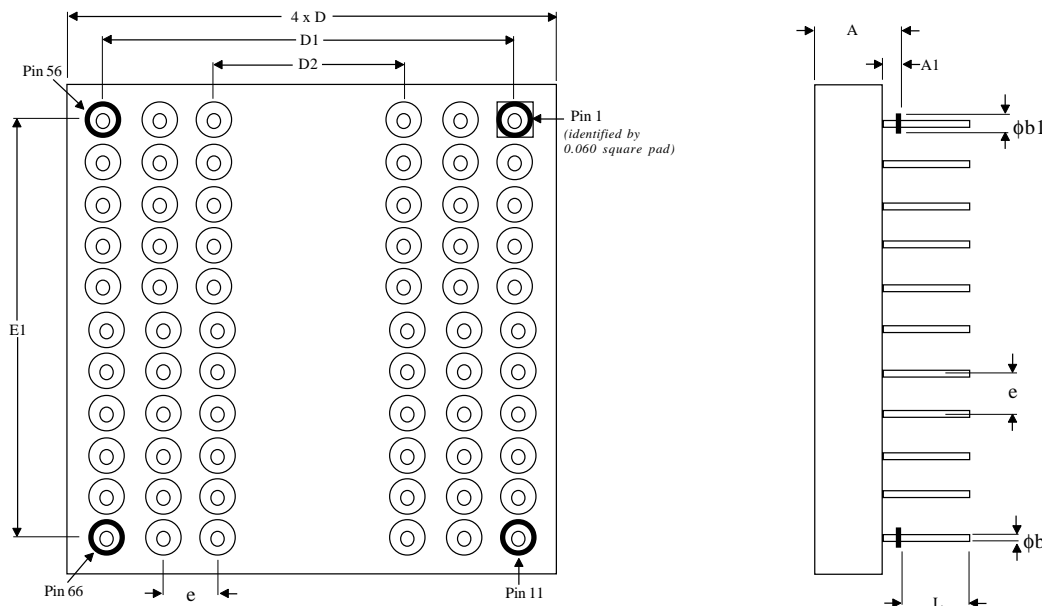


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**SRAM**  
**AS8S512K32**  
**& AS8S512K32A**

**MECHANICAL DEFINITIONS\***

ASI Case #904 (Package Designator P )  
 SMD 5962-94611, Case Outline T



SYMBOL	SMD SPECIFICATIONS	
	MIN	MAX
A	0.144	0.181
A1	0.025	0.035
$\phi b$	0.016	0.020
$\phi b1$	0.045	0.055
D	1.065	1.085
D1/E1	1.000 TYP	
D2	0.600 TYP	
e	0.100 TYP	
L	0.145	0.155

\*All measurements are in inches.



## ORDERING INFORMATION

EXAMPLE: AS8S512K32Q-25L/XT

Device Number	Options**	Package Type	Speed ns	Options**	Process
AS8S512K32	A	Q	-17	L	/*
AS8S512K32	A	Q	-20	L	/*
AS8S512K32	A	Q	-25	L	/*
AS8S512K32	A	Q	-35	L	/*
AS8S512K32	A	Q	-45	L	/*
AS8S512K32	A	Q	-55	L	/*

EXAMPLE: AS8S512K32AP-25/XT

Device Number	Options**	Package Type	Speed ns	Options**	Process
AS8S512K32	A	P	-17	L	/*
AS8S512K32	A	P	-20	L	/*
AS8S512K32	A	P	-25	L	/*
AS8S512K32	A	P	-35	L	/*
AS8S512K32	A	P	-45	L	/*
AS8S512K32	A	P	-55	L	/*

### \*AVAILABLE PROCESSES

IT = Industrial Temperature Range      -40°C to +85°C  
 XT = Extended Temperature Range      -55°C to +125°C  
 833C = Full Military Processing      -55°C to +125°C

### \*\*DEFINITION OF OPTIONS

A = Commercial Pinout  
 no indicator = Military Pinout  
 L = Low Power Data Retention Mode



## ASI TO DSCC PART NUMBER CROSS REFERENCE

### Package Designator Q

<b>ASI Part #</b>	<b>SMD Part #</b>
AS8S512K32Q-17L/883C	5962-9461110HMA
AS8S512K32Q-17L/883C	5962-9461110HMC
AS8S512K32Q-20L/883C	5962-9461109HMA
AS8S512K32Q-20L/883C	5962-9461109HMC
AS8S512K32Q-25L/883C	5962-9461108HMA
AS8S512K32Q-25L/883C	5962-9461108HMC
AS8S512K32Q-35L/883C	5962-9461107HMA
AS8S512K32Q-35L/883C	5962-9461107HMC
AS8S512K32Q-45L/883C	5962-9461106HMA
AS8S512K32Q-45L/883C	5962-9461106HMC
AS8S512K32Q-55L/883C	5962-9461105HMA
AS8S512K32Q-55L/883C	5962-9461105HMC
AS8S512K32Q-17/883C	5962-9461116HMA
AS8S512K32Q-17/883C	5962-9461116HMC
AS8S512K32Q-20/883C	5962-9461115HMA
AS8S512K32Q-20/883C	5962-9461115HMC
AS8S512K32Q-25/883C	5962-9461114HMA
AS8S512K32Q-25/883C	5962-9461114HMC
AS8S512K32Q-35/883C	5962-9461113HMA
AS8S512K32Q-35/883C	5962-9461113HMC
AS8S512K32Q-45/883C	5962-9461112HMA
AS8S512K32Q-45/883C	5962-9461112HMC
AS8S512K32Q-55/883C	5962-9461111HMA
AS8S512K32Q-55/883C	5962-9461111HMC

### Package Designator P

<b>ASI Part #</b>	<b>SMD Part #</b>
AS8S512K32P-17L/883C	5962-9461110HTA
AS8S512K32P-17L/883C	5962-9461110HTC
AS8S512K32P-20L/883C	5962-9461109HTA
AS8S512K32P-20L/883C	5962-9461109HTC
AS8S512K32P-25L/883C	5962-9461108HTA
AS8S512K32P-25L/883C	5962-9461108HTC
AS8S512K32P-35L/883C	5962-9461107HTA
AS8S512K32P-35L/883C	5962-9461107HTC
AS8S512K32P-45L/883C	5962-9461106HTA
AS8S512K32P-45L/883C	5962-9461106HTC
AS8S512K32P-55L/883C	5962-9461105HTA
AS8S512K32P-55L/883C	5962-9461105HTC
AS8S512K32P-17/883C	5962-9461116HTA
AS8S512K32P-17/883C	5962-9461116HTC
AS8S512K32P-20/883C	5962-9461115HTA
AS8S512K32P-20/883C	5962-9461115HTC
AS8S512K32P-25/883C	5962-9461114HTA
AS8S512K32P-25/883C	5962-9461114HTC
AS8S512K32P-35/883C	5962-9461113HTA
AS8S512K32P-35/883C	5962-9461113HTC
AS8S512K32P-45/883C	5962-9461112HTA
AS8S512K32P-45/883C	5962-9461112HTC
AS8S512K32P-55/883C	5962-9461111HTA
AS8S512K32P-55/883C	5962-9461111HTC