- **Organization . . . 1048576 by 16 Bits**
- **Single 5-V Power Supply (±10% Tolerance)**
- **Performance Ranges:**

	ACCESS TIME t_{RAC} MAX	ACCESS TIME t_{CAC} MAX	ACCESS TIME t_{AA} MAX	READ OR WRITE CYCLE MIN
'41x160-70	70 ns	18 ns	35 ns	130 ns
'41x160-80	80 ns	20 ns	40 ns	150 ns

- **Enhanced Page-Mode Operation for Faster Memory Access**
- **$\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ (CBR) Refresh**
- **Long Refresh Period**
  - **'416160 – 4096-Cycle Refresh in 32 ms (Maximum)**
  - **'418160 – 1024-Cycle Refresh in 8 ms (Maximum)**
- **3-State Unlatched Output**
- **Low Power Dissipation**
- **All Inputs/Outputs Are TTL Compatible**
- **Packaging**
  50-Lead, 650-Mil-Wide Ceramic Flatpack
- **Operating Free-Air Temperature Range**
  –55°C to 125°C

description

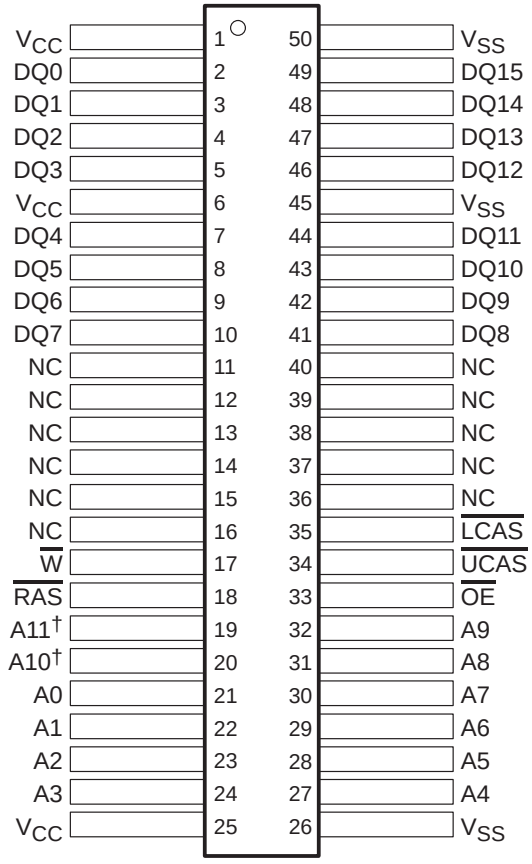
The SMJ41x160 series is a set of 16777216-bit dynamic random-access memories (DRAMs) organized as 1048576 words of 16 bits each.

They employ state-of-the-art technology for high performance, reliability, and low power at low cost.

These devices feature maximum $\overline{\text{RAS}}$ access times of 70 ns and 80 ns. All addresses and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The SMJ41x160 series is offered in a 50-lead, 650-mil-wide ceramic flatpack and is characterized for operation from –55°C to 125°C.

HKD PACKAGE
(TOP VIEW)

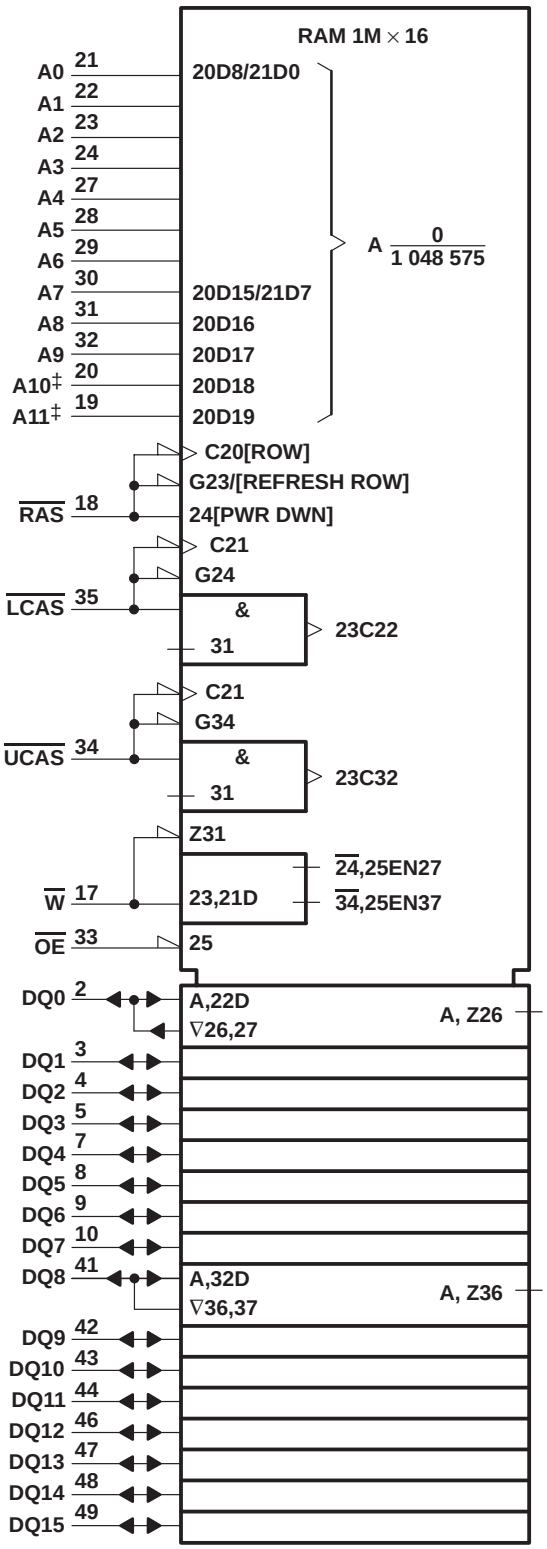


† A10 and A11 are NC for SMJ418160.

PIN NOMENCLATURE	
A0–A11	Address Inputs
DQ0–DQ15	Data In/Data Out
$\overline{\text{LCAS}}$	Lower Column-Address Strobe
$\overline{\text{UCAS}}$	Upper Column-Address Strobe
NC	No Internal Connection
$\overline{\text{OE}}$	Output Enable
$\overline{\text{RAS}}$	Row-Address Strobe
V_{CC}	5-V Supply
V_{SS}	Ground
$\overline{\text{W}}$	Write Enable

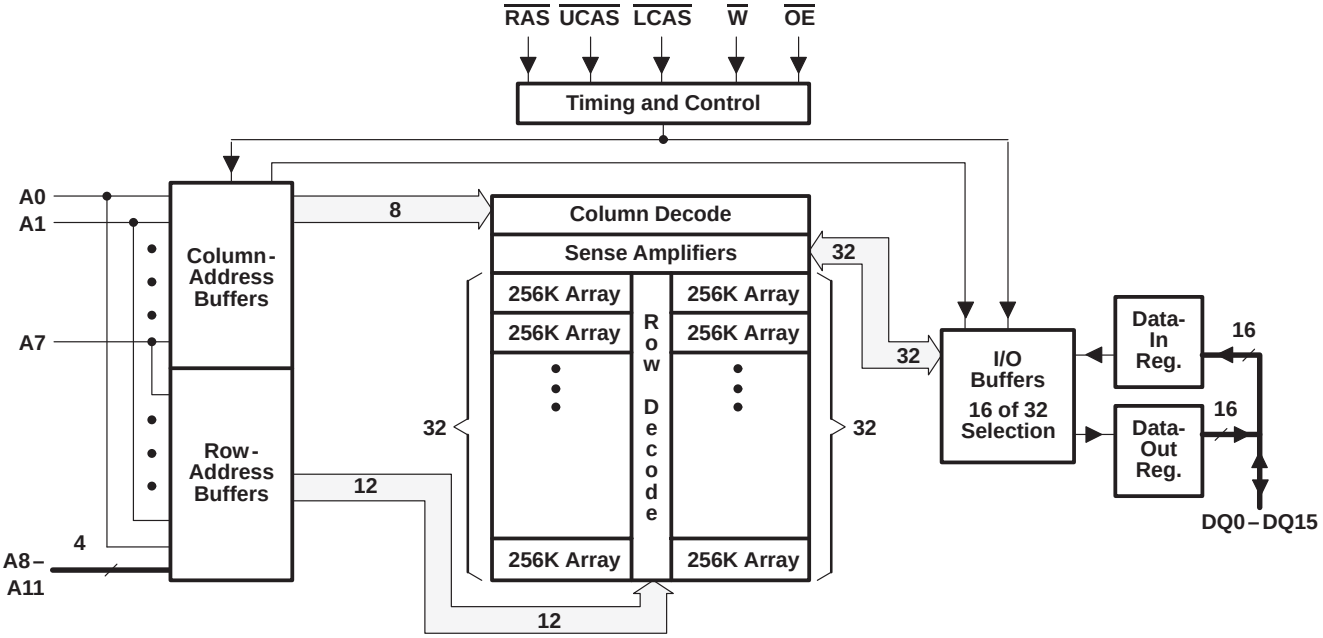
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

logic symbol†

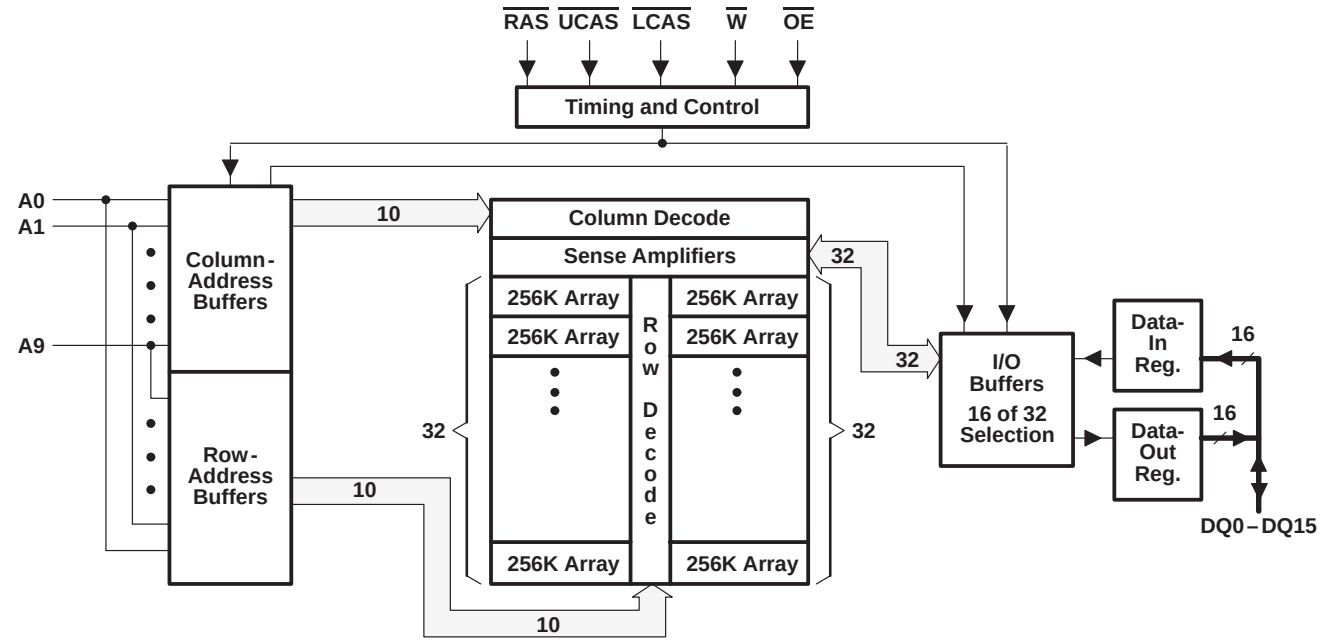


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
‡ A10 and A11 are NC for SMJ418160.

’416160 functional block diagram



’418160 functional block diagram



operation

dual $\overline{CAS}$

Two $\overline{CAS}$ pins ($\overline{LCAS}$ and $\overline{UCAS}$) are provided to give independent control of the 16 data-I/O pins (DQ0–DQ15), with $\overline{LCAS}$ corresponding to DQ0–DQ7 and $\overline{UCAS}$ corresponding to DQ8–DQ15. For read or write cycles, the column address is latched on the first $\overline{xCAS}$ falling edge. Each $\overline{xCAS}$ going low enables its corresponding DQx pin with data associated with the column address latched on the first falling $\overline{xCAS}$ edge. All address-setup and -hold parameters are referenced to the first falling $\overline{xCAS}$ edge.The delay time from $\overline{xCAS}$ low to valid data out (see parameter t_{CAC}) is measured from each individual $\overline{xCAS}$ to its corresponding DQx pin.

In order to latch in a new column address, both $\overline{xCAS}$ pins must be brought high. The column-precharge time (see parameter t_{CP}) is measured from the last $\overline{xCAS}$ rising edge to the first $\overline{xCAS}$ falling edge of the new cycle. Keeping a column address valid while toggling $\overline{xCAS}$ requires a minimum setup time, t_{CLCH}. During t_{CLCH}, at least one $\overline{xCAS}$ must be brought low before the other $\overline{xCAS}$ is taken high.

For early-write cycles, the data is latched on the first $\overline{xCAS}$ falling edge. Only the DQs that have the corresponding $\overline{xCAS}$ low are written into. Each $\overline{xCAS}$ must meet t_{CAS} minimum in order to ensure writing into the storage cell. To latch a new address and new data, all $\overline{xCAS}$ pins must be high and meet t_{CP}.

enhanced page mode

Enhanced page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row-address setup and hold and address multiplex is eliminated. The maximum number of columns that can be accessed is determined by the maximum $\overline{RAS}$ low time and the $\overline{xCAS}$ page-mode cycle time used. With minimum $\overline{xCAS}$ page-cycle time, all columns can be accessed without intervening $\overline{RAS}$ cycles.

Unlike conventional page-mode DRAMs, the column-address buffers in this device are activated on the falling edge of $\overline{RAS}$. The buffers act as transparent or flow-through latches while $\overline{xCAS}$ is high. The falling edge of the first $\overline{xCAS}$ latches the column addresses. This feature allows the device to operate at a higher data bandwidth than conventional page-mode parts because data retrieval begins as soon as the column address is valid rather than when $\overline{xCAS}$ goes low. This performance improvement is referred to as enhanced page mode. A valid column address can be presented immediately after row-address hold time (t_{RAH}) has been satisfied, usually well in advance of the falling edge of $\overline{xCAS}$. In this case, data is obtained after access time from xCAS low (t_{CAC}) maximum if access time from column address (t_{AA}) maximum has been satisfied. In the event that column addresses for the next page cycle are valid at the time $\overline{xCAS}$ goes high, minimum-access time for the next cycle is determined by access time from rising edge of the last $\overline{xCAS}$ (t_{CPA}).

address: A0–A11 (’416160) and A0–A9 (’418160)

Twenty address bits are required to decode one of the 1048576 storage-cell locations. For the SMJ416160, 12 row-address bits are set up on A0 through A11 and latched onto the chip by $\overline{RAS}$. Eight column-address bits are set up on A0 through A7 and latched onto the chip by the first $\overline{xCAS}$. For the SMJ418160, ten row-address bits are set up on A0–A9 and latched onto the chip by $\overline{RAS}$. Ten column-address bits are set up on A0–A9 and latched onto the chip by the first $\overline{xCAS}$. All addresses must be stable on or before the falling edge of $\overline{RAS}$ and $\overline{xCAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{xCAS}$ is used as a chip select, activating its corresponding output buffer and latching the address bits into the column-address buffers.

write enable ($\overline{W}$)

The read or write mode is selected through $\overline{W}$. A logic high on $\overline{W}$ selects the read mode and a logic low selects the write mode. The data inputs are disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{xCAS}$ (early write), data out remains in the high-impedance state for the entire cycle, permitting a write operation with $\overline{OE}$ grounded.

data in (DQ0–DQ15)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling edge of $\overline{\text{xCAS}}$ or $\overline{\text{W}}$ strobes data into the on-chip data latch. In an early-write cycle, $\overline{\text{W}}$ is brought low prior to $\overline{\text{xCAS}}$ and the data is strobed in by the first $\overline{\text{xCAS}}$ occurrence with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{\text{xCAS}}$ is low already and the data is strobed in by $\overline{\text{W}}$ with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{\text{OE}}$ must be high to bring the output buffers to the high-impedance state prior to impressing data on the I/O lines.

data out (DQ0–DQ15)

Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{\text{xCAS}}$ and $\overline{\text{OE}}$ are brought low. In a read cycle, the output becomes valid after the access-time interval t_{CAC}. t_{CAC} begins with the negative transition of $\overline{\text{xCAS}}$ as long as t_{RAC} and t_{AA} are satisfied.

output enable ($\overline{\text{OE}}$)

$\overline{\text{OE}}$ controls the impedance of the output buffers. When $\overline{\text{OE}}$ is high, the buffers remain in the high-impedance state. Bringing $\overline{\text{OE}}$ low during a normal cycle activates the output buffers, putting them in the low-impedance state. It is necessary for both $\overline{\text{RAS}}$ and $\overline{\text{xCAS}}$ to be brought low for the output buffers to go into the low-impedance state, and they remain in the low-impedance state until either $\overline{\text{OE}}$ or $\overline{\text{xCAS}}$ is brought high.

$\overline{\text{RAS}}$-only refresh ’416160

A refresh operation must be performed at least once every 32 ms to retain data. This can be achieved by strobing each of the 4096 rows (A0–A11). A normal-read or -write cycle refreshes all bits in each row that is selected. A $\overline{\text{RAS}}$-only operation can be used by holding both $\overline{\text{xCAS}}$ at the high (inactive) level, conserving power as the output buffers remain in the high-impedance state. Externally generated addresses must be used for a $\overline{\text{RAS}}$-only refresh.

$\overline{\text{RAS}}$-only refresh ’418160

A refresh operation must be performed at least once every 8 ms to retain data. This can be achieved by strobing each of the 1024 rows (A0–A9). A normal-read or -write cycle refreshes all bits in each row that is selected. A $\overline{\text{RAS}}$-only operation can be used by holding both $\overline{\text{xCAS}}$ at the high (inactive) level, conserving power as the output buffers remain in the high-impedance state. Externally generated addresses must be used for a $\overline{\text{RAS}}$-only refresh.

hidden refresh

Hidden refresh can be performed while maintaining valid data at the output pin. This is accomplished by holding $\overline{\text{xCAS}}$ at V_{IL} after a read operation and cycling $\overline{\text{RAS}}$ after a specified precharge period, similar to a $\overline{\text{RAS}}$-only refresh cycle. The external address is ignored and the refresh address is generated internally.

$\overline{\text{xCAS}}$-before-$\overline{\text{RAS}}$ (xCBR) refresh

xCBR refresh is utilized by bringing at least one $\overline{\text{xCAS}}$ low earlier than $\overline{\text{RAS}}$ (see parameter t_{CSR}) and holding it low after $\overline{\text{RAS}}$ falls (see parameter t_{CHR}). For successive xCBR refresh cycles, $\overline{\text{xCAS}}$ can remain low while cycling $\overline{\text{RAS}}$. The external address is ignored and the refresh address is generated internally.

power up

To achieve proper device operation, an initial pause of 200 µs followed by a minimum of eight initialization cycles is required after power up to the full V_{CC} level. These eight initialization cycles must include at least one refresh ($\overline{\text{RAS}}$-only or xCBR) cycle.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . – 1 V to 7 V
Voltage range on any pin (see Note 1) . . . . . – 1 V to 7 V
Short-circuit output current . . . . . 50 mA
Power dissipation . . . . . 1 W
Operating free-air temperature range, T_A . . . . . – 55°C to 125°C
Storage temperature range, T_{stg} . . . . . – 65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Operating free-air temperature	– 55		125	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used for logic-voltage levels only.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

SMJ416160

PARAMETER		TEST CONDITIONS†	'416160-70		'416160-80		UNIT
			MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 V to 6.5 V, All others = 0 V to V_{CC}		± 10		± 10	µA
I_O	Output current (leakage)	$\overline{V_{CC}}$ = 5.5 V, V_O = 0 V to V_{CC}, $\overline{xCAS}$ high		± 10		± 10	µA
I_{CC1}‡§	Read- or write-cycle current	V_{CC} = 5.5 V, Minimum cycle		80		70	mA
I_{CC2}	Standby current	V_{IH} = 2.4 V (TTL), After one memory cycle, $\overline{RAS}$ and $\overline{xCAS}$ high		2		2	mA
		V_{IH} = V_{CC} – 0.2 V (CMOS), After one memory cycle, $\overline{RAS}$ and $\overline{xCAS}$ high		1		1	mA
I_{CC3}§	Average refresh current ($\overline{RAS}$ only refresh or CBR)	$\overline{V_{CC}}$ = 5.5 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{xCAS}$ high ($\overline{RAS}$ only), $\overline{RAS}$ low after $\overline{xCAS}$ low (CBR)		80		70	mA
I_{CC4}‡¶	Average page current	$\overline{V_{CC}}$ = 5.5 V, $t_{\overline{PC}}$ = MIN, $\overline{RAS}$ low, $\overline{xCAS}$ cycling		80		70	mA
I_{CC7}‡¶	Standby current, outputs enabled	$\overline{RAS}$ = V_{IH}, $\overline{xCAS}$ = V_{IL}, Data out = enabled		5		5	mA

† For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.
‡ Measured with outputs open
§ Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
¶ Measured with a maximum of one address change while $\overline{xCAS}$ = V_{IH}

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

SMJ418160

PARAMETER		TEST CONDITIONS†	'418160-70		'418160-80		UNIT
			MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 V to 6.5 V, All others = 0 V to V_{CC}		± 10		± 10	µA
I_O	Output current (leakage)	$\overline{V_{CC}}$ = 5.5 V, V_O = 0 V to V_{CC}, $\overline{xCAS}$ high		± 10		± 10	µA
I_{CC1}‡§	Read- or write-cycle current	V_{CC} = 5.5 V, Minimum cycle		180		170	mA
I_{CC2}	Standby current	V_{IH} = 2.4 V (TTL), After one memory cycle, $\overline{RAS}$ and $\overline{xCAS}$ high		2		2	mA
		V_{IH} = V_{CC} – 0.2 V (CMOS), After one memory cycle, $\overline{RAS}$ and $\overline{xCAS}$ high		1		1	mA
I_{CC3}§	Average refresh current ($\overline{RAS}$ only refresh or CBR)	$\overline{V_{CC}}$ = 5.5 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{xCAS}$ high ($\overline{RAS}$ only), $\overline{RAS}$ low after $\overline{xCAS}$ low (CBR)		180		170	mA
I_{CC4}‡¶	Average page current	$\overline{V_{CC}}$ = 5.5 V, t_{PC} = MIN, $\overline{RAS}$ low, $\overline{xCAS}$ cycling		180		170	mA
I_{CC7}‡¶	Standby current, outputs enabled	$\overline{RAS}$ = V_{IH}, $\overline{xCAS}$ = V_{IL}, Data out = enabled		5		5	mA

† For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.
‡ Measured with outputs open
§ Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
¶ Measured with a maximum of one address change while $\overline{xCAS}$ = V_{IH}

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 3)

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, A0–A11#		8	pF
$C_{i(OE)}$	Input capacitance, $\overline{OE}$		8	pF
$C_{i(RC)}$	Input capacitance, $\overline{xCAS}$ and $\overline{RAS}$		8	pF
$C_{i(W)}$	Input capacitance, $\overline{W}$		8	pF
C_o	Output capacitance		10	pF

A10 and A11 are NC for SMJ418160.

NOTE 3: Capacitance is sampled only at initial design and after any major changes. Samples are tested at 0 V and 25°C with a 1-MHz signal applied to the pin under test. All other pins are open.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Note 4)

PARAMETER		'41x160-70		'41x160-80		UNIT
		MIN	MAX	MIN	MAX	
t_{AA}	Access time from column address		35		40	ns
t_{CAC}	Access time from $\overline{xCAS}$ low		18		20	ns
t_{CPA}	Access time from column precharge		40		45	ns
t_{RAC}	Access time from $\overline{RAS}$ low		70		80	ns
t_{OEA}	Access time from $\overline{OE}$ low		18		20	ns
t_{OFF}	Output disable time after $\overline{xCAS}$ high (see Note 5)	0	18	0	20	ns
t_{OEZ}	Output disable time after $\overline{OE}$ high (see Note 5)	0	18	0	20	ns

NOTES: 4. Valid data is presented at the outputs after all access times are satisfied but can go from the high-impedance state to an invalid-data state prior to the specified access time as the outputs are driven when $\overline{xCAS}$ and $\overline{OE}$ are low.
5. t_{OFF} and t_{OEZ} are specified when the output is no longer driven. The outputs are disabled by bringing either $\overline{OE}$ or $\overline{xCAS}$ high.

timing requirements

		'41x160-70		'41x160-80		UNIT
		MIN	MAX	MIN	MAX	
t_{RC}	Cycle time, read (see Note 6)	130		150		ns
t_{WC}	Cycle time, write (see Note 6)	130		150		ns
t_{RWC}	Cycle time, read-write (see Note 6)	181		205		ns
t_{PC}	Cycle time, page-mode read or write (see Notes 6 and 7)	45		50		ns
t_{PRWC}	Cycle time, page-mode read-write (see Note 6)	96		105		ns
t_{RASP}	Pulse duration, $\overline{RAS}$ low, page mode (see Note 8)	70	100 000	80	100 000	ns
t_{RAS}	Pulse duration, $\overline{RAS}$ low, nonpage mode (see Note 8)	70	10 000	80	10 000	ns
t_{CAS}	Pulse duration, $\overline{xCAS}$ low (see Note 9)	18	10 000	20	10 000	ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	50		60		ns
t_{WP}	Pulse duration, $\overline{W}$ low	10		10		ns
t_{ASC}	Setup time, column address before $\overline{xCAS}$ going low	0		0		ns
t_{ASR}	Setup time, row address before $\overline{RAS}$ going low	0		0		ns
t_{DS}	Setup time, data (see Note 10)	0		0		ns
t_{RCS}	Setup time, $\overline{W}$ high before $\overline{xCAS}$ going low	0		0		ns
t_{CWL}	Setup time, $\overline{W}$ low before $\overline{xCAS}$ going high	18		20		ns
t_{RWL}	Setup time, $\overline{W}$ low before $\overline{RAS}$ going high	18		20		ns
t_{WCS}	Setup time, $\overline{W}$ low before $\overline{xCAS}$ going low (early-write operation only)	0		0		ns
t_{CAH}	Hold time, column address after $\overline{xCAS}$ low	15		15		ns
t_{DH}	Hold time, data (see Note 10)	15		15		ns
t_{RAH}	Hold time, row address after $\overline{RAS}$ low	10		10		ns
t_{RCH}	Hold time, $\overline{W}$ high after $\overline{xCAS}$ high (see Note 11)	0		0		ns
t_{RRH}	Hold time, $\overline{W}$ high after $\overline{RAS}$ high (see Note 11)	0		0		ns
t_{WCH}	Hold time, $\overline{W}$ low after $\overline{xCAS}$ low (early-write operation only)	15		15		ns

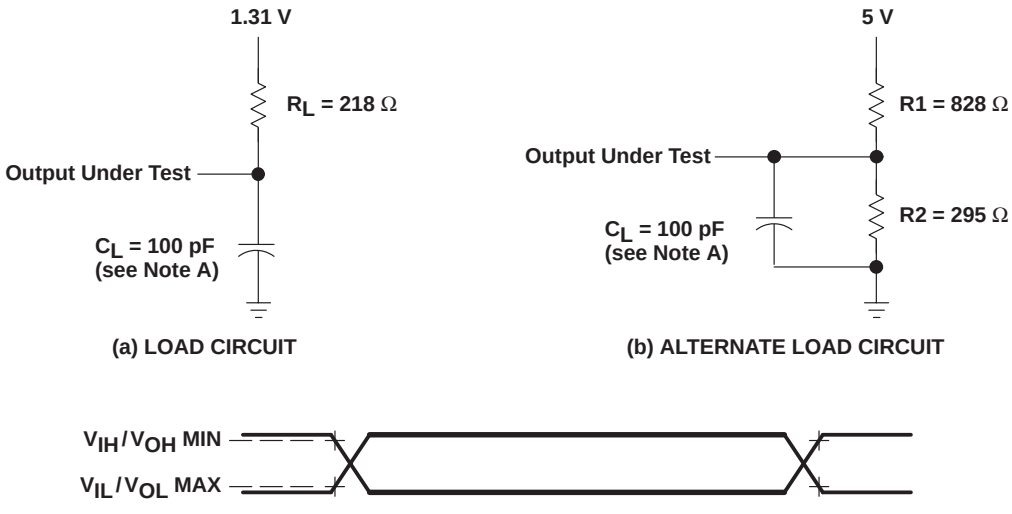
NOTES: 6. All cycle times assume t_T = 5 ns, referenced to $V_{IH(MIN)}$ and $V_{IL(MAX)}$.
7. To assure t_{PC} min, t_{ASC} should be ≥ to t_{CP}.
8. In a read-write cycle, t_{RWD} and t_{RWL} must be observed.
9. In a read-write cycle, t_{CWD} and t_{CWL} must be observed.
10. Referenced to the later of $\overline{xCAS}$ or $\overline{W}$ in write operations
11. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

timing requirements (continued)

			'41x160-70		'41x160-80		UNIT
			MIN	MAX	MIN	MAX	
t_{CLCH}	Hold time, $\overline{xCAS}$ low to $\overline{xCAS}$ going high		5		5		ns
t_{RHCP}	Hold time, $\overline{RAS}$ low after $\overline{xCAS}$ precharge		40		45		ns
t_{OEH}	Hold time, $\overline{OE}$ command		18		20		ns
t_{ROH}	Hold time, $\overline{RAS}$ referenced to $\overline{OE}$		10		10		ns
t_{CP}	Delay time, $\overline{xCAS}$ high (precharge)		10		10		ns
t_{AWD}	Delay time, column address to $\overline{W}$ going low (read-write operation only)		63		70		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{xCAS}$ going high (CBR refresh only)		10		10		ns
t_{CRP}	Delay time, $\overline{xCAS}$ high to $\overline{RAS}$ going low		5		5		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{xCAS}$ going high		70		80		ns
t_{CSR}	Delay time, $\overline{xCAS}$ low to $\overline{RAS}$ going low (CBR refresh only)		5		5		ns
t_{CWD}	Delay time, $\overline{xCAS}$ low to $\overline{W}$ going low (read-write operation only)		46		50		ns
t_{OED}	Delay time, $\overline{OE}$ to data		18		20		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column address (see Note 12)		15	35	15	40	ns
t_{RAL}	Delay time, column address to $\overline{RAS}$ going high		35		40		ns
t_{CAL}	Delay time, column address to $\overline{xCAS}$ going high		35		40		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{xCAS}$ low (see Note 12)		20	52	20	60	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{xCAS}$ going low		0		0		ns
t_{RSH}	Delay time, $\overline{xCAS}$ low to $\overline{RAS}$ going high		18		20		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ going low (read-write operation only)		98		110		ns
t_{CPW}	Delay time, $\overline{W}$ going low after $\overline{xCAS}$ precharge (read-write operation only)		68		75		ns
t_{REF}	Refresh time interval	'416160		32		32	ms
		'418160		8		8	
t_T	Transition time (see Note 13)		3	30	3	30	ns

NOTES: 12. The maximum value is specified only to ensure access time.
13. Transition times (rise and fall) should be a minimum of 3 ns and a maximum of 30 ns. This is ensured by design but not tested.

PARAMETER MEASUREMENT INFORMATION



(a) LOAD CIRCUIT

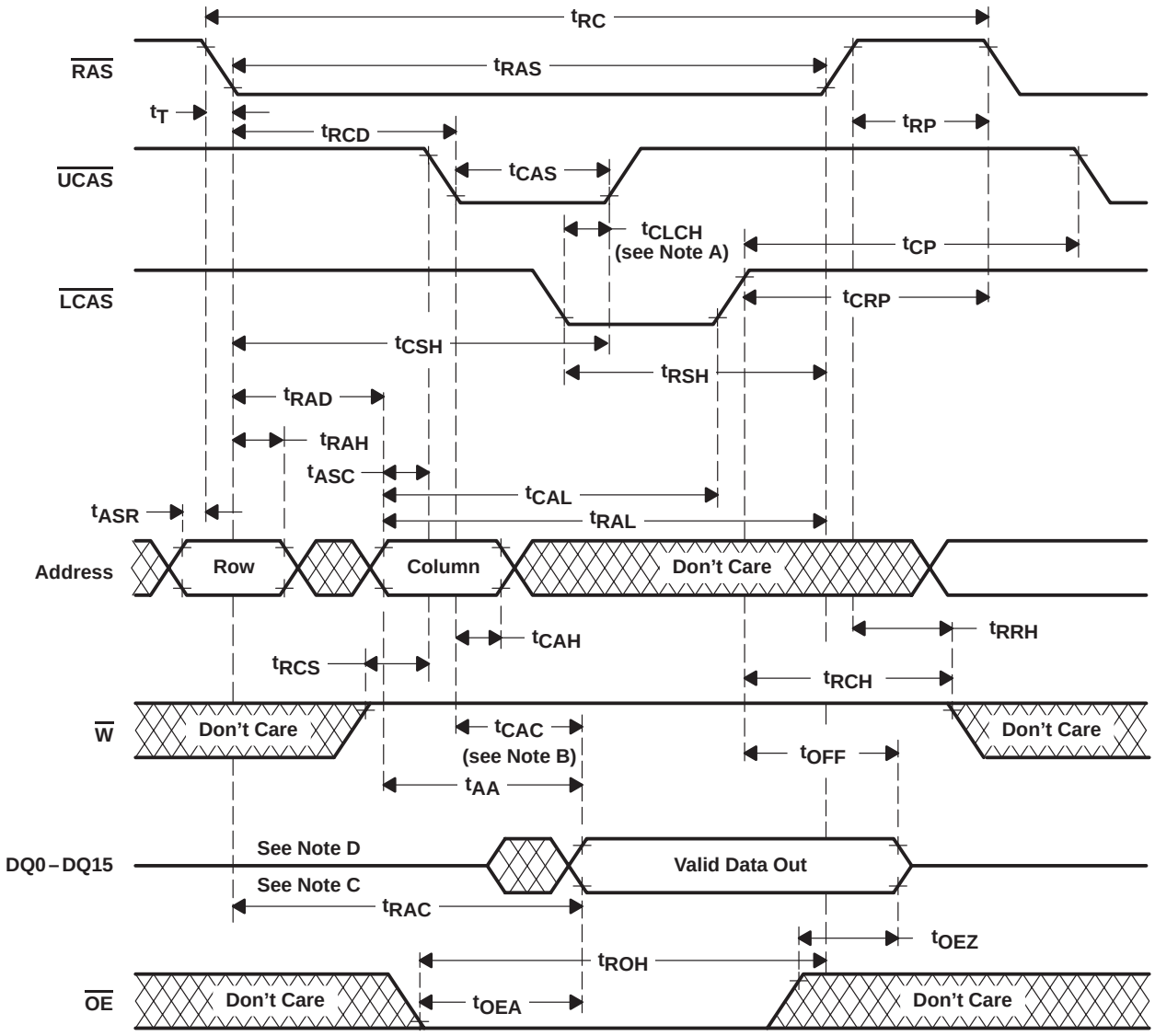
(b) ALTERNATE LOAD CIRCUIT

(c) VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and fixture capacitance.
B. The ac timing parameters are specified with reference to the minimum valid high-level voltage and the maximum valid low-level voltage for each signal. This corresponds to 2.4 V and 0.8 V for inputs; 2.4 V and 0.4 V for outputs with the given load circuit.

Figure 1. Load Circuits and Voltage Waveforms

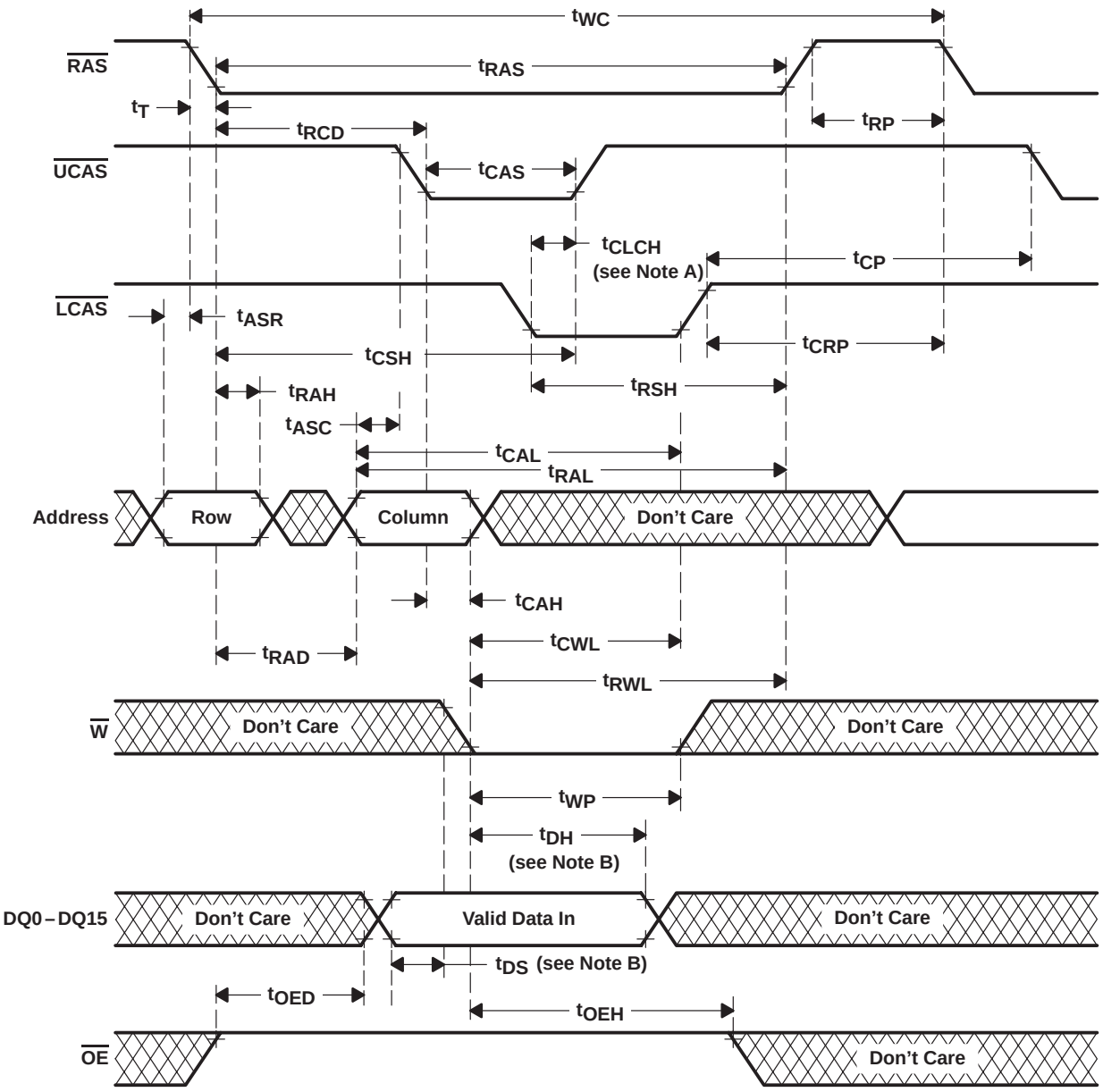
PARAMETER MEASUREMENT INFORMATION



NOTES: A. To hold the address latched by the first $\overline{\text{xCAS}}$ going low, the parameter t_{CLCH} must be met.
B. t_{CAC} is measured from $\overline{\text{xCAS}}$ to its corresponding DQx.
C. Output can go from the high-impedance state to an invalid-data state prior to the specified access time.
D. $\overline{\text{xCAS}}$ order is arbitrary.

Figure 2. Read-Cycle Timing

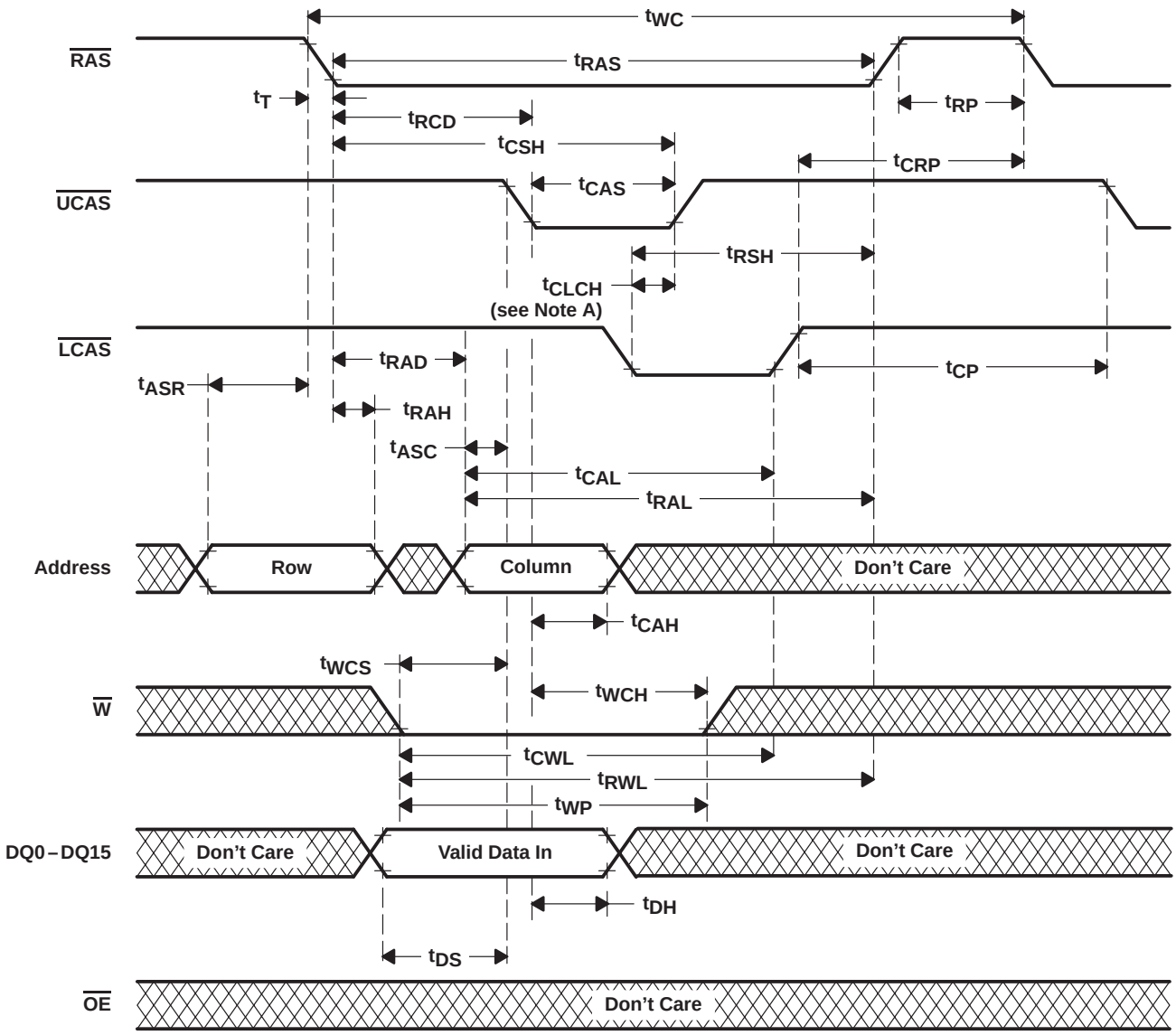
PARAMETER MEASUREMENT INFORMATION



NOTES: A. To hold the address latched by the first $\overline{\text{xCAS}}$ going low, the parameter t_{CLCH} must be met.
B. Referenced to the first $\overline{\text{xCAS}}$ or $\overline{\text{W}}$, whichever occurs last
C. $\overline{\text{xCAS}}$ order is arbitrary.

Figure 3. Write-Cycle Timing

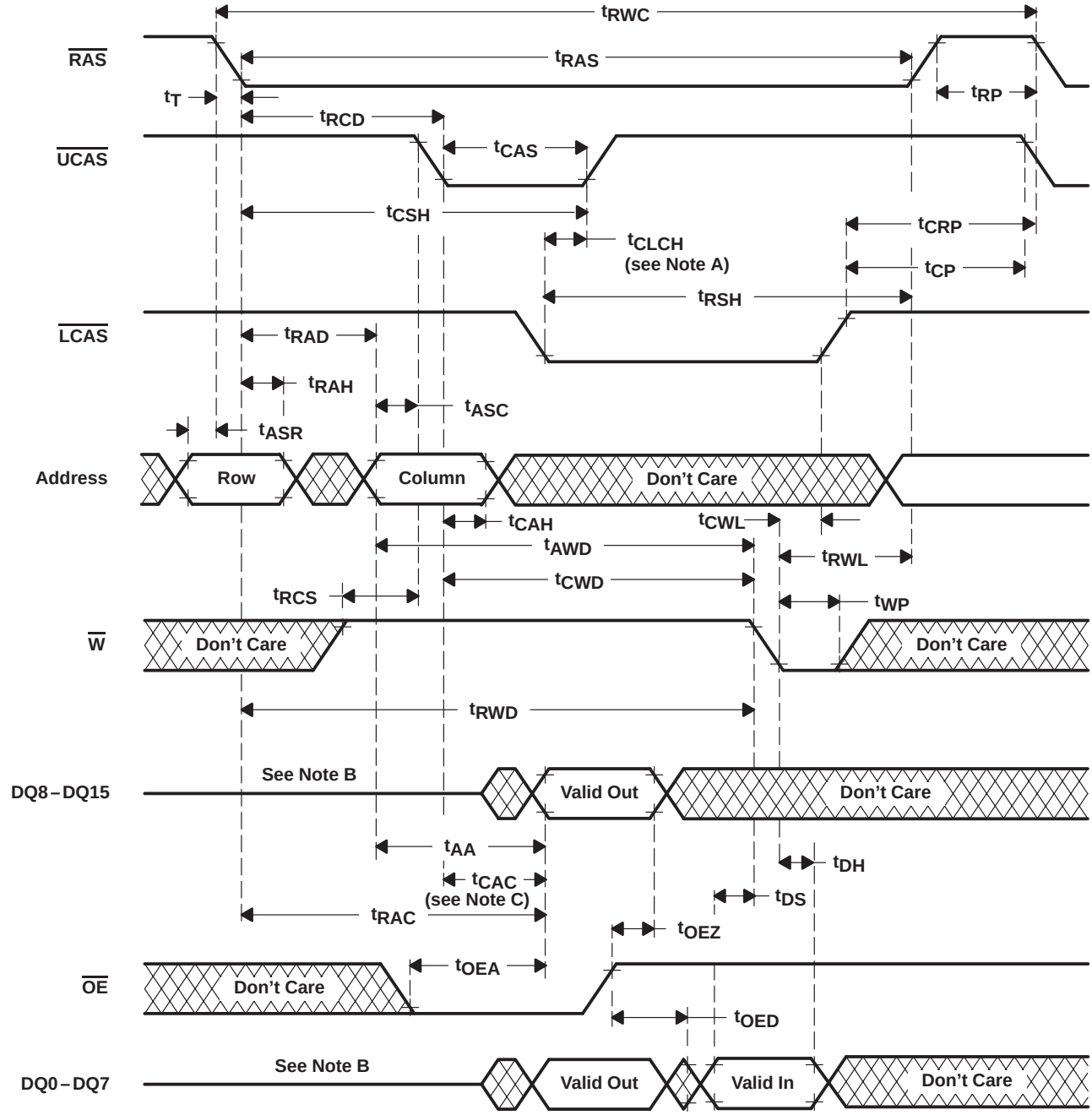
PARAMETER MEASUREMENT INFORMATION



NOTES: A. To hold the address latched by the first xCAS going low, the parameter t_{CLCH} must be met.
B. xCAS order is arbitrary.

Figure 4. Early-Write-Cycle Timing

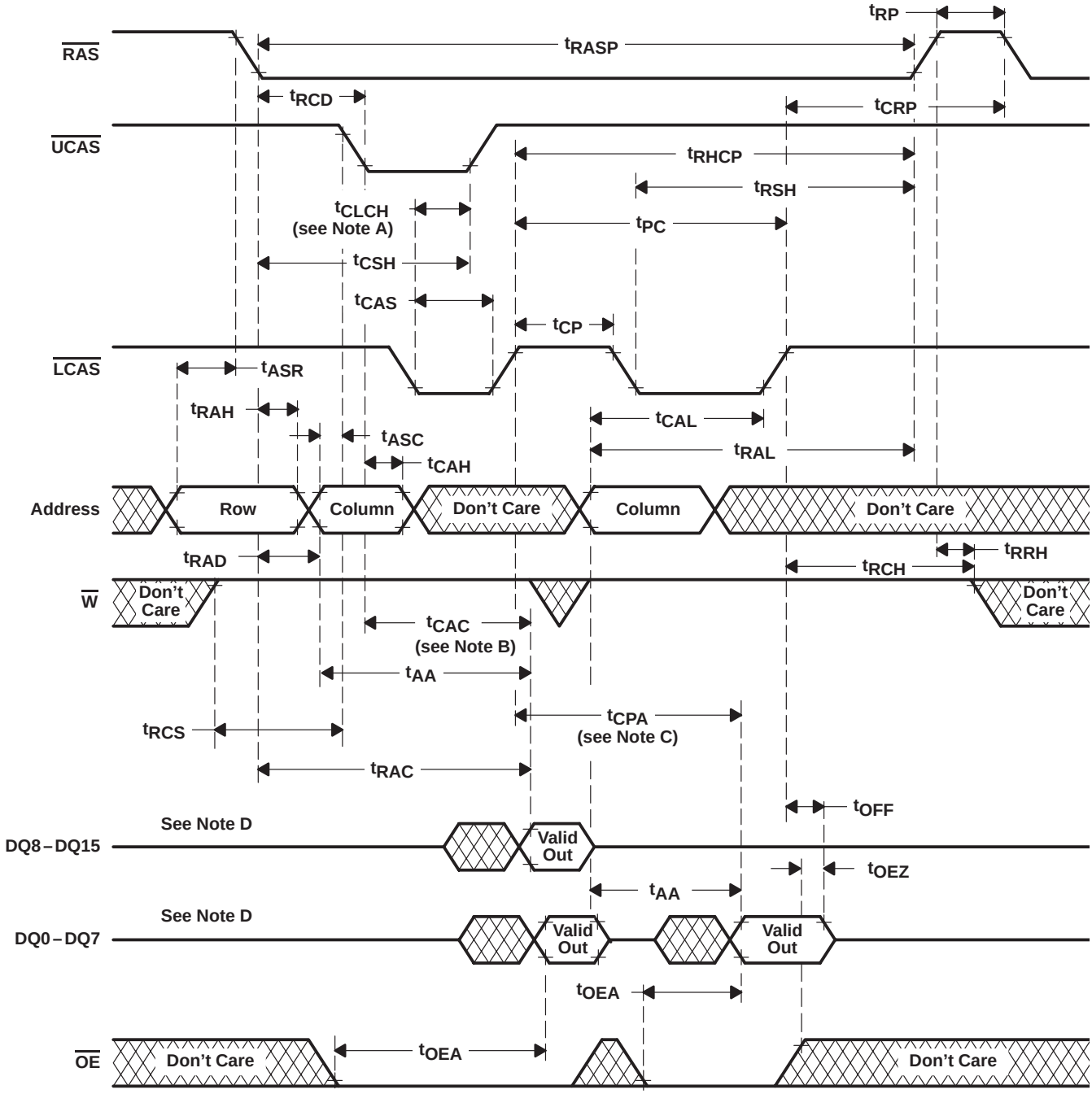
PARAMETER MEASUREMENT INFORMATION



NOTES: A. To hold the address latched by the first xCAS going low, the parameter t_{CLCH} must be met.
B. Output can go from the high-impedance state to an invalid-data state prior to the specified access time.
C. t_{CAC} is measured from xCAS to its corresponding DQx.
D. xCAS order is arbitrary.

Figure 5. Read-Modify-Write-Cycle Timing

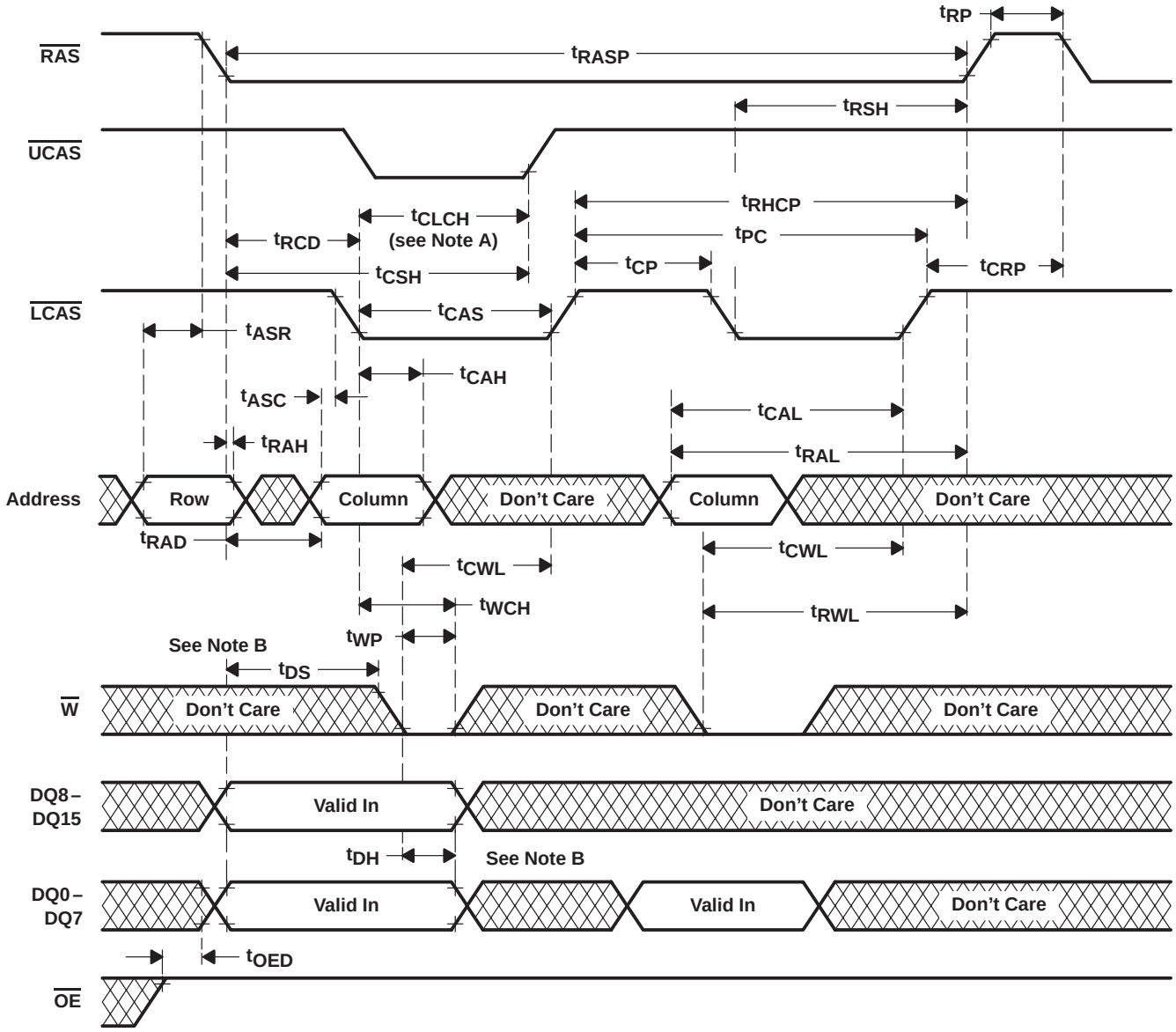
PARAMETER MEASUREMENT INFORMATION



NOTES: A. To hold the address latched by the first $\overline{\text{xCAS}}$ going low, the parameter t_{CLCH} must be met.
B. t_{CAC} is measured from $\overline{\text{xCAS}}$ to its corresponding DQx.
C. Access time is t_{CPA}- or t_{AA}-dependent.
D. Output can go from the high-impedance state to an invalid-data state prior to the specified access time.
E. A write cycle or read-modify-write cycle can be mixed with the read cycles as long as the write- and read-modify-write timing specifications are not violated.
F. $\overline{\text{xCAS}}$ order is arbitrary.

Figure 6. Enhanced-Page-Mode Read-Cycle Timing

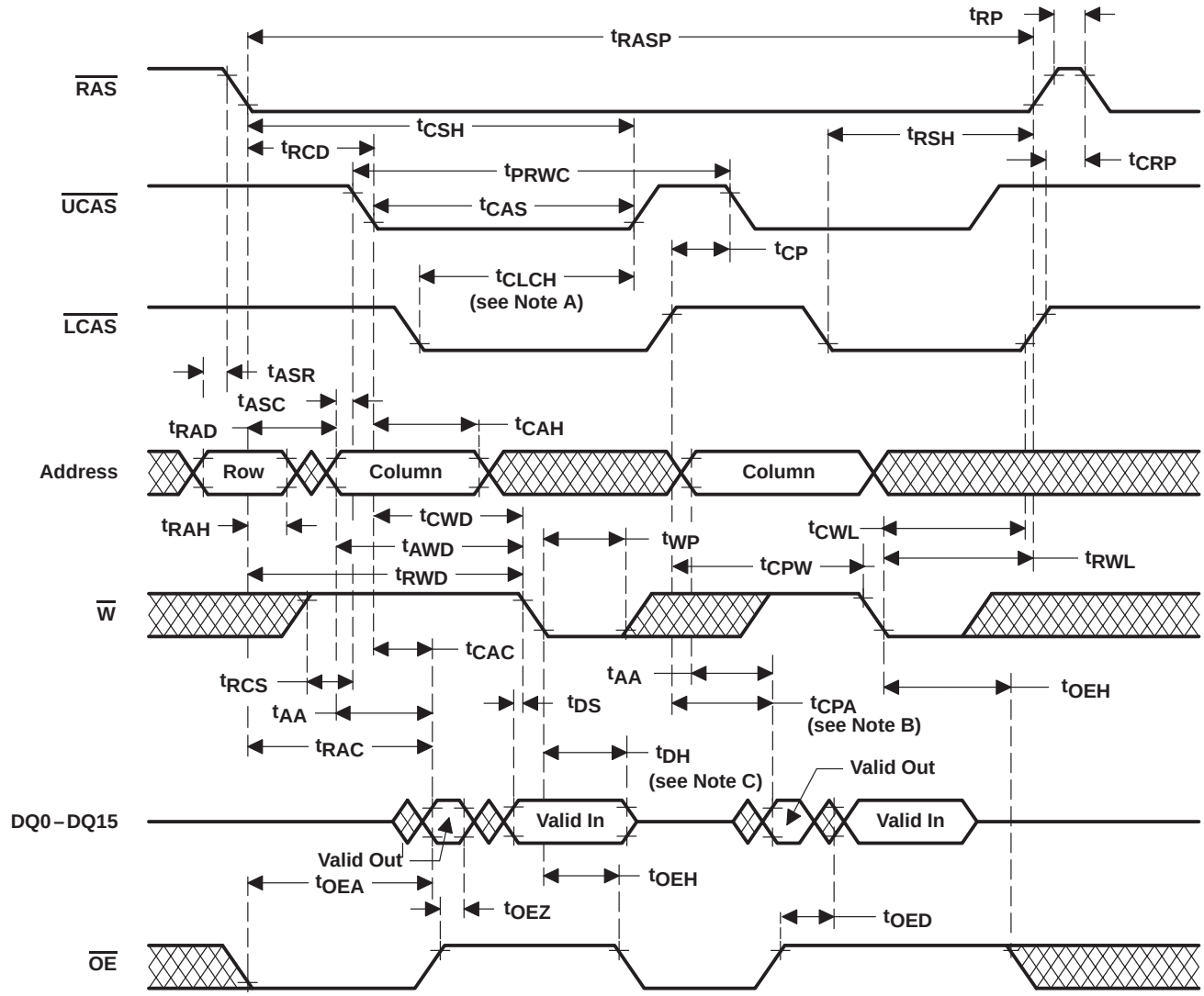
PARAMETER MEASUREMENT INFORMATION



NOTES: A. To hold the address latched by the first xCAS going low, the parameter t_{CLCH} must be met.
B. Referenced to the first xCAS or W, whichever occurs last
C. A read cycle or read-modify-write cycle can be mixed with the write cycles as long as the read- and read-modify-write timing specifications are not violated.
D. xCAS order is arbitrary.

Figure 7. Enhanced-Page-Mode Write-Cycle Timing

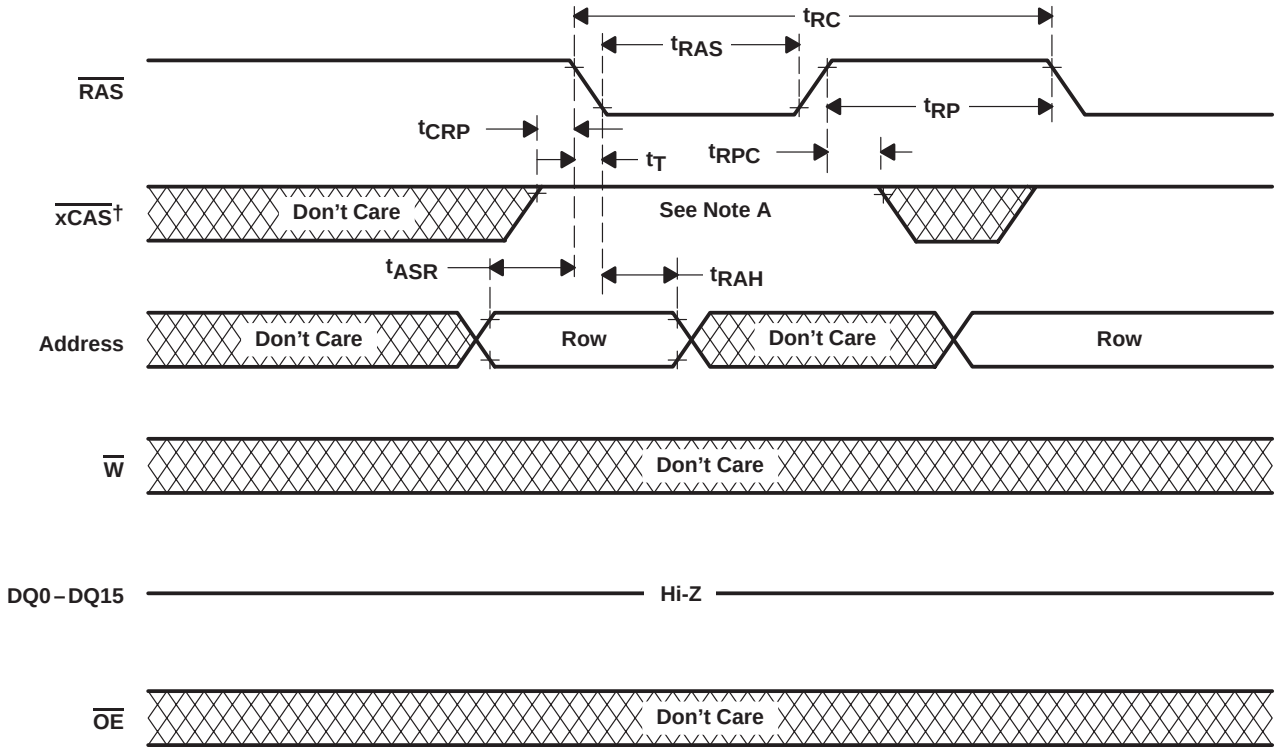
PARAMETER MEASUREMENT INFORMATION



NOTES: A. To hold the address latched by the first $\overline{\text{xCAS}}$ going low, the parameter t_{CLCH} must be met.
B. Access time is t_{CPA}- or t_{AA}-dependent.
C. Output can go from the high-impedance state to an invalid-data state prior to the specified access time.
D. $\overline{\text{xCAS}}$ order is arbitrary.
E. A read or write cycle can be intermixed with read-modify-write cycles as long as the read- and write-cycle timing specifications are not violated.
F. t_{CAC} is measured from $\overline{\text{xCAS}}$ to its corresponding DQx.

Figure 8. Enhanced-Page-Mode Read-Modify-Write-Cycle Timing

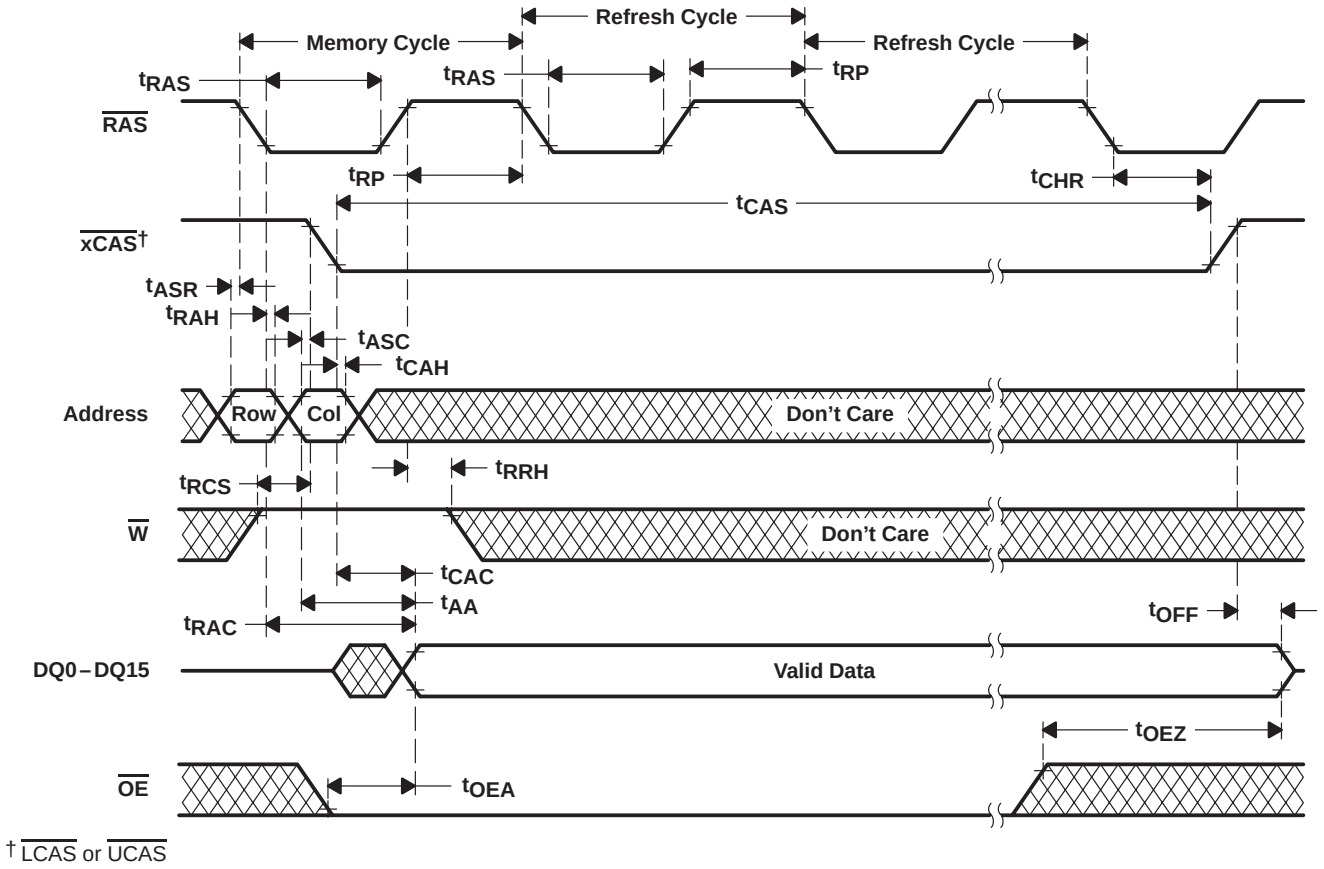
PARAMETER MEASUREMENT INFORMATION



† $\overline{\text{LCAS}}$ or $\overline{\text{UCAS}}$
NOTE A: All xCAS must be high.

Figure 9. $\overline{\text{RAS}}$-Only Refresh-Cycle Timing

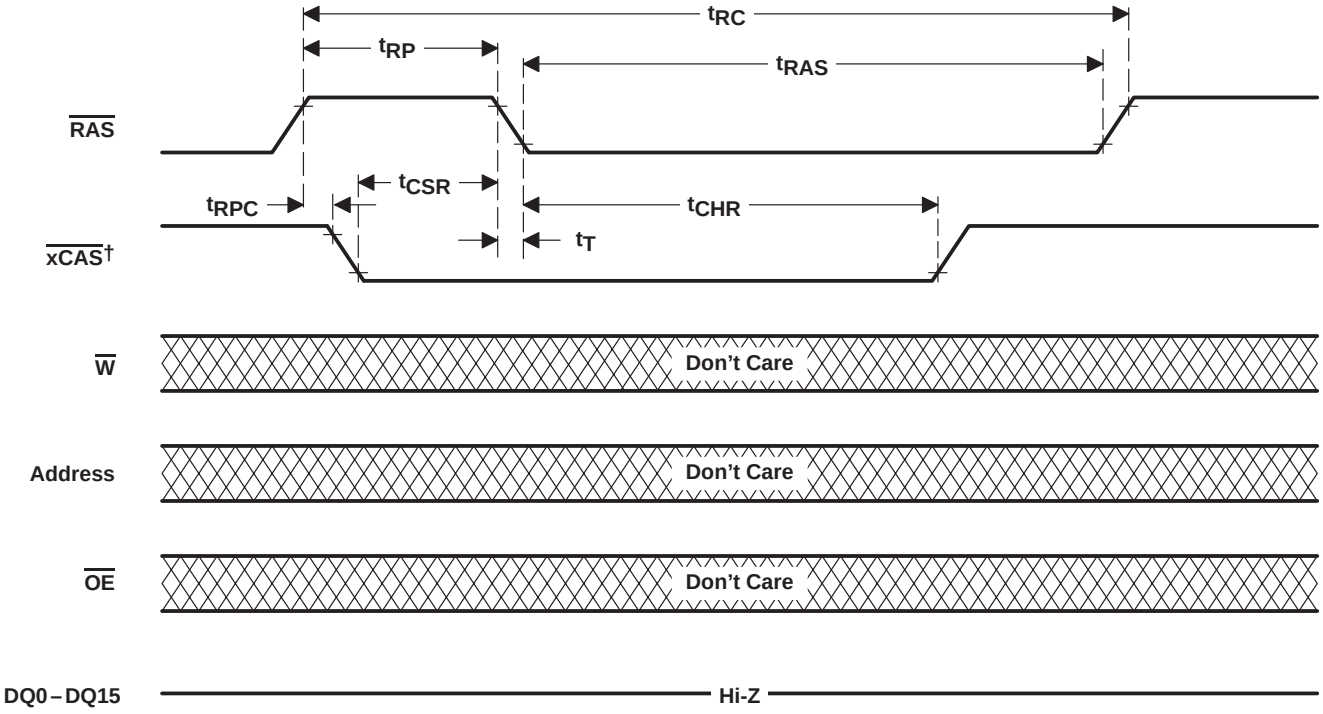
PARAMETER MEASUREMENT INFORMATION



† $\overline{\text{LCAS}}$ or $\overline{\text{UCAS}}$

Figure 10. Hidden-Refresh-Cycle Timing

PARAMETER MEASUREMENT INFORMATION



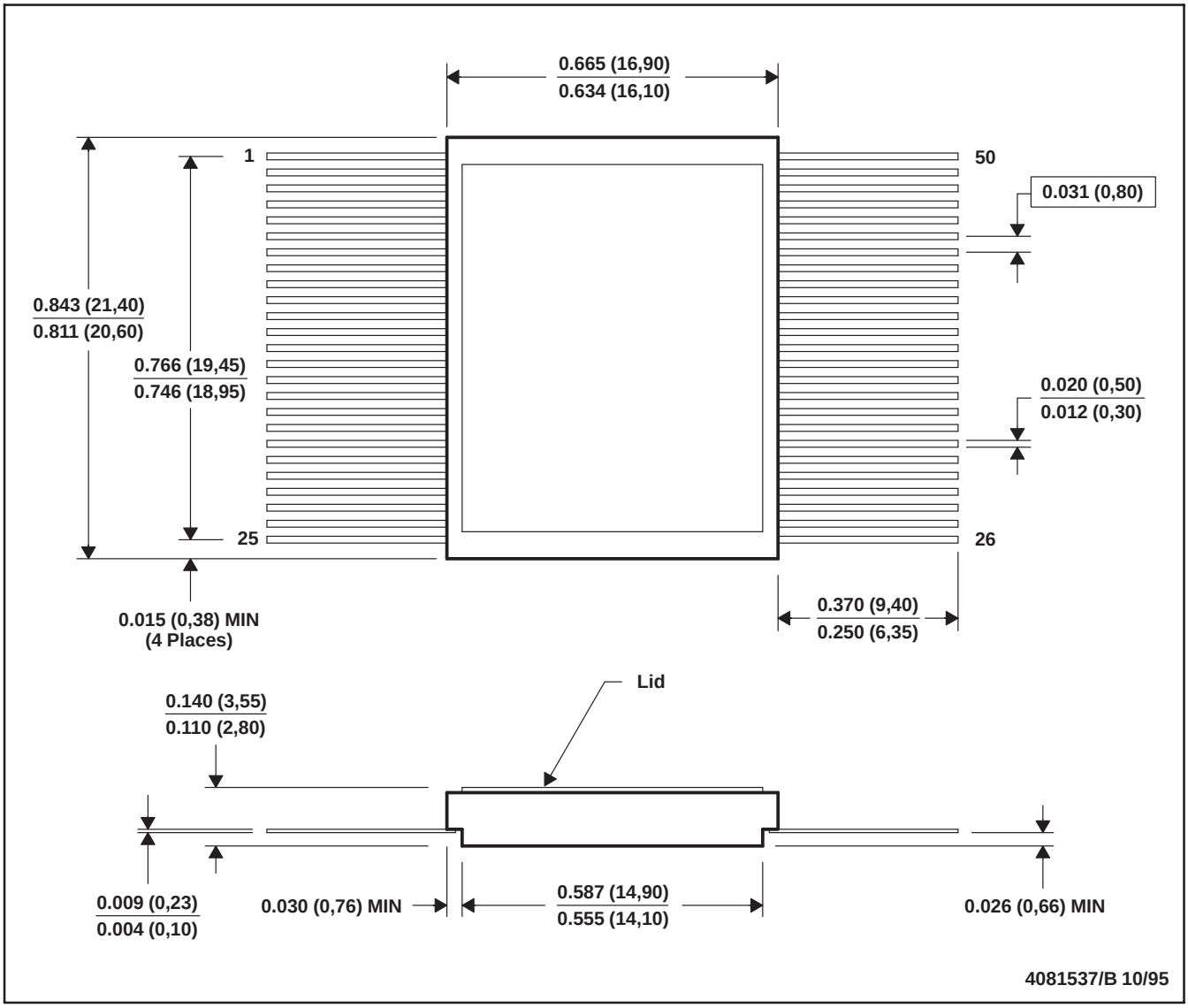
† $\overline{\text{LCAS}}$ or $\overline{\text{UCAS}}$

NOTE A: Any $\overline{\text{xCAS}}$ can be used.

Figure 11. Automatic-xCBR-Refresh-Cycle Timing

MECHANICAL DATA

HKD (R-CDFP-F50) **CERAMIC DUAL FLATPACK**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. The leads will be gold plated.

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