

# AZ10EL31 AZ100EL31

## ECL/PECL D Flip-Flop with Set and Reset

### FEATURES

- 475ps Propagation Delay
- 2.8GHz Toggle Frequency
- 75kΩ Internal Input Pulldown Resistors
- Direct Replacement for ON Semiconductor MC10EL31 & MC100EL31

### PACKAGE AVAILABILITY

PACKAGE	PART NO.	MARKING
SOIC 8	AZ10EL31D	AZM10EL31
SOIC 8 T&R	AZ10EL31DR1	AZM10EL31
SOIC 8 T&R	AZ10EL31DR2	AZM10EL31
SOIC 8	AZ100EL31D	AZM100EL31
SOIC 8 T&R	AZ100EL31DR1	AZM100EL31
SOIC 8 T&R	AZ100EL31DR2	AZM100EL31
TSSOP 8	AZ10EL31T	AZTEL31
TSSOP 8 T&R	AZ10EL31TR1	AZTEL31
TSSOP 8 T&R	AZ10EL31TR2	AZTEL31
TSSOP 8	AZ100EL31T	AZHTEL31
TSSOP 8 T&R	AZ100EL31TR1	AZHTEL31
TSSOP 8 T&R	AZ100EL31TR2	AZHTEL31

### DESCRIPTION

The AZ10/100EL31 is a master-slave D flip-flop with set and reset. The device is functionally equivalent to the E131 device with higher performance capabilities. With propagation delays and output transition times significantly faster than the E131, the EL31 is ideally suited for those applications that require the ultimate in AC performance.

Both set and reset inputs are asynchronous, level triggered signals. Data enters the master section of the flip-flop when the clock is LOW. When the clock transitions from LOW to HIGH, the data in the master section transfers into the slave section and through to the outputs.

NOTE: Specifications in ECL/PECL tables are valid when thermal equilibrium is established.

### TRUTH TABLE

D	S*	R*	CLK	Q	$\bar{Q}$
L	L	L	Z	L	H
H	L	L	Z	H	L
X	H	L	X	H	L
X	L	H	X	L	H
X	H	H	X	Undef	Undef

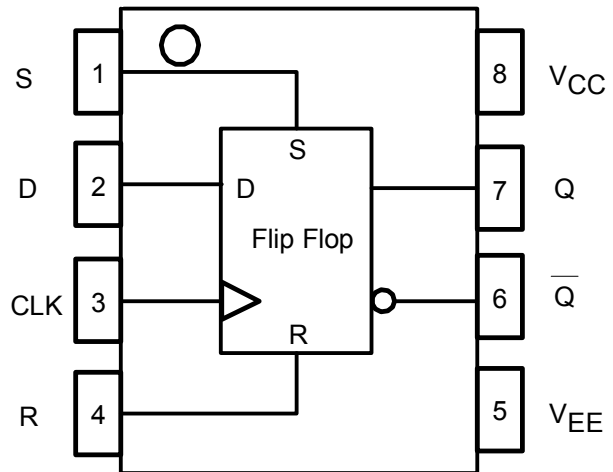
Z = LOW to HIGH Transition

\* Pins will default low when left open

### PIN DESCRIPTION

PIN	FUNCTION
S	Set Input
D	Data Input
R	Reset Input
CLK	Clock Input
Q, $\bar{Q}$	Data Outputs
V <sub>CC</sub>	Positive Supply
V <sub>EE</sub>	Negative Supply

### LOGIC DIAGRAM AND PINOUT ASSIGNMENT



# AZ10EL31

## AZ100EL31

**Absolute Maximum Ratings are those values beyond which device life may be impaired.**

Symbol	Characteristic	Rating	Unit
$V_{CC}$	PECL Power Supply ( $V_{EE} = 0V$ )	0 to +8.0	Vdc
$V_I$	PECL Input Voltage ( $V_{EE} = 0V$ )	0 to +6.0	Vdc
$V_{EE}$	ECL Power Supply ( $V_{CC} = 0V$ )	-8.0 to 0	Vdc
$V_I$	ECL Input Voltage ( $V_{CC} = 0V$ )	-6.0 to 0	Vdc
$I_{OUT}$	Output Current --- Continuous --- Surge	50 100	mA
$T_A$	Operating Temperature Range	-40 to +85	°C
$T_{STG}$	Storage Temperature Range	-65 to +150	°C

### 10K ECL DC Characteristics ( $V_{EE} = -4.75$ to $-5.5V$ , $V_{CC} = GND$ )

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$V_{OH}$	Output HIGH Voltage <sup>1</sup>	-1080		-890	-1020		-840	-980		-810	-910		-720	mV
$V_{OL}$	Output LOW Voltage <sup>1</sup>	-1950		-1650	-1950		-1630	-1950		-1630	-1950		-1595	mV
$V_{IH}$	Input HIGH Voltage	-1230		-890	-1170		-840	-1130		-810	-1060		-720	mV
$V_{IL}$	Input LOW Voltage	-1950		-1500	-1950		-1480	-1950		-1480	-1950		-1445	mV
$I_{IH}$	Input HIGH Current D, CLK S, R			150 300			150 300			150 300			150 300	μA
$I_{IL}$	Input LOW Current	0.5			0.5			0.5			0.5			μA
$I_{EE}$	Power Supply Current		27	32		27	32		27	32		27	32	mA

- Each output is terminated through a 50Ω resistor to  $V_{CC} - 2V$ .

### 10K PECL DC Characteristics ( $V_{EE} = GND$ , $V_{CC} = +5.0V$ )

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$V_{OH}$	Output HIGH Voltage <sup>1,2</sup>	3920		4110	3980		4160	4020		4190	4090		4280	mV
$V_{OL}$	Output LOW Voltage <sup>1,2</sup>	3050		3350	3050		3370	3050		3370	3050		3405	mV
$V_{IH}$	Input HIGH Voltage <sup>1</sup>	3770		4110	3830		4160	3870		4190	3940		4280	mV
$V_{IL}$	Input LOW Voltage <sup>1</sup>	3050		3500	3050		3520	3050		3520	3050		3555	mV
$I_{IH}$	Input HIGH Current D, CLK S, R			150 300			150 300			150 300			150 300	μA
$I_{IH}$	Input HIGH Current			150			150			150			150	μA
$I_{IL}$	Input LOW Current	0.5			0.5			0.5			0.5			μA
$I_{EE}$	Power Supply Current		27	32		27	32		27	32		27	32	mA

- For supply voltages other than 5.0V, use the ECL table values and ADD supply voltage value.
- Each output is terminated through a 50Ω resistor to  $V_{CC} - 2V$ .

### 100K ECL DC Characteristics ( $V_{EE} = -4.2V$ to $-5.5V$ , $V_{CC} = GND$ )

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$V_{OH}$	Output HIGH Voltage <sup>1</sup>	-1085	-1005	-880	-1025	-955	-880	-1025	-955	-880	-1025	-955	-880	mV
$V_{OL}$	Output LOW Voltage <sup>1</sup>	-1830	-1695	-1555	-1810	-1705	-1620	-1810	-1705	-1620	-1810	-1705	-1620	mV
$V_{IH}$	Input HIGH Voltage	-1165		-880	-1165		-880	-1165		-880	-1165		-880	mV
$V_{IL}$	Input LOW Voltage	-1810		-1475	-1810		-1475	-1810		-1475	-1810		-1475	mV
$I_{IH}$	Input HIGH Current D, CLK S, R			150 300			150 300			150 300			150 300	μA
$I_{IH}$	Input HIGH Current			150			150			150			150	μA
$I_{IL}$	Input LOW Current	0.5			0.5			0.5			0.5			μA
$I_{EE}$	Power Supply Current		27	32		27	32		27	32		31	37	mA

- Each output is terminated through a 50Ω resistor to  $V_{CC} - 2V$ .

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**100K PECL DC Characteristics** ( $V_{EE} = \text{GND}$ ,  $V_{CC} = +5.0\text{V}$ )

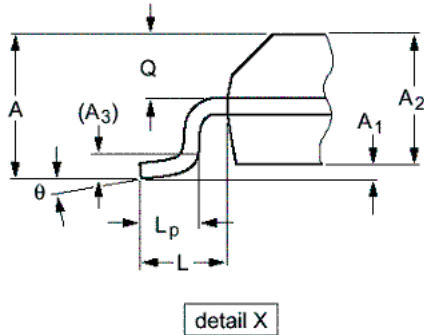
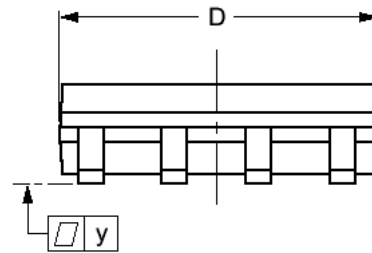
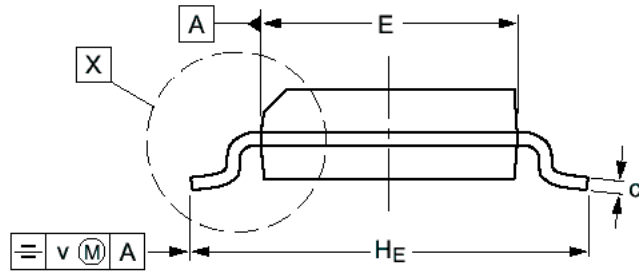
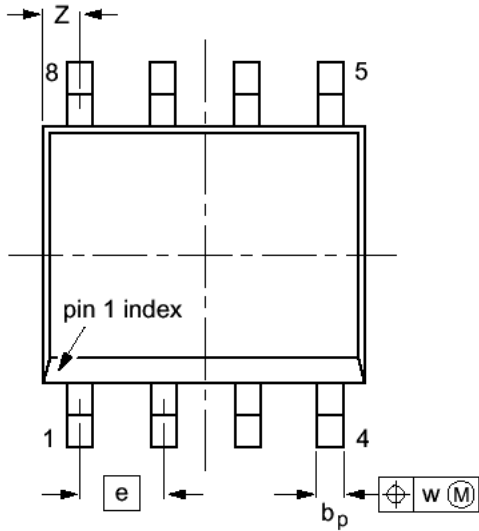
Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$V_{OH}$	Output HIGH Voltage <sup>1,2</sup>	3915	3995	4120	3975	4045	4120	3975	4045	4120	3975	4045	4120	mV
$V_{OL}$	Output LOW Voltage <sup>1,2</sup>	3170	3305	3445	3190	3295	3380	3190	3295	3380	3190	3295	3380	mV
$V_{IH}$	Input HIGH Voltage <sup>1</sup>	3835		4120	3835		4120	3835		4120	3835		4120	mV
$V_{IL}$	Input LOW Voltage <sup>1</sup>	3190		3525	3190		3525	3190		3525	3190		3525	mV
$I_{IH}$	Input HIGH Current D, CLK S, R			150 300			150 300			150 300			150 300	μA
$I_{IH}$	Input HIGH Current			150			150			150			150	μA
$I_{IL}$	Input LOW Current	0.5			0.5			0.5			0.5			μA
$I_{EE}$	Power Supply Current		27	32		27	32		27	32		31	37	mA

- For supply voltages other than 5.0V, use the ECL table values and ADD supply voltage value.
- Each output is terminated through a 50Ω resistor to  $V_{CC} - 2\text{V}$ .

**AC Characteristics** ( $V_{EE} = 10\text{E}(-4.75\text{V to } -5.5\text{V})$ ,  $100\text{E}(-4.2\text{V to } -5.5\text{V})$ ;  $V_{CC} = \text{GND}$  or  $V_{EE} = \text{GND}$ ;  $V_{CC} = 10\text{E}(+4.75\text{V to } +5.5\text{V})$ ,  $100\text{E}(+4.2\text{V to } +5.5\text{V})$ )

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{MAX}$	Maximum Toggle Frequency	2.0	2.5		2.2	2.8		2.2	2.8		2.2	2.8		GHz
$t_{PLH} / t_{PHL}$	Propagation Delay to Output CLK S,R	315 295	465 455	630 630	365 345	465 455	580 580	375 355	475 465	590 590	430 400	530 510	645 645	ps
$t_S$	Setup Time	150	0		150	0		150	0		150	0		ps
$t_H$	Hold Time	250	100		250	100		250	100		250	100		ps
$t_{RR}$	Set/Reset Recovery	400	200		400	200		400	200		400	200		ps
$t_{PW}$	Minimum Pulse Width CLK, Set, Reset	400			400			400			400			ps
$t_r / t_f$	Output Rise/Fall Times Q (20% - 80%)	100		350	100		350	100		350	100		350	ps

**PACKAGE DIAGRAM  
SOIC 8**



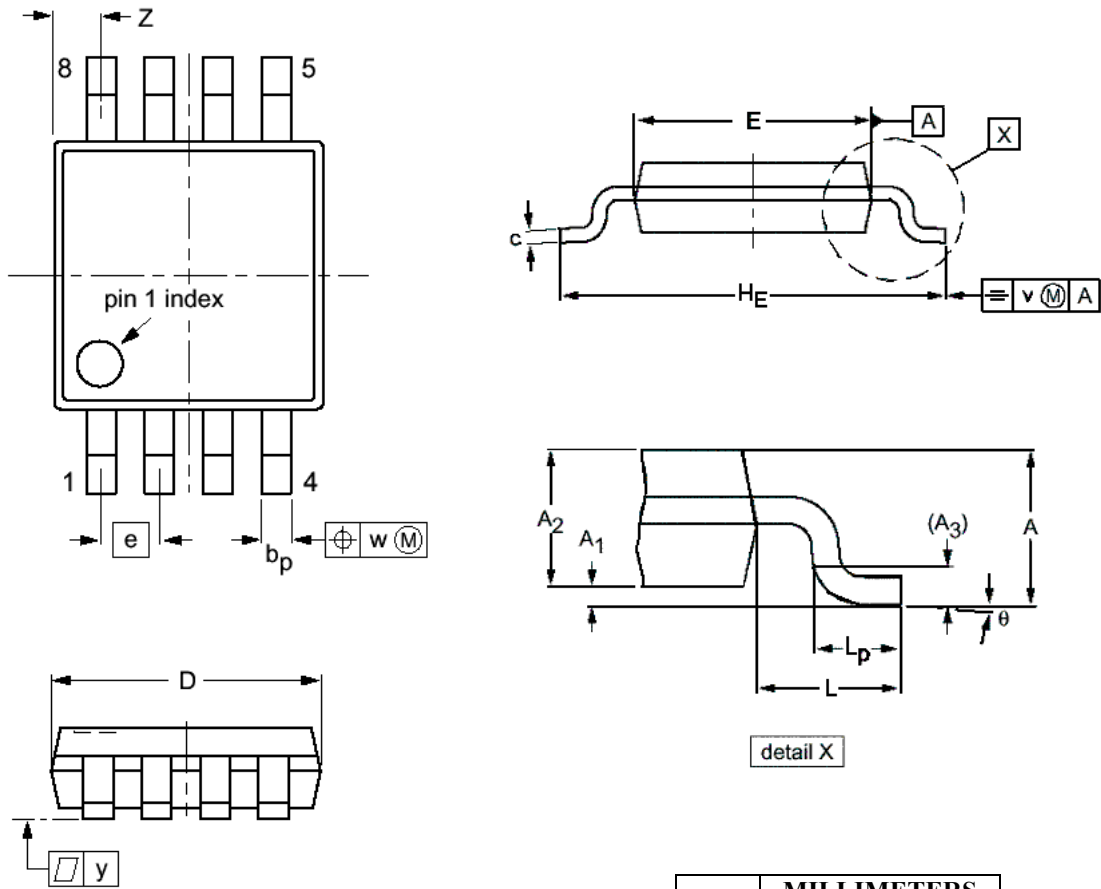
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A		1.75		0.069
A <sub>1</sub>	0.10	0.25	0.004	0.010
A <sub>2</sub>	1.25	1.45	0.049	0.057
A <sub>3</sub>	0.25		0.01	
b <sub>p</sub>	0.36	0.49	0.014	0.019
c	0.19	0.25	0.0075	0.0100
D	4.8	5.0	0.19	0.20
E	3.8	4.0	0.15	0.16
e	1.27		0.050	
H <sub>E</sub>	5.80	6.20	0.228	0.244
L	1.05		0.041	
L <sub>p</sub>	0.40	1.00	0.016	0.039
Q	0.60	0.70	0.024	0.028
v	0.25		0.01	
w	0.25		0.01	
y	0.10		0.004	
Z	0.30	0.70	0.012	0.028
θ	0°	8°	0°	8°

NOTES:

1. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
2. MAXIMUM MOLD PROTRUSION FOR D IS 0.15mm.
3. MAXIMUM MOLD PROTRUSION FOR E IS 0.25mm.

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**PACKAGE DIAGRAM  
TSSOP 8**



- NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
  2. MAXIMUM MOLD PROTRUSION FOR D IS 0.15mm.
  3. MAXIMUM MOLD PROTRUSION FOR E IS 0.25mm.

DIM	MILLIMETERS	
	MIN	MAX
A		1.10
A <sub>1</sub>	0.05	0.15
A <sub>2</sub>	0.80	0.95
A <sub>3</sub>	0.25	
b <sub>p</sub>	0.25	0.45
c	0.15	0.28
D	2.90	3.10
E	2.90	3.10
e	0.65	
H <sub>E</sub>	4.70	5.10
L	0.94	
L <sub>p</sub>	0.40	0.70
v	0.10	
w	0.10	
y	0.10	
Z	0.35	0.70
θ	0°	6°

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