ARIZONA MICROTEK, INC.

AZ10EP16VS
AZ100EP16VS

ECL/PECL Differential Receiver with Variable Output Swing

FEATURES

- Silicon-Germanium for High Speed Operation
- 150ps Typical Propagation Delay
- AZ100EP16VS Functionally Equivalent to ON Semiconductor MC100EP16VS at 3.3V
- Available in a 3x3mm MLP Package

PACKAGE AVAILABILITY

PACKAGE	PART NO.	MARKING
MLP 8	AZ10EP16VSL	AZM16E
MLP 8 T&R	AZ10EP16VSLR1	AZM16E
MLP 8 T&R	AZ10EP16VSLR2	AZM16E
MLP 8	AZ100EP16VSL	AZM16F
MLP 8 T&R	AZ100EP16VSLR1	AZM16F
MLP 8 T&R	AZ100EP16VSLR2	AZM16F
SOIC 8	AZ10EP16VSD	AZM10EP16VS
SOIC 8 T&R	AZ10EP16VSDR1	AZM10EP16VS
SOIC 8 T&R	AZ10EP16VSDR2	AZM10EP16VS
SOIC 8	AZ100EP16VSD	AZM100EP16VS
SOIC 8 T&R	AZ100EP16VSDR1	AZM100EP16VS
SOIC 8 T&R	AZ100EP16VSDR2	AZM100EP16VS
TSSOP 8	AZ10EP16VST	AZTP16VS
TSSOP 8 T&R	AZ10EP16VSTR1	AZTP16VS
TSSOP 8 T&R	AZ10EP16VSTR2	AZTP16VS
TSSOP 8	AZ100EP16VST	AZHP16VS
TSSOP 8 T&R	AZ100EP16VSTR1	AZHP16VS
TSSOP 8 T&R	AZ100EP16VSTR2	AZHP16VS

DESCRIPTION

The AZ10/100EP16VS is a Silicon–Germanium (SiGe) differential receiver with variable output swing. The EP16VS has functionality and output transition times similar to the EP16, with an input that controls the amplitude of the Q/$\overline{Q}$ outputs.

The operational range of the EP16VS control input, V_{CTRL}, is from V_{REF} (full swing) to V_{CC} (min. swing). Maximum swing is achieved by leaving the V_{CTRL} pin open or tied to V_{EE}. Simple control of the output swing can be obtained by a variable resistor between the V_{REF} and V_{CC} pins, with the wiper driving V_{CTRL}. Typical application circuits and results are described in this Data Sheet.

The EP16VS provides a V_{REF} output for a DC bias for AC coupling to the device. The V_{REF} pin should be used only as a bias for the EP16VS as its current sink/source capability is limited. Whenever used, the V_{REF} pin should be bypassed to ground via a 0.01µF capacitor.

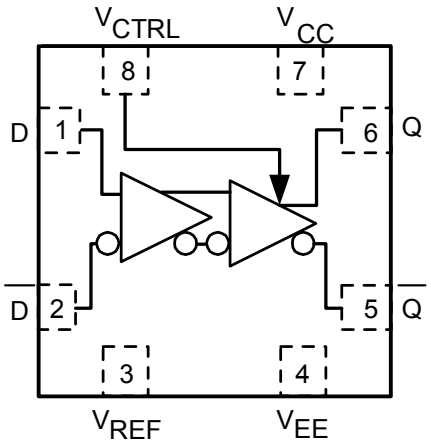
Under open input conditions for D/$\overline{D}$, the Q/$\overline{Q}$ outputs are not guaranteed.

NOTE: Specifications in ECL/PECL tables are valid when thermal equilibrium is established.

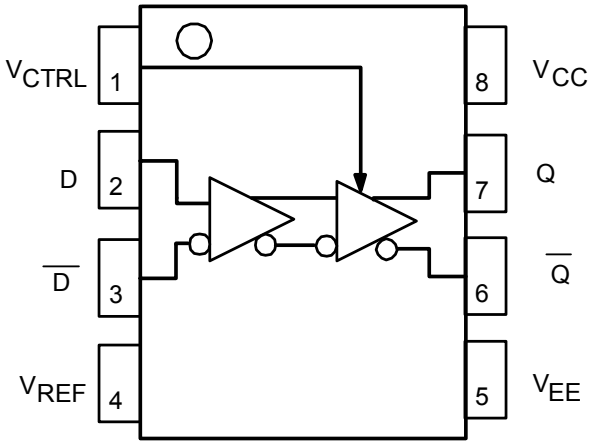
PIN DESCRIPTION

PIN	FUNCTION
D, $\overline{D}$	Data Inputs
V_{CTRL}	Output Swing Control
Q, $\overline{Q}$	Data Outputs
V_{REF}	Reference Voltage Output
V_{CC}	Positive Supply
V_{EE}	Negative Supply

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



MLP 8 (TOP VIEW)



8 SOIC & 8 TSSOP

Absolute Maximum Ratings are those values beyond which device life may be impaired.

Symbol	Characteristic	Rating	Unit
V_{CC}	PECL Power Supply (V_{EE} = 0V)	0 to +4.5	Vdc
V_I	PECL Input Voltage (V_{EE} = 0V)	0 to +4.5	Vdc
V_{EE}	ECL Power Supply (V_{CC} = 0V)	-4.5 to 0	Vdc
V_I	ECL Input Voltage (V_{CC} = 0V)	-4.5 to 0	Vdc
I_{OUT}	Output Current --- Continuous --- Surge	50 100	mA
T_A	Operating Temperature Range	-40 to +85	°C
T_{STG}	Storage Temperature Range	-65 to +150	°C

10K ECL DC Characteristics (V_{EE} = -3.0V to -3.6V, V_{CC} = GND)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage[1]	-1085		-835				-1020	-895	-770	-960		-710	mV
V_{OL}	Output LOW Voltage[1] $V_{CTRL} = V_{REF}$	-2115		-1865				-2050	-1925	-1800	-1990		-1740	mV
V_{OL}	Output LOW Voltage[1] $V_{CTRL} = V_{CC}$	-1330		-1080				-1265	-1140	-1015	-1205		-915	mV
V_{REF}	Reference Voltage	-1700	-1600	-1500	-1670	-1570	-1470	-1650	-1550	-1450	-1600	-1500	-1400	mV
I_{IH}	Input HIGH Current D,$\overline{D}$ V_{CTRL}			80 400			80 400			80 400			80 400	µA
I_{IL}	Input LOW Current	0.5			0.5			0.5			0.5			µA
I_{EE}	Power Supply Current	21	27	36	22	28	37	22	29	38	24	30	40	mA

1. Each output is terminated through a 50Ω resistor to V_{CC} – 2V.

10K LVPECL DC Characteristics (V_{EE} = GND, V_{CC} = +3.3V)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage[1,2]	2215		2465				2280	2405	2530	2340		2590	mV
V_{OL}	Output LOW Voltage[2] $V_{CTRL} = V_{REF}$	1185		1435				1250	1375	1500	1310		1560	mV
V_{OL}	Output LOW Voltage[2] $V_{CTRL} = V_{CC}$	1970		2220				2035	2160	2285	2095		2385	mV
V_{REF}	Reference Voltage	1600	1700	1800	1630	1730	1830	1650	1750	1850	1700	1800	1900	mV
I_{IH}	Input HIGH Current D,$\overline{D}$ V_{CTRL}			80 400			80 400			80 400			80 400	µA
I_{IL}	Input LOW Current	0.5			0.5			0.5			0.5			µA
I_{EE}	Power Supply Current	21	27	36	22	28	37	22	29	38	24	30	40	mA

1. For supply voltages other that 3.3V, use the ECL table values and ADD supply voltage value.
2. Each output is terminated through a 50Ω resistor to V_{CC} – 2V.

100K ECL DC Characteristics (V_{EE} = -3.0V to -3.6V, V_{CC} = GND)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage[1]	-1095		-890	-1035		-890	-1035	-965	-890	-1035		-890	mV
V_{OL}	Output LOW Voltage[1] $V_{CTRL} = V_{REF}$	-1925		-1835	-1965		-1775	-1965	-1870	-1775	-1965		-1775	mV
V_{OL}	Output LOW Voltage[1] $V_{CTRL} = V_{CC}$	-1180		-1045	-1160		-970	-1160	-1065	-970	-1160		-970	mV
V_{REF}	Reference Voltage	-1650		-1450	-1650		-1450	-1650	-1550	-1450	-1650		-1450	mV
I_{IH}	Input HIGH Current D,$\overline{D}$ V_{CTRL}			80 400			80 400			80 400			80 400	µA
I_{IL}	Input LOW Current	0.5			0.5			0.5			0.5			µA
I_{EE}	Power Supply Current	20	26	35	21	27	36	22	28	38	25	31	41	mA

1. Each output is terminated through a 50Ω resistor to V_{CC} – 2V.

100K LVPECL DC Characteristics (V_{EE} = GND, V_{CC} = +3.3V)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage[1,2]	3905		4110	3965		4110	3965	4035	4110	3965		4110	mV
V_{OL}	Output LOW Voltage[2] $V_{CTRL} = V_{REF}$	3075		3165	3035		3225	3035	3130	3225	3035		3225	mV
V_{OL}	Output LOW Voltage[2] $V_{CTRL} = V_{CC}$	3820		3955	3840		4030	3840	3935	4030	3840		4030	mV
V_{REF}	Reference Voltage	1650		1850	1650		1850	1650	1750	1850	1650		1850	mV
I_{IH}	Input HIGH Current D,$\overline{D}$ V_{CTRL}			80 400			80 400			80 400			80 400	µA
I_{IL}	Input LOW Current	0.5			0.5			0.5			0.5			µA
I_{EE}	Power Supply Current	20	26	35	21	27	36	22	28	38	25	31	41	mA

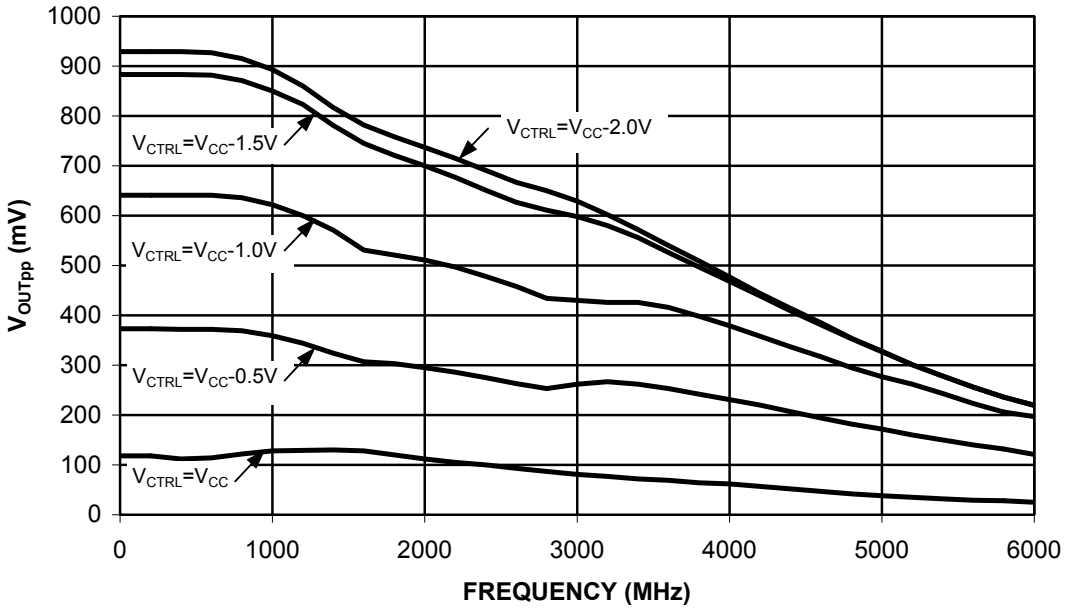
1. For supply voltages other that 3.3V, use the ECL table values and ADD supply voltage value.
2. Each output is terminated through a 50Ω resistor to V_{CC} – 2V.

AC Characteristics (V_{EE} = -3.0 to -3.6V, V_{CC} = GND, V_{CTRL}=V_{REF} or V_{EE} = GND, V_{CC} = +3.0V to 3.6V, V_{CTRL} = V_{REF})

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Toggle Frequency[5]		>4			>4			>4			>4		GHz
t_{PLH} / t_{PHL}	Input to Output (Diff) Delay (SE)	100	150 155	240	100	150 155	240	100	150 155	240	120	170 175	280	ps
t_{SKEW}	Duty Cycle Skew[1] (Diff)		4	20		4	15		4	15		4	15	ps
V_{pp}	Minimum Input Swing[2]	150			150			150			150			mV
V_{CMR}	Common Mode Range[3]	V_{EE} + 2.0		V_{CC}	V_{EE} + 2.0		V_{CC}	V_{EE} + 2.0		V_{CC}	V_{EE} + 2.0		V_{CC}	V
A_v	Small Signal Gain[4]								28					dB
t_r / t_f	Output Rise/Fall Times Q (20% - 80%)		120	70		120	180		120	180		120	200	ps

1. Duty cycle skew is the difference between a t_{PLH} and t_{PHL} propagation delay through a device.
2. V_{PP} is the minimum peak-to-peak differential input swing for which AC parameters are guaranteed.
3. The V_{CMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}(min) and 1V.
4. Differential input, differential output. 240Ω to V_{EE} on Q/$\overline{Q}$ outputs and V_{CTRL} = Open Circuit.
5. See graph below.

Large Signal Performance*



*Measured using a 750mV differential input source at 50% duty cycle.

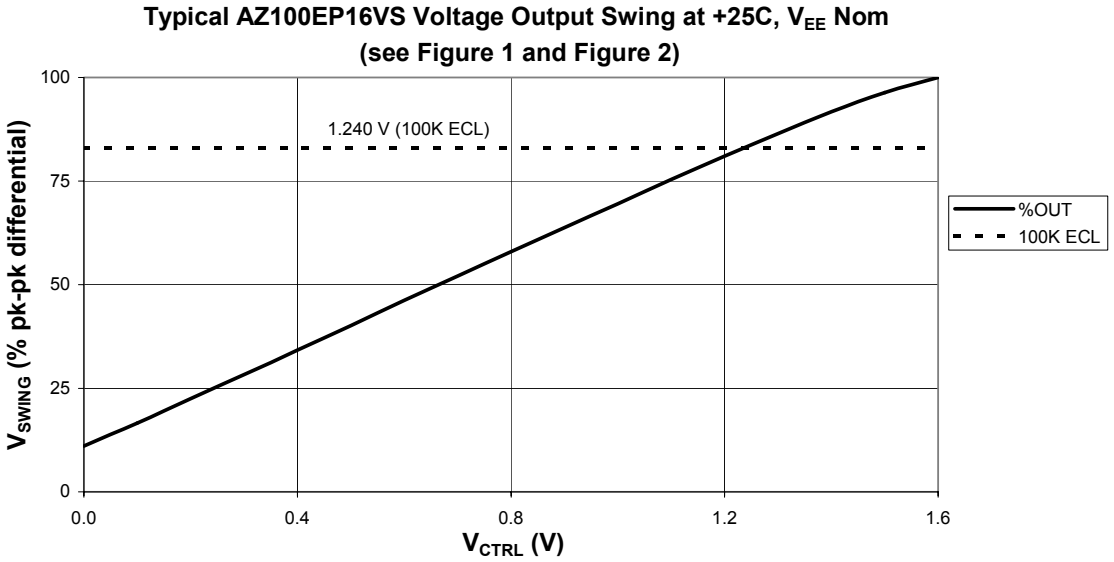


Figure 1: Voltage Source Implementation

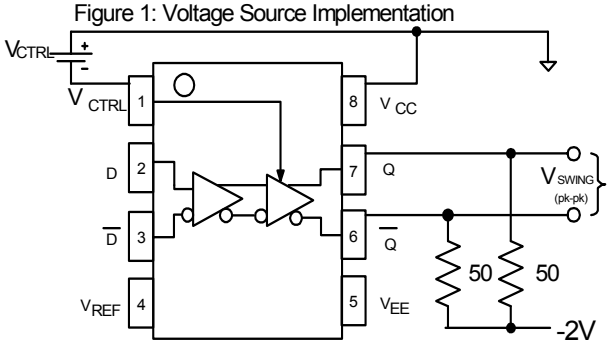
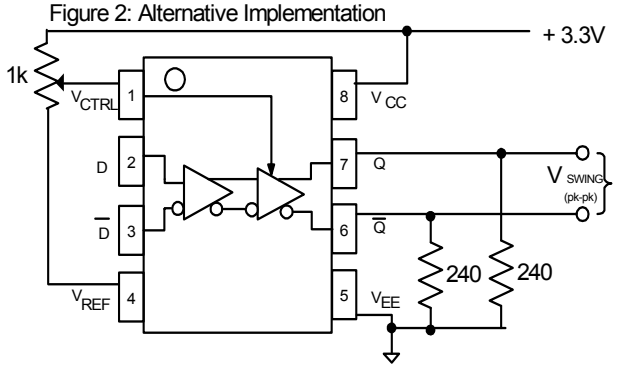
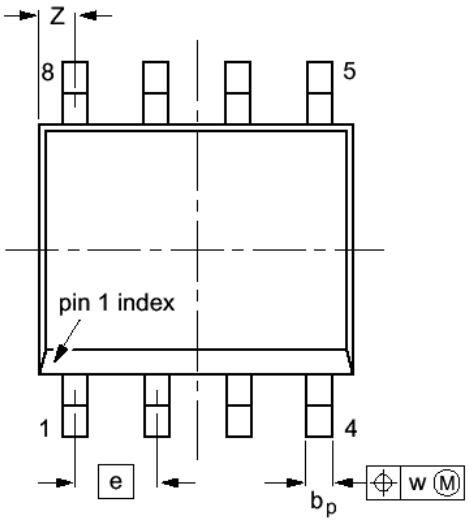
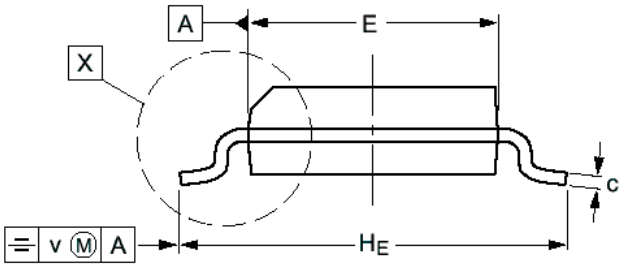


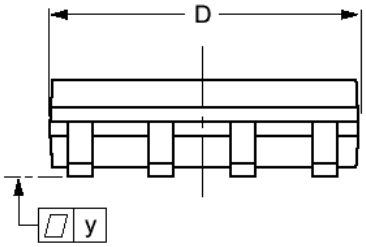
Figure 2: Alternative Implementation

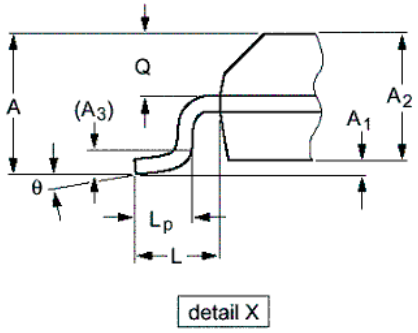


PACKAGE DIAGRAM
SOIC 8







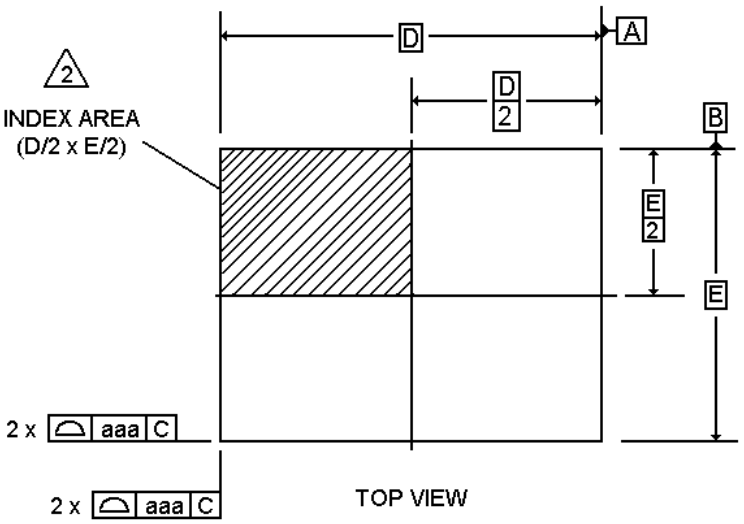


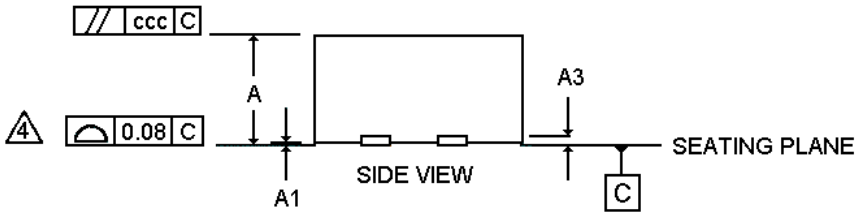
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A		1.75		0.069
A_1	0.10	0.25	0.004	0.010
A_2	1.25	1.45	0.049	0.057
A_3	0.25		0.01	
b_p	0.36	0.49	0.014	0.019
c	0.19	0.25	0.0075	0.0100
D	4.8	5.0	0.19	0.20
E	3.8	4.0	0.15	0.16
e	1.27		0.050	
H_E	5.80	6.20	0.228	0.244
L	1.05		0.041	
L_p	0.40	1.00	0.016	0.039
Q	0.60	0.70	0.024	0.028
v	0.25		0.01	
w	0.25		0.01	
y	0.10		0.004	
Z	0.30	0.70	0.012	0.028
θ	0^O	8^O	0^O	8^O

NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
2. MAXIMUM MOLD PROTRUSION FOR D IS 0.15mm.
3. MAXIMUM MOLD PROTRUSION FOR E IS 0.25mm.

AZ10EP16VS
AZ100EP16VS

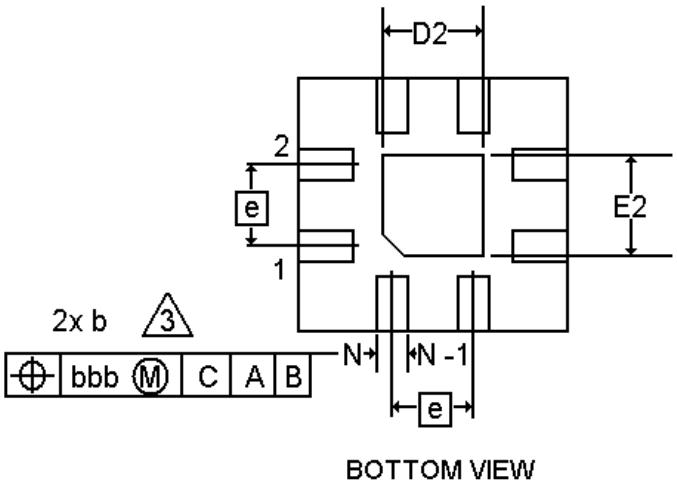
PACKAGE DIAGRAM
MLP 8



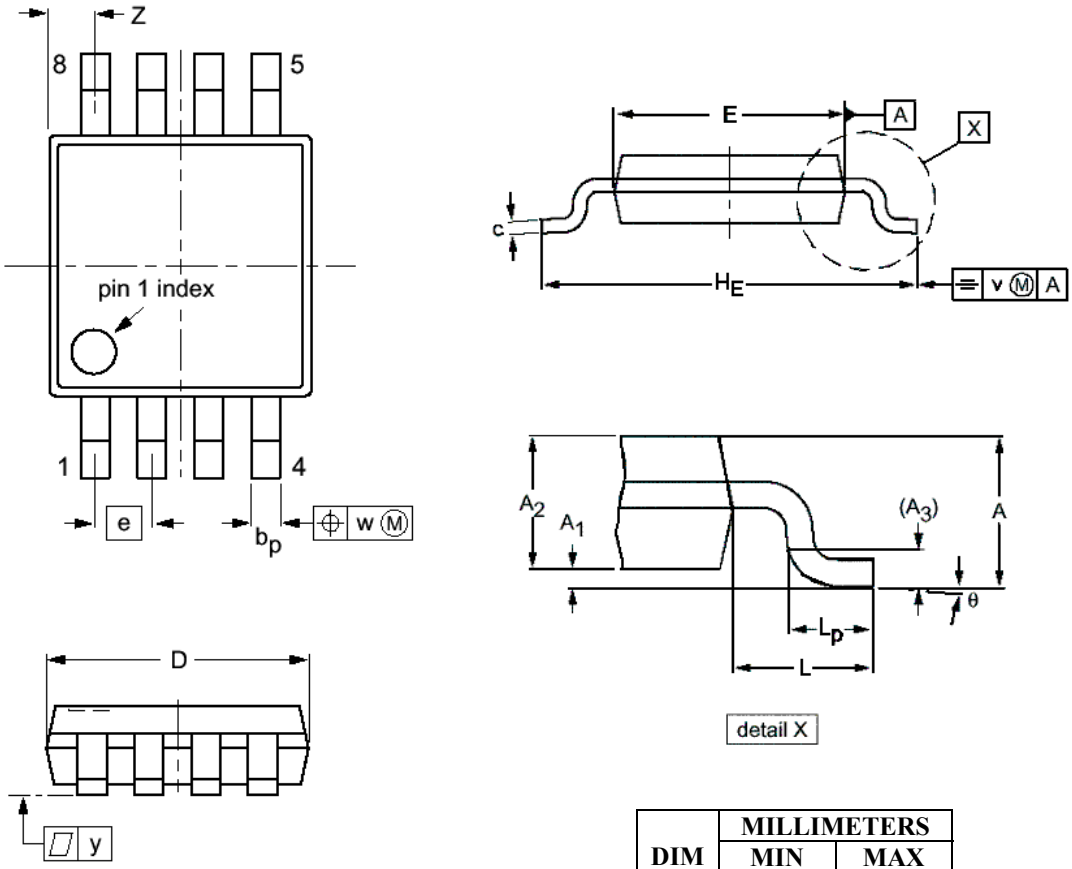


NOTES
1. DIMENSIONING AND TOLERANCING CONFORM TO ASME T14-1994.
2. THE TERMINAL #1 AND PAD NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012.
3. DIMENSION b APPLIES TO METALLIZED PAD AND IS MEASURED BETWEEN 0.25 AND 0.30mm FROM PAD TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS	
	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.25 REF	
b	0.30	0.35
D	2.90	3.10
D2	1.65	1.95
E	2.90	3.10
E2	1.65	1.95
e	0.65 BSC	
L	0.35	0.45
aaa	0.25	
bbb	0.10	
ccc	0.10	



PACKAGE DIAGRAM
TSSOP 8



DIM	MILLIMETERS	
	MIN	MAX
A		1.10
A_1	0.05	0.15
A_2	0.80	0.95
A_3	0.25	
b_p	0.25	0.45
c	0.15	0.28
D	2.90	3.10
E	2.90	3.10
e	0.65	
H_E	4.70	5.10
L	0.94	
L_p	0.40	0.70
v	0.10	
w	0.10	
y	0.10	
Z	0.35	0.70
θ	0^O	6^O

NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
2. MAXIMUM MOLD PROTRUSION FOR D IS 0.15mm.
3. MAXIMUM MOLD PROTRUSION FOR E IS 0.25mm.