Bay Linear

Inspire the Linear Power

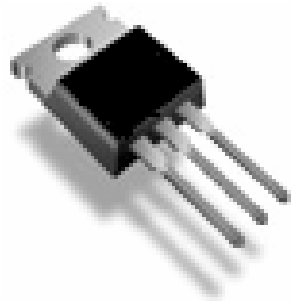
N-Channel Field Effect Transistor

4N600(3600)

Description

The Bay Linear n-channel power field effect transistors are produced using high cell density DMOS technology , These devices are particularly suited for high voltage applications such as automotive and other battery powered circuits where fast switching, low in-line power loss and resistance to transistors are needed.

The TO-220 is offered in a 3-pin is universally preferred for all commercial-industrial applications at power dissipation level to approximately to 50 watts. Also, available in a D^2 surface mount power package with a power dissipation up to 2 Watts



Features

- **Critical DC Electrical parameters specified at elevated Temp.**
- **Rugged internal source-drain diode can eliminate the need for external Zener diode transient suppresser**
- **Super high density cell design for extremely low $R_{DS(ON)}$**

V_{DSS} = 600V
$R_{DS\ (ON)}$ = 1.9 Ω
I_D = 4.0A

Ordering Information

Device	Package	Temp.
4N600T	TO-220	0 to 150°C
4N600S	TO-263 (D^2)	0 to 150°C

Absolute Maximum Rating

Symbol	Parameter	Max	Unit
I_D (T_C=25°C)	Drain Current	4.0	A
I_D (T_C=100°C)	-Continues	2.5	
	-Pulsed	16	
V_{GSV}	Gate Source Voltage	±20	V
P_D	Total Power Dissipation @ T_C =25°C	75	W
	Derate above 25°C	0.59	W/°C
T_J	Operating and Storage	-55 to 150	°C
T_{STG}	Temperature Range		

Electrical Characteristics (T_C = 25°C unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=600V V_{GS}=0V			100	μA
V	Drain-to-Source Breakdown	I_D=100μA, V_{GS}=0	600	-	-	V
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=250μA	2		4	V
$R_{DS(ON)}$	Static Drain Voltage	V_{GS}=10V, I_D=2.4A	-	-	1.9	Ω
I_{GSS}	Gate-to-Source Forward Leakage Gate-to-Source Reverse Leakage	V_{GS}=20V V_{GS}=-20V			100 -100	NA
g_{fs}	Forward Tranconductance	V_{DS}=100V, I_D =2.4A	2.9			S
C_{ISS}	Input Capacitance	V_{DS}= 25V, V_{GS}=0V F=1.0 MHZ		800		pF
C_{OSS}	Output Capacitance			110		pF
C_{RSS}	Reverse Tras. Capacitance			20		pF
$t_{D(ON)}$	Turn-ON Delay Time	V_{DD}=300V I_D=2.4A, R_{GEN}=12Ω R_D=74Ω		12		NS
t_r	Turn-ON Rise Time			18		
$t_{d(off)}$	Turn-OFF Delay Time			53		
t_F	Turn-OFF Fall Time			19		
I_S	Maxim Continuous Drain source Diode Forward Current				4.0	A
V_{DS} (note)	Drain Source Diode Forward Voltage	V_{GS}=0V I_S=4A			1.50	V
THERMAI CHRACTERISTICS						
R_{JC}	Thermal Resistance, Junction to Case				5	°C/W
R_{JC}	Thermal Resistance, Junction to Ambient				100	°C/W

Note: Pulse Test: Pulse With≤ 300 μS, Duty Cycle ≤ 2.0%

Advance Information- These data sheets contain descriptions of products that are in development. The specifications are based on the engineering calculations, computer simulations and/ or initial prototype evaluation.

Preliminary Information- These data sheets contain minimum and maximum specifications that are based on the initial device characterizations. These limits are subject to change upon the completion of the full characterization over the specified temperature and supply voltage ranges.

The application circuit examples are only to explain the representative applications of the devices and are not intended to guarantee any circuit design or permit any industrial property right to other rights to execute. Bay Linear takes no responsibility for any problems related to any industrial property right resulting from the use of the contents shown in the data book. Typical parameters can and do vary in different applications. Customer's technical experts must validate all operating parameters including " Typical" for each customer application.

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