BURR - BROWN®

ADS1250

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Resolution PLUS™ 20-Bit Data Acquisition System
ANALOG-TO-DIGITAL CONVERTER

FEATURES

- 20 BITS NO MISSING CODES
- 18 BITS EFFECTIVE RESOLUTION UP TO 25kHz DATA RATE
- LOW NOISE: 2.8ppm at PGA = 1
- DIFFERENTIAL INPUTS
- INL: 0.002% (MAX)
- PROGRAMMABLE FULL SCALE
- I/O CONTROLLED PGA: 1, 2, 4, 8
- EXTERNAL REFERENCE

APPLICATIONS

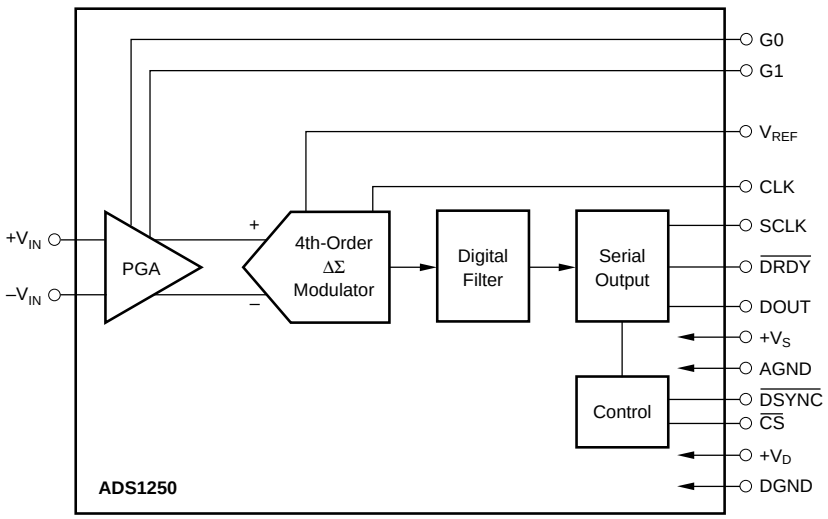
- CARDIAC DIAGNOSTICS
- DIRECT THERMOCOUPLE INTERFACE
- BLOOD ANALYSIS
- INFRARED PYROMETER
- LIQUID/GAS CHROMATOGRAPHY
- PRECISION PROCESS CONTROL

DESCRIPTION

The ADS1250 is a precision, wide dynamic range, delta-sigma, analog-to-digital converter with 20-bit resolution operating from a single +5V supply. The delta-sigma architecture is used for wide dynamic range and to guarantee 20 bits of no missing code performance. An effective resolution of 18 bits (2.8ppm of rms noise) is achieved for conversion rates up to 25kHz. The dynamic range of the converter is further increased by providing a low-noise Programmable Gain Amplifier (PGA) with gain stages of 1, 2, 4, or 8 for low level input signals.

The ADS1250 is designed for high-resolution measurement applications in cardiac diagnostics, smart transmitters, industrial process control, weigh scales, chromatography and portable instrumentation. The converter includes a flexible synchronous serial interface and offers a three-wire control mode for low-cost isolation.

The ADS1250 is a single-channel converter and is offered in an SOL-16 package.



International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111
Twx: 910-952-1111 • Internet: http://www.burr-brown.com/ • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

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SPECIFICATIONS

All specifications at T_{MIN} to T_{MAX}, V_D = V_S = +5V, CLK = 9.6MHz, PGA = 1, and V_{REF} = 4.096, unless otherwise specified.

PARAMETER	CONDITIONS	ADS1250U MIN	ADS1250U TYP	ADS1250U MAX	UNITS
ANALOG INPUT					
Input Voltage Range[1]	G = Gain	AGND		$\pm V_{REF}/G$	V
Programmable Gain Amplifier		1		8	
Input Impedance (differential)	G = Gain		104/G		kΩ
Input Capacitance	G = Gain		6 • G		pF
Input Leakage	At +25°C		5	50	pA
	At T_{MIN} to T_{MAX}			1	nA
DYNAMIC CHARACTERISTICS					
Data Rate				25	kHz
Bandwidth	3dB	5.4			kHz
Serial Clock (SCLK)				9.6	MHz
System Clock Input (CLK)				9.6	MHz
ACCURACY					
Integral Linearity Error[2]			±0.0012	±0.0020	% of FSR
THD	1kHz Input; 0.1dB below FS		97		dB
Noise			2.8	3.8	ppm of FSR, rms
Resolution			20		Bits
No Missing Codes			20		Bits
Common-Mode Rejection[3]	at DC	90	105		dB
Gain Error				1	% of FSR
Offset Error			±100	±200	ppm of FSR
Gain Sensitivity to V_{REF}	V_{REF} = 4.096V ±0.1V		1:1		
Power Supply Rejection Ratio		60	78		dB
PERFORMANCE OVER TEMPERATURE					
Offset Drift			0.25		ppm/°C
Gain Drift			5.0		ppm/°C
VOLTAGE REFERENCE					
V_{REF}		3.996V	4.096	4.196	V
Load Current			125		µA
DIGITAL INPUT/OUTPUT					
Logic Family			CMOS		
Logic Level: V_{IH}		+4.0		$+V_D$ + 0.3	V
V_{IL}		–0.3		+0.8	V
V_{OH}	I_{OH} = –500µA	+4.5			V
V_{OL}	I_{OL} = 500µA			0.4	V
Data Format		Binary Two's Complement			
POWER SUPPLY REQUIREMENTS					
Operation		+4.75	+5	+5.25	VDC
Quiescent Current, Analog	V = +5VDC		14		mA
Quiescent Current, Digital	V = +5VDC		1		mA
Operating Power			75	100	mW
TEMPERATURE RANGE					
Operating		–40		+85	°C
Storage		–60		+100	°C

NOTES: (1) In order to achieve the converter's full-scale range, the input must be fully differential. If the input is single-ended ($+V_{IN}$ or $-V_{IN}$ is fixed), then the full-scale range is one-half that of the differential range. (2) Applies to full-differential signals. (3) The common-mode rejection test is performed with a 100mV differential input.

ABSOLUTE MAXIMUM RATINGS

Analog Input: Current	±100mA, Momentary
	±10mA, Continuous
Voltage	AGND –0.3V to V_S + 0.3V
V_S to V_D	–0.3V to 6V
V_S to AGND	–0.3V to 6V
V_D to DGND	–0.3V to 6V
AGND to DGND	±0.3V
V_{REF} Voltage to AGND	–0.3V to V_S + 0.3V
Digital Input Voltage to DGND	–0.3V to V_D + 0.3V
Digital Output Voltage to DGND	–0.3V to V_D + 0.3V
Lead Temperature (soldering, 10s)	+300°C
Power Dissipation (any package)	500mW

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

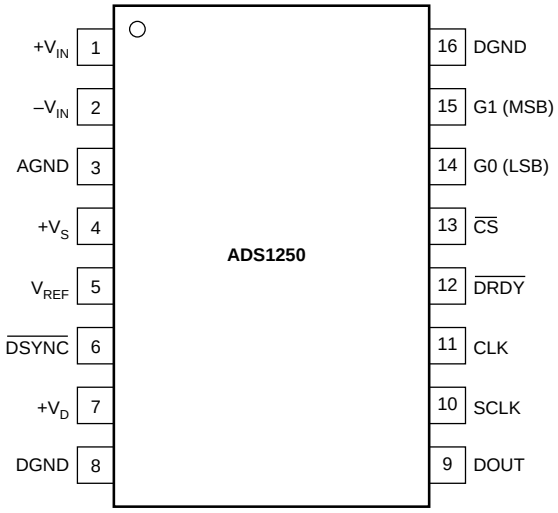
PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER(1)	TRANSPORT MEDIA
ADS1250U	SOL-16	211	–40°C to +85°C	ADS1250U	ADS1250U	Rails
"	"	"	"	"	ADS1250U/1K	Tape and Reel

NOTE: (1) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /1K indicates 1000 devices per reel). Ordering 1000 pieces of “ADS1250U/1K” will get a single 1000-piece Tape and Reel.

PIN CONFIGURATION

Top View **SOL-16**



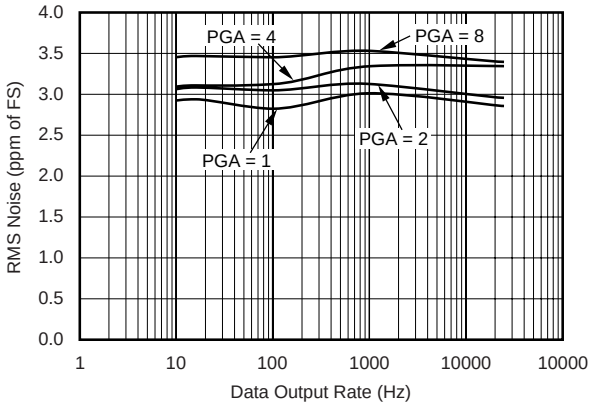
PIN DESCRIPTIONS

PIN	NAME	PIN DESCRIPTION
1	$+V_{IN}$	Analog Input: Positive Input of the Differential Analog Input.
2	$-V_{IN}$	Analog Input: Negative Input of the Differential Analog Input.
3	AGND	Analog Input: Analog Ground.
4	$+V_S$	Analog Input: Analog Power Supply Voltage, +5V.
5	V_{REF}	Analog Input: Reference Voltage Input.
6	$\overline{DSYNC}$	Digital Input: Data Synchronization. A falling edge on this input will reset the modulator count and place the modulator in a hold state. The modulator is released from the hold state on the rising edge of $\overline{DSYNC}$. This can be used to synchronize multiple ADS1250s.
7	$+V_D$	Digital Input: Digital Power Supply Voltage, +5V.
8	DGND	Digital Input: Digital Ground.
9	DOUT	Digital Output: Serial Data Output. The serial data is clocked out of the serial data output shift register through this pin. The pin is driven when $\overline{CS}$ is LOW, and high impedance when $\overline{CS}$ is HIGH.
10	SCLK	Digital Input: Serial Clock. The serial clock is in the form of a CMOS-compatible clock. The serial clock can operate up to the device's system clock frequency. The serial clock can be either a free-running clock or noncontinuous clock, with either type of clock; the serial data output is gated by $\overline{CS}$.
11	CLK	Digital Input: Device System Clock. The system clock is in the form of a CMOS-compatible clock.
12	$\overline{DRDY}$	Digital Output: Data Ready. A falling edge on this output indicates that a new output word is available from the ADS1250 data output register.
13	$\overline{CS}$	Digital Input: Chip Select. Active LOW logic input used to enable serial data output from the ADS1250. $\overline{CS}$ controls the state of the DOUT pin. If $\overline{CS}$ is HIGH, DOUT is high impedance; if $\overline{CS}$ is LOW, DOUT drives the bus. $\overline{CS}$ can be used in three ways: (1) If the ADS1250 shares the bus with other devices, $\overline{CS}$ is used as serial data output enable for communications. (2) If the ADS1250 shares the bus with other devices and SCLK is a free-running clock, $\overline{CS}$ is used to gate serial data out of the device. (3) If the ADS1250 is the only device on the bus, $\overline{CS}$ can be tied LOW to always enable serial data output for a two-wire interface. Refer to the Serial Communications section of this data sheet for more detail.
14	G0	Digital Input: Gain Selection Control (LSB).
15	G1	Digital Input: Gain Selection Control (MSB).
16	DGND	Digital Input: Digital Ground.

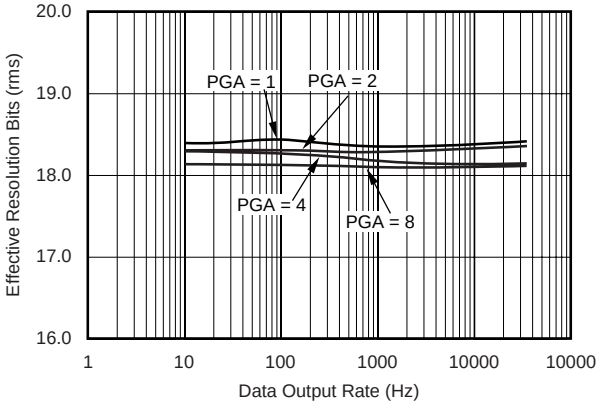
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, V_D = V_S = +5V, CLK = 9.6MHz, PGA = 1, and V_{REF} = 4.096, unless otherwise specified.

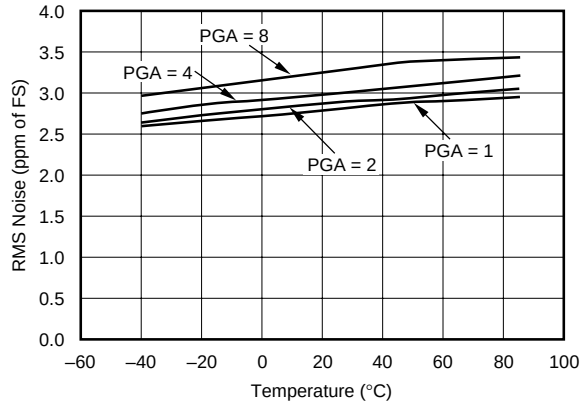
RMS NOISE vs DATA OUTPUT RATE



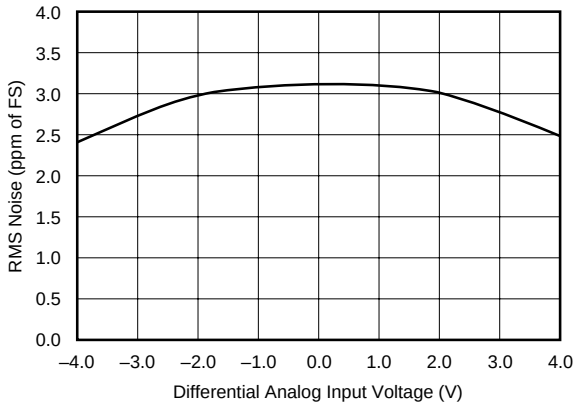
EFFECTIVE RESOLUTION vs DATA OUTPUT RATE



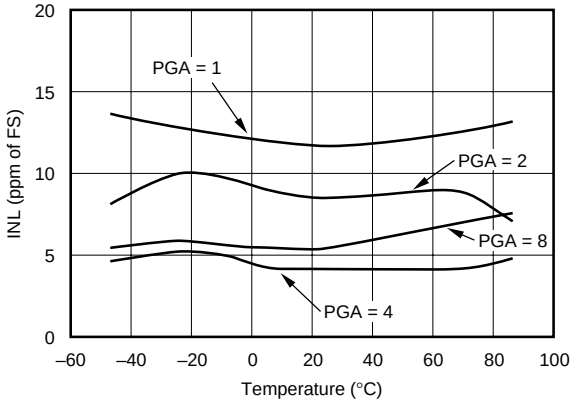
RMS NOISE vs TEMPERATURE



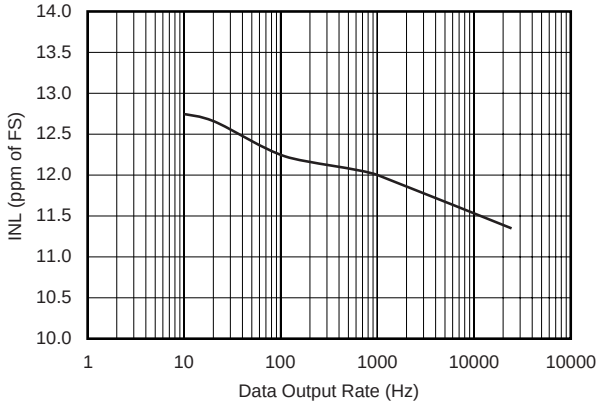
RMS NOISE vs INPUT VOLTAGE (PGA = 1)



INTEGRAL NON-LINEARITY vs TEMPERATURE



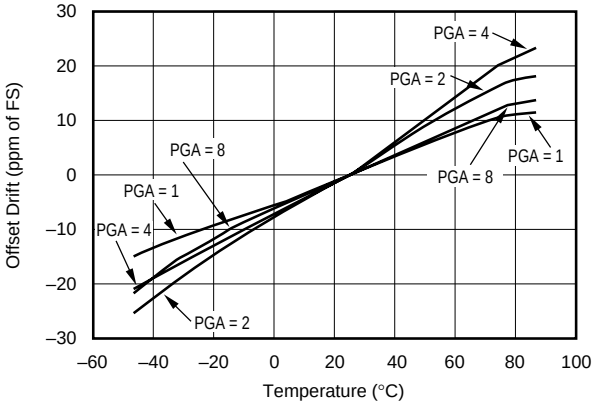
INTEGRAL NON-LINEARITY vs DATA OUTPUT RATE (PGA = 1)



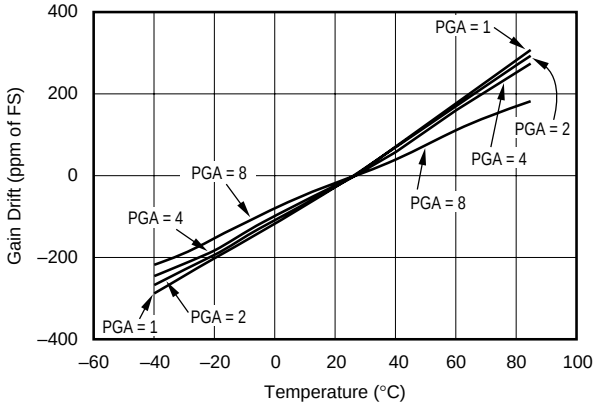
TYPICAL PERFORMANCE CURVES (Cont.)

At T_A = +25°C, V_D = V_S = +5V, CLK = 9.6MHz, PGA = 1, and V_{REF} = 4.096, unless otherwise specified.

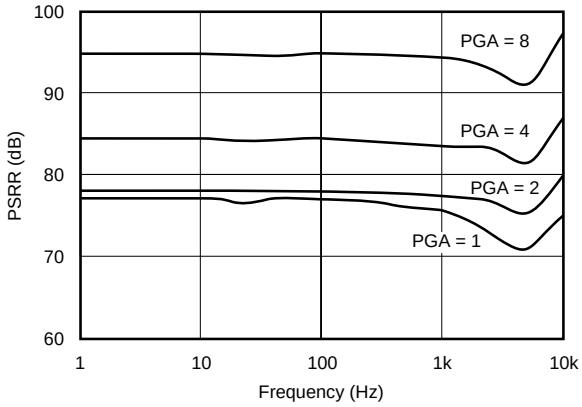
OFFSET DRIFT vs TEMPERATURE



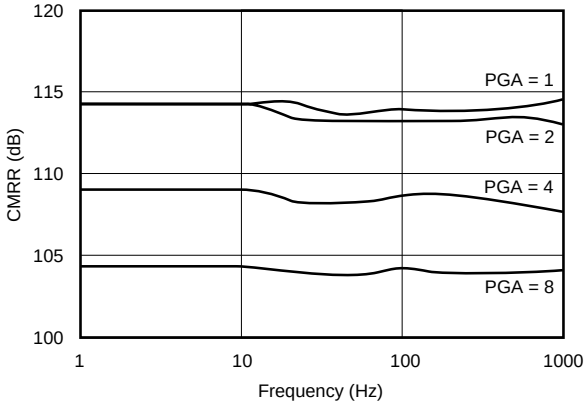
GAIN DRIFT vs TEMPERATURE



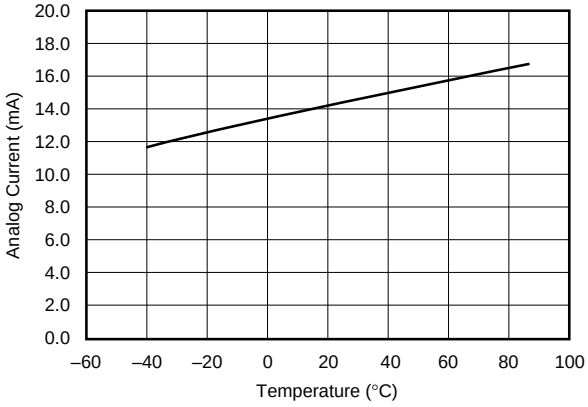
POWER SUPPLY REJECTION RATIO
vs FREQUENCY



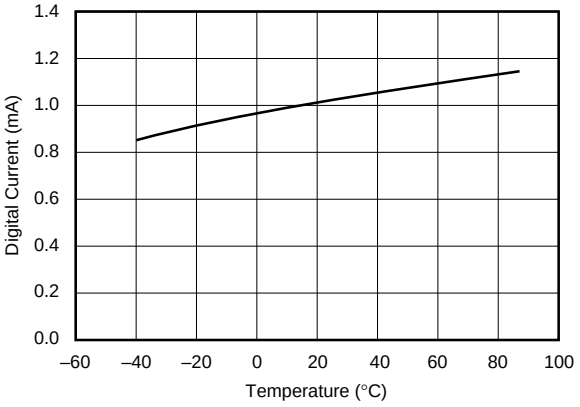
COMMON-MODE REJECTION RATIO
vs FREQUENCY



ANALOG CURRENT vs TEMPERATURE
(PGA = 1)



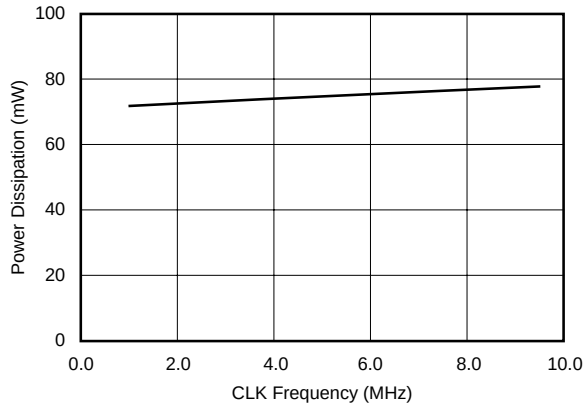
DIGITAL CURRENT vs TEMPERATURE
(PGA = 1)



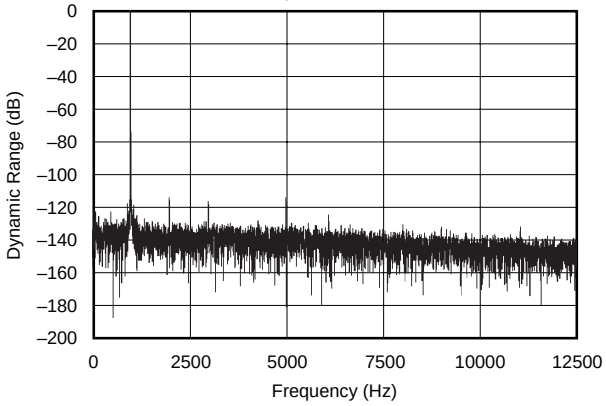
TYPICAL PERFORMANCE CURVES (Cont.)

At T_A = +25°C, V_D = V_S = +5V, CLK = 9.6MHz, PGA = 1, and V_{REF} = 4.096, unless otherwise specified.

POWER DISSIPATION vs CLK FREQUENCY
(PGA = 1)



TYPICAL FFT ANALYSIS
OF THE 1kHz f_S INPUT SIGNAL (PGA = 4)



THEORY OF OPERATION

The ADS1250 is a precision, high dynamic range, 20-bit, delta-sigma, A/D converter capable of achieving very high-resolution digital results at high data rates. The analog input signal is continuously sampled at a rate determined by the frequency of the system clock (CLK). The sampled analog input is modulated by the delta-sigma A/D modulator, followed by a digital filter value. A programmable gain function is also incorporated in the delta-sigma modulator with larger input sampling capacitors for higher gains. A $sinc^5$ digital low-pass filter processes the output of the delta-sigma modulator and writes the result into the data output register. The $\overline{DRDY}$ pin is pulled LOW indicating that new data is available to be read by the external microcontroller/microprocessor. As shown in the block diagram, the main functional blocks of the ADS1250 are the programmable gain amplifier, a fourth-order delta-sigma modulator, a digital filter, control logic, and a serial interface. Each of these functional blocks is described below.

ANALOG INPUT

The ADS1250 contains a fully differential analog input with programmable gain. The fully differential switched capacitor architecture provides low system noise, common-mode rejection of 105dB, and excellent power supply rejection. The selectable gains on the input are 1, 2, 4, or 8, which gives a bipolar input voltage range from –4.096 to +4.096V, to –512mV to +512mV, when the reference input voltage equals +4.096V. The bipolar ranges are with respect to $-V_{IN}$ and not with respect to GND.

Figure 1 shows the basic input structure of the ADS1250. The analog input impedance is directly related to the sampling frequency of the input capacitor (f_{MOD}), and the gain setting (G) of the device. The sampling frequency of the input capacitor is derived from the system clock (CLK). Therefore, a lower CLK rate decreases the sampling frequency, which results in a higher analog input impedance.

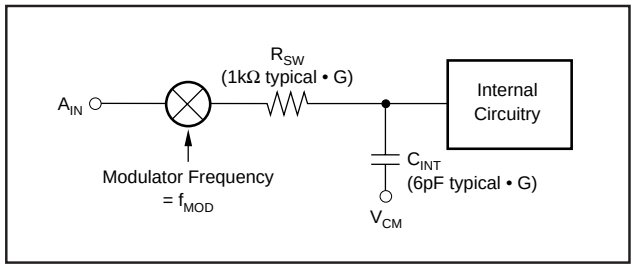


FIGURE 1. Analog Input Structure.

Additionally, a lower gain setting (G) decreases the sampling capacitor size, which results in a higher analog input impedance. This can be seen in the following equation:

$$A_{IN}\ \text{Impedance}\ (\Omega) = \frac{9.6\ \text{MHz} \bullet 104\text{E}3}{\text{CLK} \bullet \text{G}}$$

With regard to the analog input signal, the overall analog performance of the device is affected by three items. First, the input impedance can affect accuracy. If the source impedance of the input signal is significant, or if there is passive filtering prior to the ADS1250, a significant portion of the signal can be lost across this external impedance. The magnitude of the effect is dependent on the desired system performance.

Second, the current into or out of the analog inputs must be limited. Under no conditions should the current into or out of the analog inputs exceed 10mA.

Third, to prevent aliasing of the input signal, the bandwidth of the analog input signal must be band limited. The bandwidth is a function of the system clock frequency. With a system clock frequency of 9.6MHz, the data output rate is 25kHz, with a –3dB frequency of 5.4kHz. The –3dB frequency scales with the system clock frequency.

To guarantee the best linearity of the ADS1250, a fully differential signal is recommended.

PROGRAMMABLE GAIN AMPLIFIER

The PGA gain setting is programmed via the PGA pins on the ADS1250. Changes in the gain setting (G) of the PGA results in an increase in the input capacitor size. Therefore, higher gain settings result in a lower analog input impedance.

The PGA of the ADS1250 can be set to a gain of 1, 2, 4, or 8, substantially increasing the dynamic range of the converter and simplifying the interface to the more common transducers (see Table I).

GAIN SETTING			ANALOG INPUT	
G1	G0	GAIN VALUE	DIFFERENTIAL FSR (V)	SINGLE-ENDED FSR (V)
0	0	1	8.192	4.096
0	1	2	4.096	2.048
1	0	4	2.048	1.024
1	1	8	1.024	0.512

NOTE: Based on a 4.096V reference. The ADS1250 allows common-mode voltage as long as the absolute input voltage on $+V_{IN}$ or $-V_{IN}$ does not go below AGND or above $+V_S$.

TABLE I. Full-Scale Range versus PGA Setting.

DELTA-SIGMA MODULATOR

The modulator clock is generated by dividing the system clock by 6. With a nominal system clock frequency of 9.6MHz, the modulator clock frequency is 1.6MHz (9.6MHz / 6). The output from the modulator is oversampled 64 times by the digital filter. Therefore, with 1.6MHz modulator clock (derived from a 9.6MHz system clock), the data output rate is 25kHz (1.6MHz / 64). The data output rate scales directly with the system clock frequency, as shown in Table II.

CLK (MHz)	DATA OUTPUT RATE (Hz)
9.600000	25,000
7.372800[1]	19,200
6.144000[1]	16,000
6.000000[1]	15,625
4.915200[1]	12,800
3.686400[1]	9,600
3.072000[1]	8,000
2.457600[1]	6,400
1.843200[1]	4,800
0.921600	2,400
0.460800	1,200
0.384000	1,000
0.192000	500
0.038400	100
0.023040	60
0.019200	50
0.011520	30
0.009600	25
0.007680	20
0.006400	16.67
0.005760	15
0.004800	12.50
0.003840	10

NOTE: (1) Standard Clock Oscillator.

TABLE II. CLK Rate versus Data Output Rate.

REFERENCE INPUT

Unlike the analog input, the reference input impedance has no dependency on the PGA gain setting.

Reference input takes an average current of 125µA with a 9.6MHz system clock. This current will be proportional to the system clock. A buffered reference is needed for ADS1250. The recommended reference circuit is shown in Figure 2.

Reference voltages higher than 4.096V will increase the full-scale range, while the absolute internal circuit noise of the converter remains the same. This will decrease the noise in terms of ppm of full scale. However, using a higher reference voltage will also degrade linearity. Therefore, the use of a higher reference voltage is not recommended.

Reference voltages lower than 4.096V will decrease the full-scale range, while the absolute internal circuit noise at the converter remains the same. This will increase the noise in terms of ppm of full scale. However, using a lower reference voltage will not degrade linearity. Therefore, the use of a lower reference voltage will reduce the effective resolution.

DIGITAL FILTER

The digital filter is a sinc^5 and is described by the following transfer function:

$$|H(f)| = \left| \frac{\sin\left(\frac{\pi \cdot f \cdot 64}{f_{MOD}}\right)}{64 \cdot \sin\left(\frac{\pi \cdot f}{f_{MOD}}\right)} \right|^5$$

or

$$H(z) = \left(\frac{1 - z^{-64}}{64 \cdot \left(1 - z^{-1}\right)} \right)^5$$

The digital filter of the ADS1250 computes the digital result based on the most recent outputs from the delta-sigma modulator. At the most basic level, the digital filter can be thought of as simply averaging the modulator results in a weighted form and presenting this average as the digital result. The digital result is calculated from the digital filter every 64 modulator clock cycles, or 6 • 64 = 384 system clock cycles (refer to the Delta-Sigma Modulator section). However, if there is a significant change in the analog input, five full conversions are needed for the digital filter to settle. If the analog input change occurs asynchronously to the $\overline{DRDY}$ pulse, six conversions are needed for the conversion to fully settle. Furthermore, the group delay is only 2.5 conversions due to the digital filter's linear phase response.

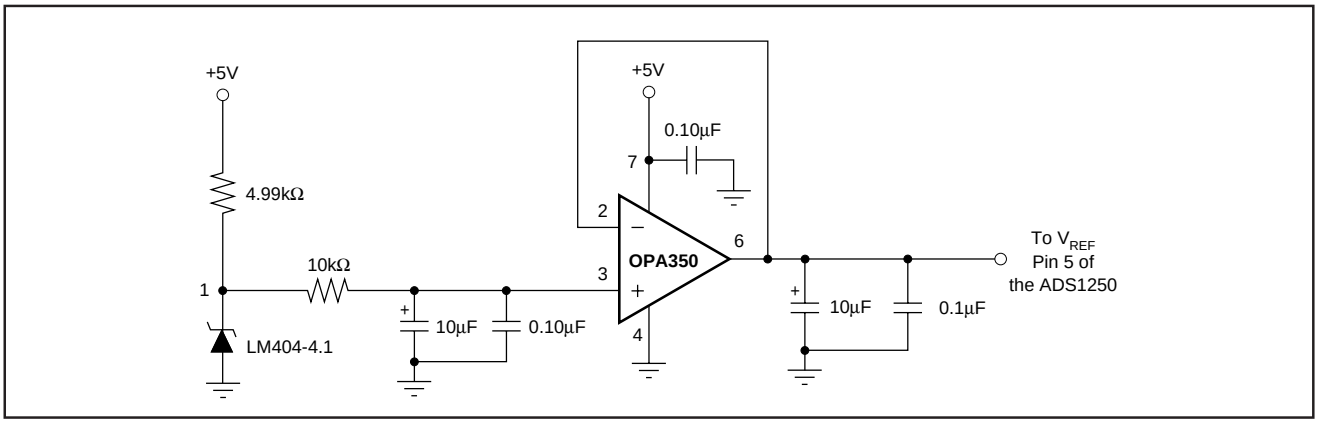


FIGURE 2. Recommended External Voltage Reference Circuit for Best Low Noise Operation with the ADS1250.

The digital output rate, or data rate, scales directly with the system CLK frequency. This allows the data output rate to be changed over a very wide range (five orders of magnitude) by changing the system CLK frequency. However, it is important to note that the –3dB point of the filter is 0.216 times the data output rate. Therefore, the data output rate should allow for sufficient margin to prevent attenuation of the signal of interest.

Since the conversion result is essentially an average, the data output rate determines the location of the resulting notches in the digital filter (see Figure 3). Note that the first notch is located at the data output rate frequency, and subsequent notches are located at integer multiples of the data output rate to allow for rejection of not only the fundamental frequency, but also harmonic frequencies. In this manner, the data output rate can be used to set specific notch frequencies in the digital filter response.

For example, if rejection of the power line frequency is desired, the data output rate can simply be set to the power line frequency. For 50Hz rejection, the system CLK frequency should be 19.200kHz; this will set the data output rate to 50Hz (see Table II and Figure 4). For 60Hz rejection, the system CLK frequency should be 23.040kHz; this will set the data output rate to 60Hz (see Table II and Figure 5). If both 50Hz and 60Hz rejection is required, then the system CLK should be 3.840kHz; this will set the data output rate to 10Hz and reject both 50Hz and 60Hz (See Table II and Figure 6).

There is an additional benefit in using a lower data output rate. It will provide better rejection of signals in the frequency band of interest. For example, with a 50Hz data output rate, a significant signal at 75Hz may alias back into the passband at 25Hz. This is due to the fact that rejection at 75Hz may only be 66dB in the stopband (frequencies higher than the first notch frequency), as shown in Figure 4. However, setting the data output rate to 10Hz will provide 135dB rejection at 75Hz (see Figure 6). A similar benefit is gained at frequencies near the data output rate (see Figures 7, 8, 9, and 10). If a slower data output rate does not meet the system requirements, the analog front end can be designed to provide the needed attenuation to prevent aliasing. Additionally the data output rate may be increased and additional digital filtering may be done in the processor or controller.

CONTROL LOGIC

The control logic is used for communications and control of the ADS1250.

Power-Up Sequence

Prior to power-up, all digital and analog input pins must be LOW. At the time of power-up, these signal inputs can be biased to a voltage other than 0V, however, they should never exceed $+V_S$ or $+V_D$.

Once the ADS1250 powers up, the $\overline{\text{DRDY}}$ line will pulse LOW on the first conversion. This data will not be valid. The sixth pulse of $\overline{\text{DRDY}}$ will be valid data from the analog input signal.

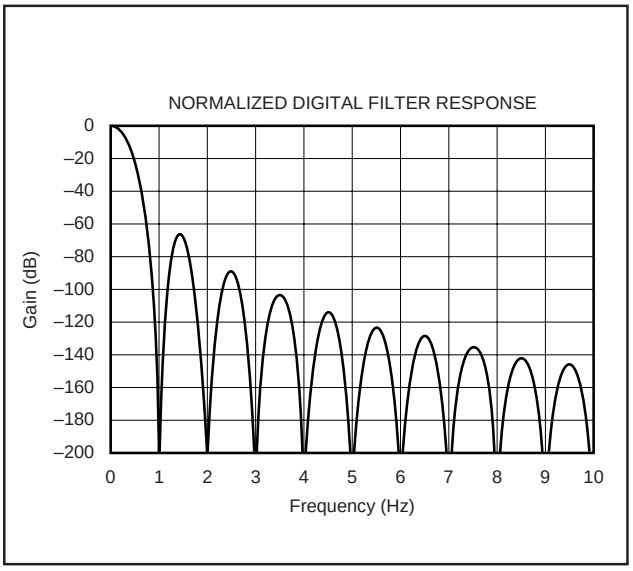


FIGURE 3. Normalized Digital Filter Response.

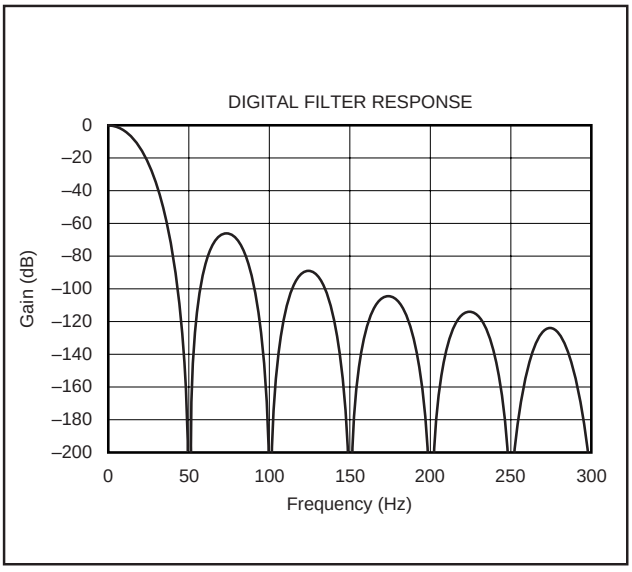


FIGURE 4. Digital Filter Response (50Hz).

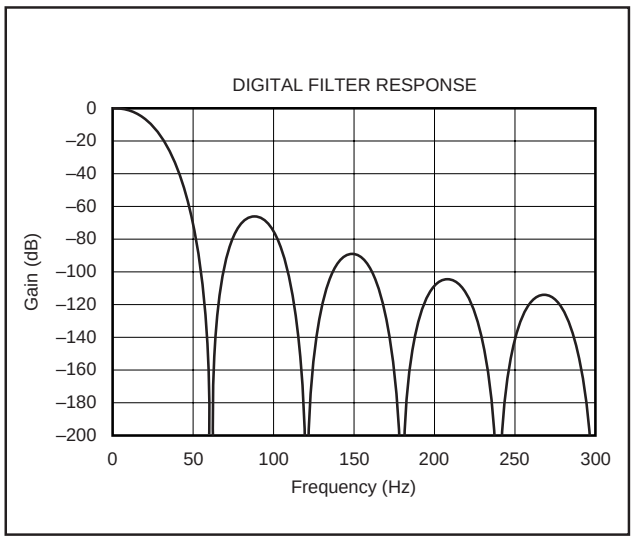


FIGURE 5. Digital Filter Response (60Hz).

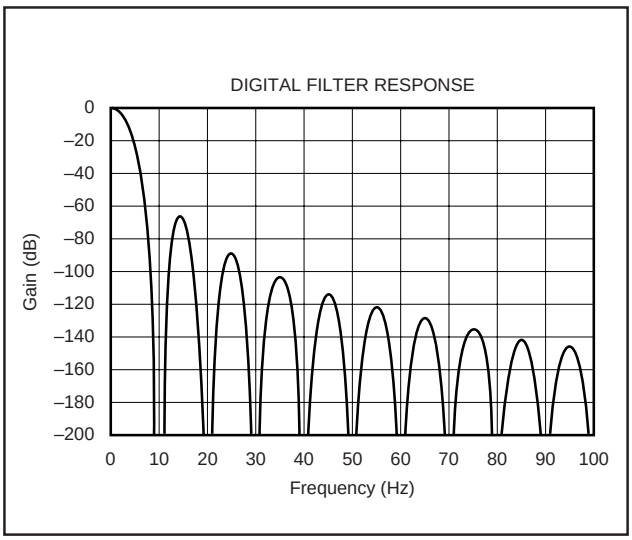


FIGURE 6. Digital Filter Response (10Hz Multiples).

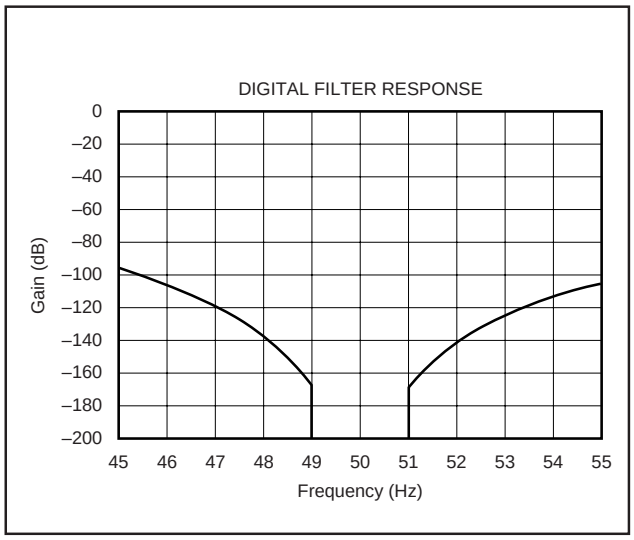


FIGURE 7. Expanded Digital Filter Response (50Hz with a 50Hz Notch).

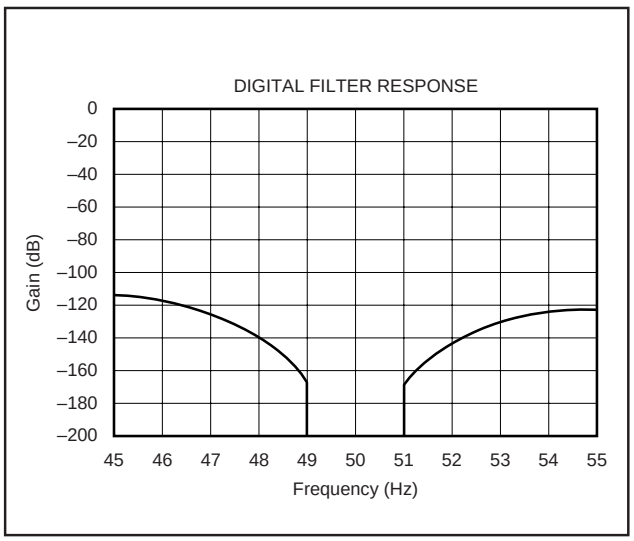


FIGURE 8. Expanded Digital Filter Response (50Hz with a 10Hz Notch).

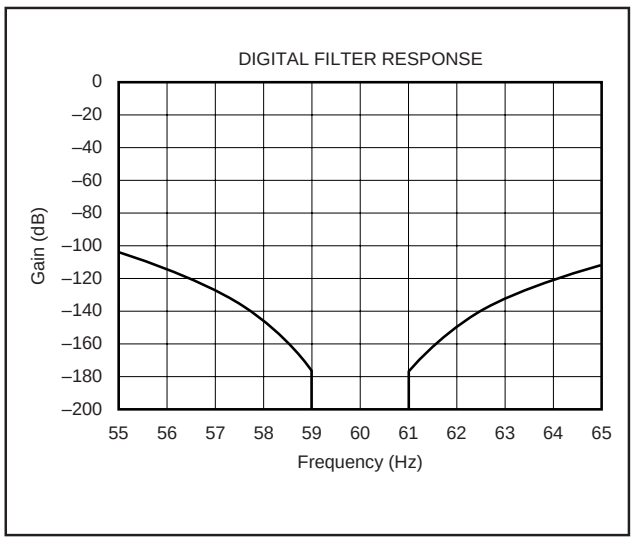


FIGURE 9. Expanded Digital Filter Response (60Hz with a 60Hz Notch).

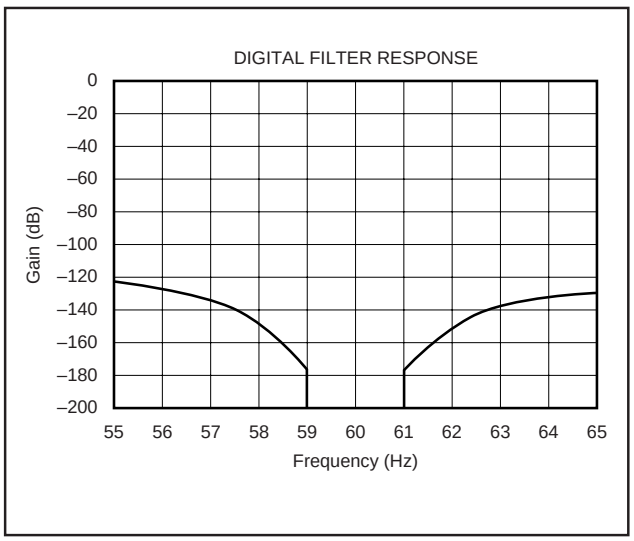


FIGURE 10. Expanded Digital Filter Response (60Hz with a 10Hz Notch).

$\overline{\text{DSYNC}}$

The $\overline{\text{DSYNC}}$ signal can be used is two ways. First, $\overline{\text{DSYNC}}$ can be used to synchronize multiple converters. This is done by applying a negative-going pulse on $\overline{\text{DSYNC}}$. The negative pulse resets the current modulator count to zero and places it in a hold state. The modulator is released from the hold state and synchronization occurs on the rising edge of $\overline{\text{DSYNC}}$. $\overline{\text{DSYNC}}$ does not reset the internal data to zero. Synchronization assumes that each ADS1250 is driven from the same system clock. If the $\overline{\text{DSYNC}}$ pulse is completely asynchronous to the master clock, some ADS1250s may start-up one CLK clock cycle before the others. Therefore, the output data will be synchronized, but only to within one CLK clock cycle. To ensure exact synchronization to the same CLK clock edge, the timing relationship between the $\overline{\text{DSYNC}}$ and CLK signals must be observed, as shown in Figure 11 and Table III. Figure 12 shows a simple circuit which can be used to clock multiple ADS1250s from one ADS1250, as well as to ensure that an asynchronous $\overline{\text{DSYNC}}$ signal will exactly synchronize all the converters.

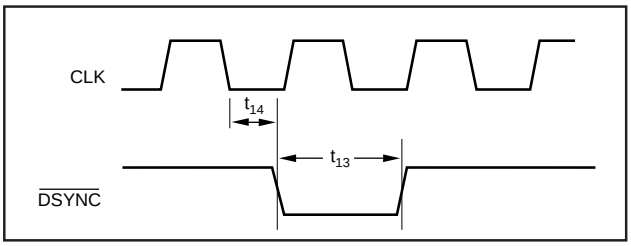


FIGURE 11. $\overline{\text{DSYNC}}$ to CLK Timing for Synchronizing Multiple ADS1250s.

The second use of $\overline{\text{DSYNC}}$ is to reset the modulator count to zero in order to obtain valid data as quickly as possible. For example, if the analog input signal is changed significantly on the ADS1250, the current conversion cycle will be a mix of the old data and the new data. Five conversions are needed for the digital filter to settle. Therefore, the sixth conversion will be valid data. However, if the analog input signal is changed and then $\overline{\text{DSYNC}}$ is used to reset the modulator count, the modulator data at the end of the current conversion cycle will be entirely from the new signal. After four additional conversion cycles, the output data will be completely valid. Note that the conversion cycle in which $\overline{\text{DSYNC}}$ is used will be slightly longer than normal. Its length will depend on when $\overline{\text{DSYNC}}$ was set.

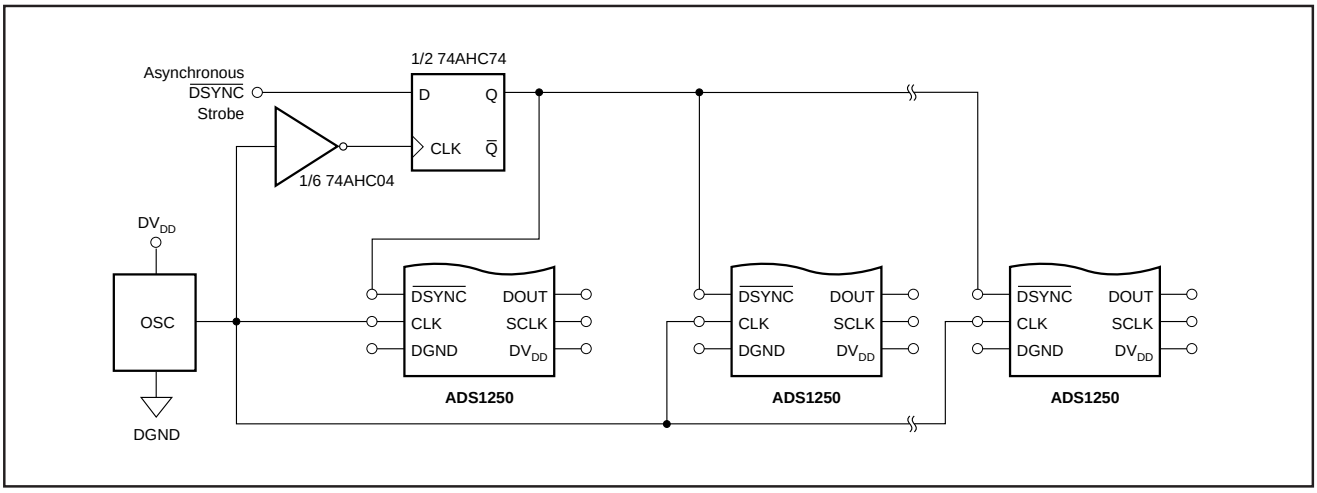


FIGURE 12. Exactly Synchronizing Multiple ADS1250s to an Asynchronous $\overline{\text{DSYNC}}$ Signal.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_1	DOR Write Time (Using $\overline{\text{CS}}$)			6 • CLK	ns
t_2	$\overline{\text{DRDY}}$ LOW Time			6 • CLK	ns
t_3	DOR Write Time ($\overline{\text{CS}}$ HIGH)			6 • CLK	ns
t_4	$\overline{\text{DRDY}}$ HIGH Time			6 • CLK	ns
t_5	Rising Edge of CLK to Falling Edge of $\overline{\text{DRDY}}$			30	ns
t_6	Falling Edge of $\overline{\text{DRDY}}$ to Falling Edge of $\overline{\text{CS}}$	30			ns
t_7	Falling Edge of $\overline{\text{CS}}$ to Rising Edge of $\overline{\text{DRDY}}$			6 • CLK	ns
t_8	Falling Edge of $\overline{\text{CS}}$ to Rising Edge of SCLK or Falling Edge of $\overline{\text{DRDY}}$ to Rising Edge of SCLK if $\overline{\text{CS}}$ is Tied LOW	30			ns
t_9	Falling Edge of $\overline{\text{CS}}$ to DOUT Valid or Falling Edge of $\overline{\text{DRDY}}$ to DOUT Valid if $\overline{\text{CS}}$ is Tied LOW (Setup Time)			30	ns
t_{10}	Falling Edge of SCLK to DOUT Valid (Hold Time)	5			ns
t_{11}	Falling Edge of SCLK to Next DOUT Valid (Setup Time)			30	ns
t_{12}	Rising Edge of $\overline{\text{CS}}$ to DOUT High Impedance			30	ns
t_{13}	$\overline{\text{DSYNC}}$ Pulse Width	100			ns
t_{14}	Falling Edge of CLK to Falling Edge of $\overline{\text{DSYNC}}$			$\frac{\text{CLK}}{2} - 5$	ns

TABLE III. Digital Timing.

$\overline{CS}$

The $\overline{CS}$ signal controls the state of DOUT. If $\overline{CS}$ is HIGH, DOUT is in a high-impedance state. When $\overline{CS}$ is LOW, DOUT drives the bus.

$\overline{DRDY}$

The $\overline{DRDY}$ signal is used to indicate that new data has been loaded into the data output register and is ready to be read. The operation of $\overline{DRDY}$ depends on how the $\overline{CS}$ signal is used. The specifics of the three communications methods are described in the Serial Interface section.

In the first case, which is typical for three-wire serial communications ($\overline{CS}$ tied LOW), $\overline{DRDY}$ would normally be HIGH. The result of the A/D conversion would be written to the DOR from MSB to LSB in the time defined by t_1. The $\overline{DRDY}$ line would then pulse LOW for time defined by t_2, as shown in Figure 13.

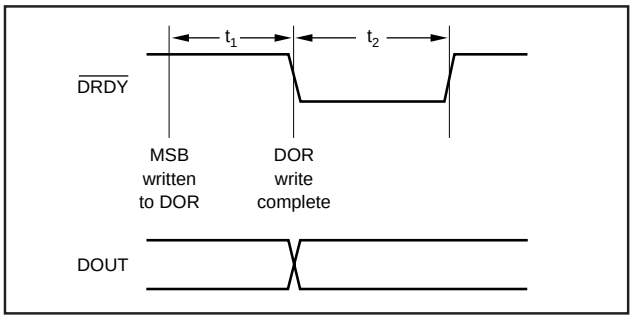


FIGURE 13. $\overline{DRDY}$ Pulse ($\overline{CS}$ tied LOW).

In the second case, which is typical for four-wire serial communications ($\overline{CS}$ used), $\overline{DRDY}$ would normally be HIGH. The result of the A/D conversion would be written to the DOR from MSB to LSB in the time defined by t_1. The $\overline{DRDY}$ would go LOW after the DOR write is completed. After taking $\overline{CS}$ LOW, the $\overline{DRDY}$ line would remain LOW for the time defined by t_2, as shown in Figure 14.

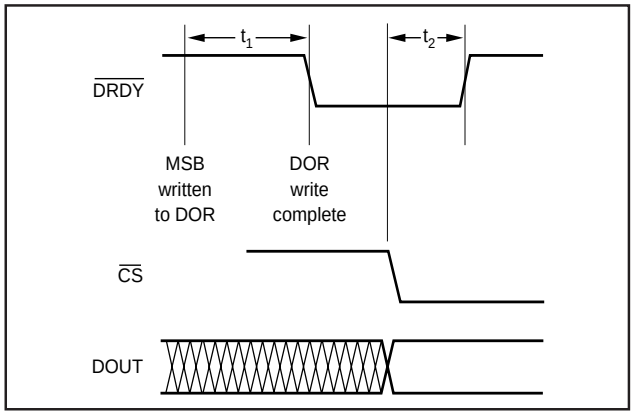


FIGURE 14. $\overline{DRDY}$ Pulse (using $\overline{CS}$).

In the third case, $\overline{CS}$ is left HIGH, which may be used if data is only periodically read from the ADS1250. In this case, $\overline{DRDY}$ would normally be LOW. $\overline{DRDY}$ would go HIGH immediately prior to the MSB being written to the DOR. The result of the A/D conversion would be written from MSB to LSB in the time defined by t_3. The $\overline{DRDY}$ line would stay HIGH for the time defined by t_4, as shown in Figure 15.

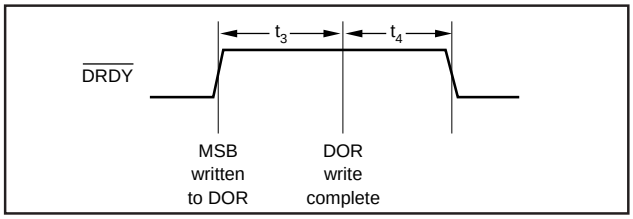


FIGURE 15. $\overline{DRDY}$ Pulse ($\overline{CS}$ HIGH).

Reading $\overline{DRDY}$ during the time shown by t_1 and t_3 (Figures 13, 14, and 15) will result in invalid data being read. This is due to the fact that writes to the DOR are not blocked. Subsequently, a read from DOR during this time will result in a combination of old and new data.

SERIAL INTERFACE

The ADS1250 includes a simple serial interface which can be connected to microcontrollers and digital signal processors in a variety of ways. Communications with the ADS1250 can commence on the first detection of the $\overline{DRDY}$ pulse after power up, although data will not be valid until the sixth conversion.

It is important to note that the data from the ADS1250 is a 20-bit result transmitted MSB-first in Binary Two's Complement format, as shown in Table IV.

DIFFERENTIAL VOLTAGE INPUT	DIGITAL OUTPUT (HEX)
+Full Scale	7FFFFH
Zero	00000H
–Full Scale	80000H

TABLE IV. ADS1250 Data Format (Binary Two's Complement).

The entire 20-bit result can be read out of the device by simply providing 20 SCLKs during serial communication with the part. However, the most common method of communicating with the device is with a standard SSI interface, such as SPI. This protocol is based on 8-bit or 16-bit data transfers. It is possible to use a standard 8-bit or 16-bit data transfer with the ADS1250. For instance, if only 16 bits of data are read, the internal bit pointer will automatically reset to the MSB of the DOR on the next $\overline{DRDY}$ pulse. This will ensure that the next read from the DOR will begin with the MSB of newly converted data. If more than 20 bits of data are read, the data will be 0 padded. Therefore, if 24 bits of data are read from the ADS1250, the lowest four bits of the 24-bit data transfer are read as 0s (0 padded).

The only limitation on SCLK is that it cannot be higher than 9.6MHz. Therefore, it is possible to run CLK at a lower frequency than SCLK. For instance, it is possible to run CLK at 23.040kHz for a 60Hz notch, and run SCLK at 9.6MHz to achieve high-speed serial communications. Additionally, the data must be clocked out before the next $\overline{DRDY}$ to ensure valid data, as described in the $\overline{DRDY}$ section.

There are three basic methods of receiving data from the ADS1250. The first two methods involve a four-wire interface and the third method is a three-wire interface.

Method 1: Four-Wire Interface

The most common method of receiving data is using a simple four-wire interface ($\overline{CS}$, SCLK, DOUT, and $\overline{DRDY}$). The $\overline{DRDY}$ line will pulse LOW after the DOR is updated. The processor would then take $\overline{CS}$ LOW to select the device for communication. Once $\overline{CS}$ is taken LOW, the DOUT would be driven to the level dictated by the MSB of the data output register. The processor would provide 20 (or 24) SCLKs to read the contents of the DOR. The data bits in the DOR are shifted out on the DOUT pin after the falling edge of SCLK. If more than 20 bits of data are read, the data is 0 padded. Taking $\overline{CS}$ HIGH will take DOUT to a high-impedance state. The timing for the data transfer is shown in Figure 16 (see Table III). A simple four-wire interface using this method is shown in Figure 17. The P1.0 output from the 8xC51 is a free-running clock.

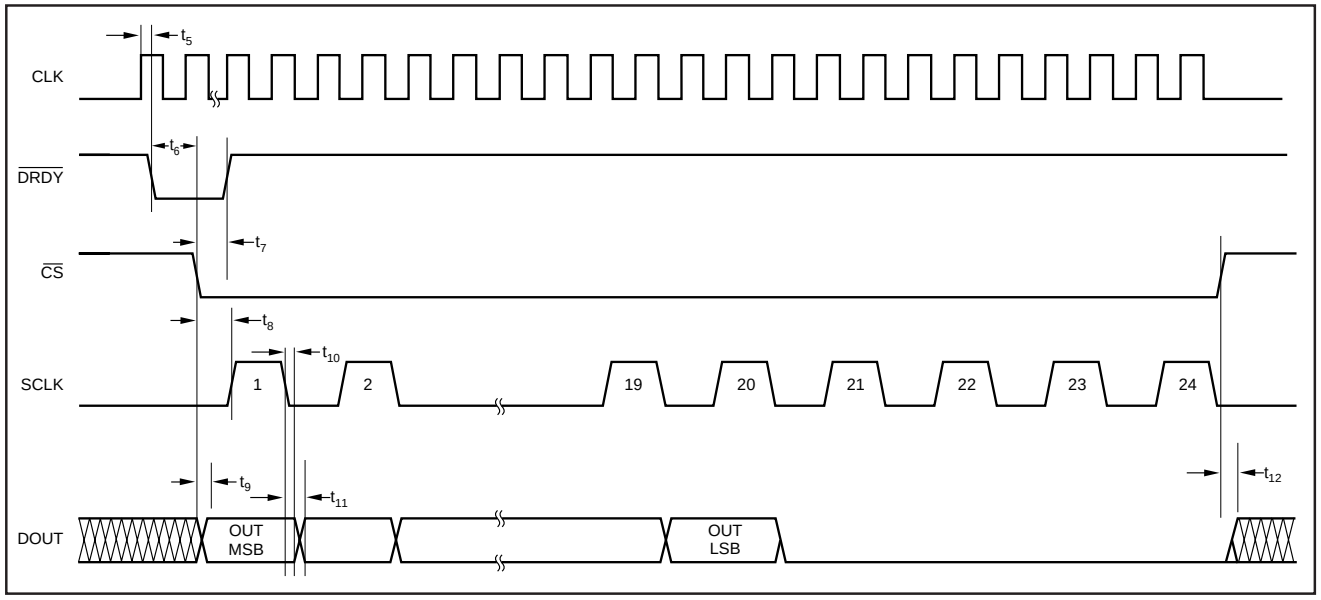


FIGURE 16. Method 1: Four-Wire Interface Using Noncontinuous SCLK.

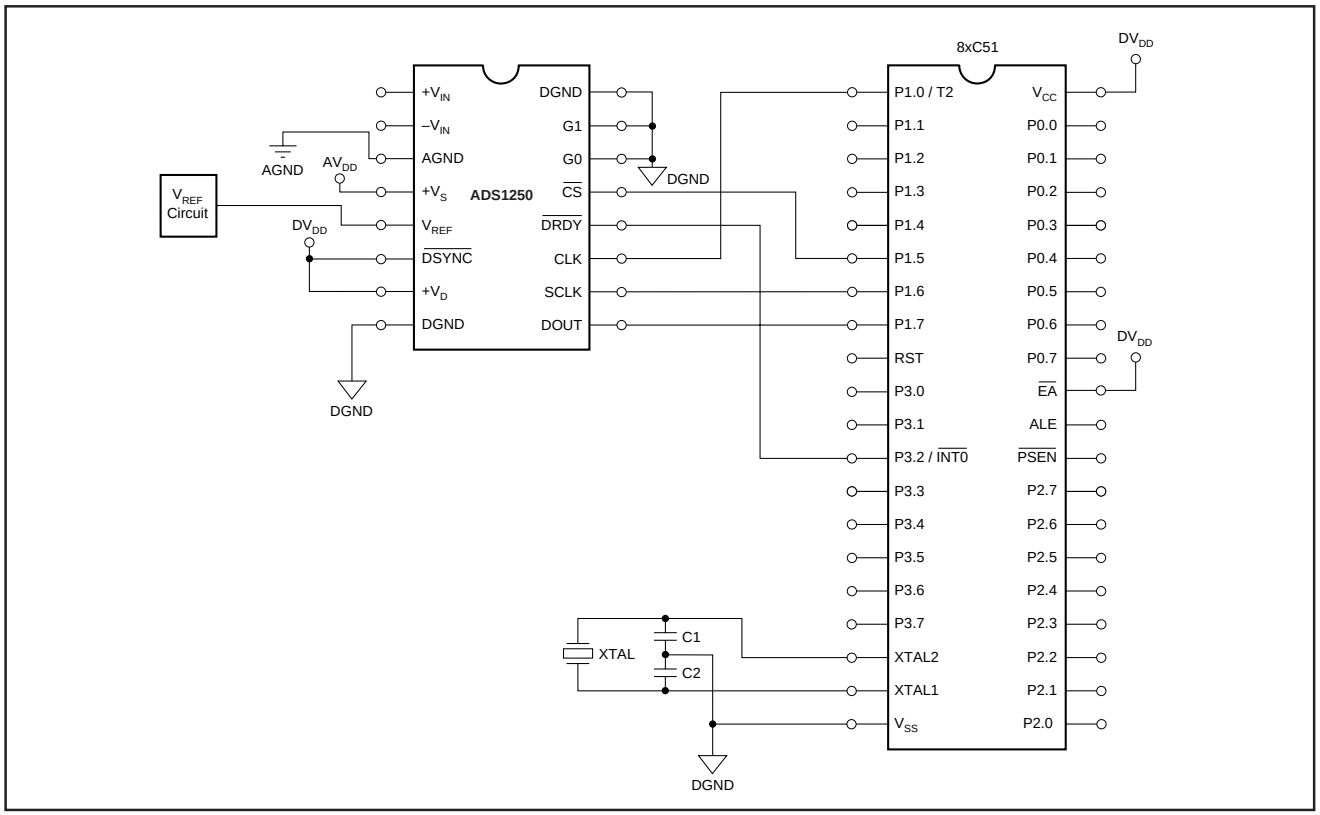


FIGURE 17. Four-Wire Interface to an 8xC51.

Method 2: Four-Wire Interface

The second method of receiving data also uses a simple four-wire interface ($\overline{CS}$, SCLK, DOUT, and $\overline{DRDY}$). The main difference from method 1 is that SCLK is a free-running clock. The $\overline{DRDY}$ line will pulse LOW for the time defined by t_2 after the DOR is updated. The processor would then take $\overline{CS}$ LOW to select the device for communication. The recommended method of using $\overline{CS}$ is to take $\overline{CS}$ LOW on the falling edge of SCLK. The only timing constraint of $\overline{CS}$ is that the setup time (t_9) for the data must be met before the rising edge of SCLK. Once $\overline{CS}$ is taken LOW, the DOUT would be driven to the level dictated by the MSB of the data output register. $\overline{CS}$ would be held low for 20 (or 24) SCLKs to read the contents of the DOR. The data bits in the DOR are shifted out on the DOUT pin after the falling edge of SCLK. If $\overline{CS}$ is held low for more than 20 SCLKs, the data would be 0 padded. Taking $\overline{CS}$ HIGH will take DOUT to a high-impedance state. The timing for the data transfer is shown in Figure 18 (see Table III). A simple four-wire interface is shown in Figure 19. The P1.0 output from the 8xC51 is a free-running clock.

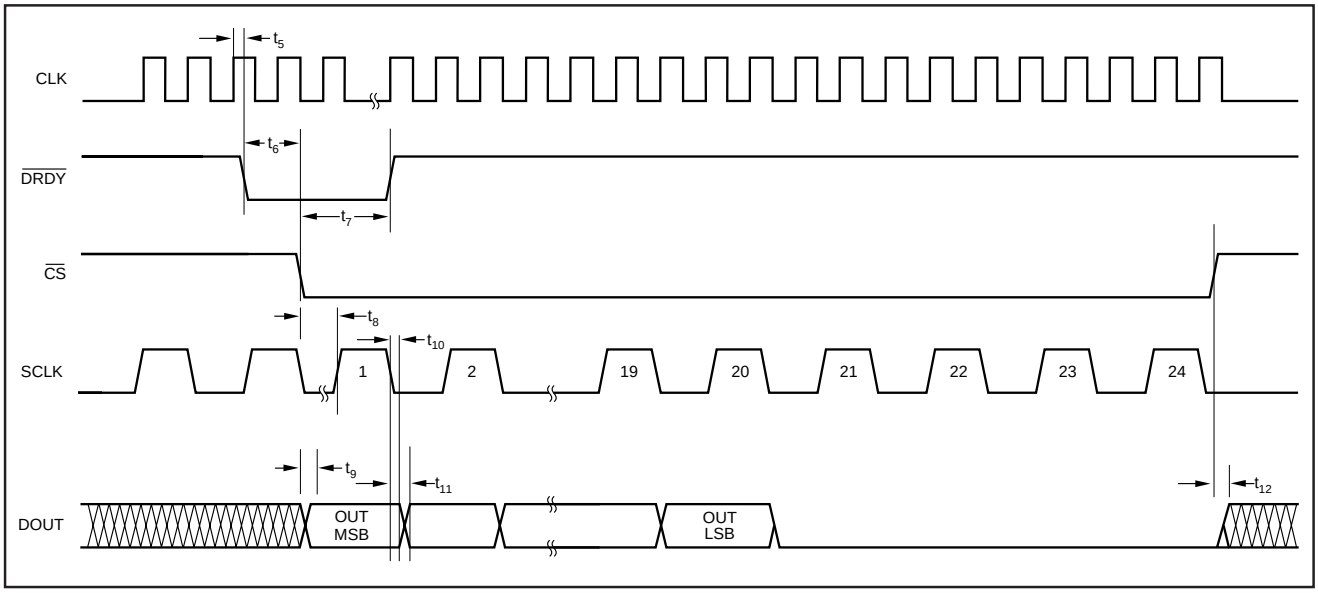


FIGURE 18. Method 2: Four-Wire Interface Using a Free-Running SCLK.

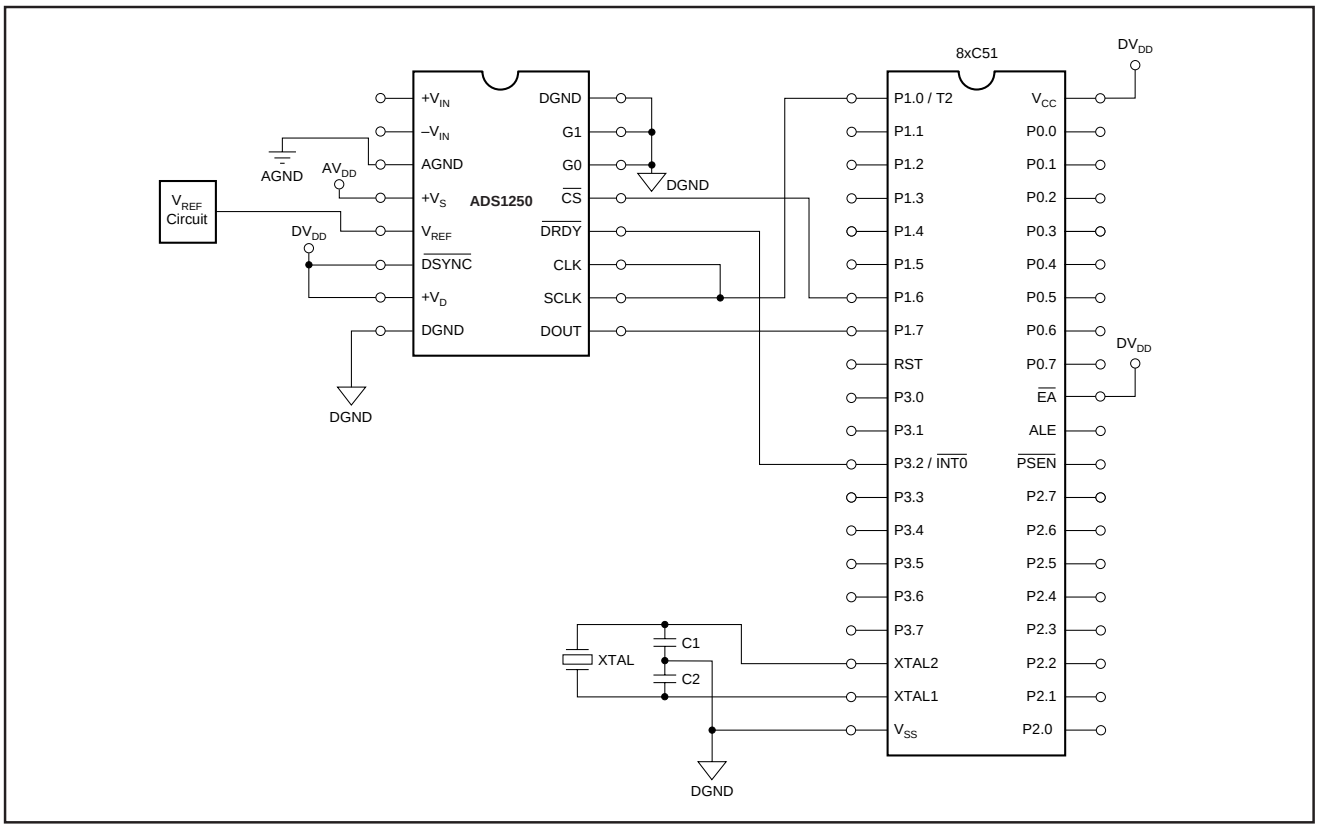


FIGURE 19. Four-Wire Interface to an 8xC51 (Free-Running SCLK).

Method 3: Three-Wire Interface

The third method of receiving data uses a simple three-wire interface (SCLK, DOUT, and $\overline{DRDY}$). The main difference from method 1 is that $\overline{CS}$ is tied LOW, therefore, the DOUT pin is always driving the bus. The $\overline{DRDY}$ line will pulse LOW after the DOR is updated. Since $\overline{CS}$ is tied LOW (the DOUT pin is enabled for output), the level dictated by the MSB of the data output register would be driven on the bus. The processor would provide 20 (or 24) SCLKs to read the contents of the DOR. The data bits in the DOR are shifted out on the DOUT pin after the falling edge of SCLK. If more than 20 bits of data are read, the data is 0 padded. Since $\overline{CS}$ is tied LOW, the bus will be driven to the state of the last bit that was shifted out of the DOR. The timing for the data transfer is shown in Figure 20 (see Table III). A simple three-wire interface using this method is shown in Figure 21. The P1.0 output from the 8xC51 is a free-running clock.

Figure 22 shows a five-wire interface using $\overline{DSYNC}$. The communication with the ADS1250 is the same as described in Method 1. Figure 23 shows a full interface using $\overline{DSYNC}$, G1, and G0. The communication with ADS1250 is the same as described in Method 1.

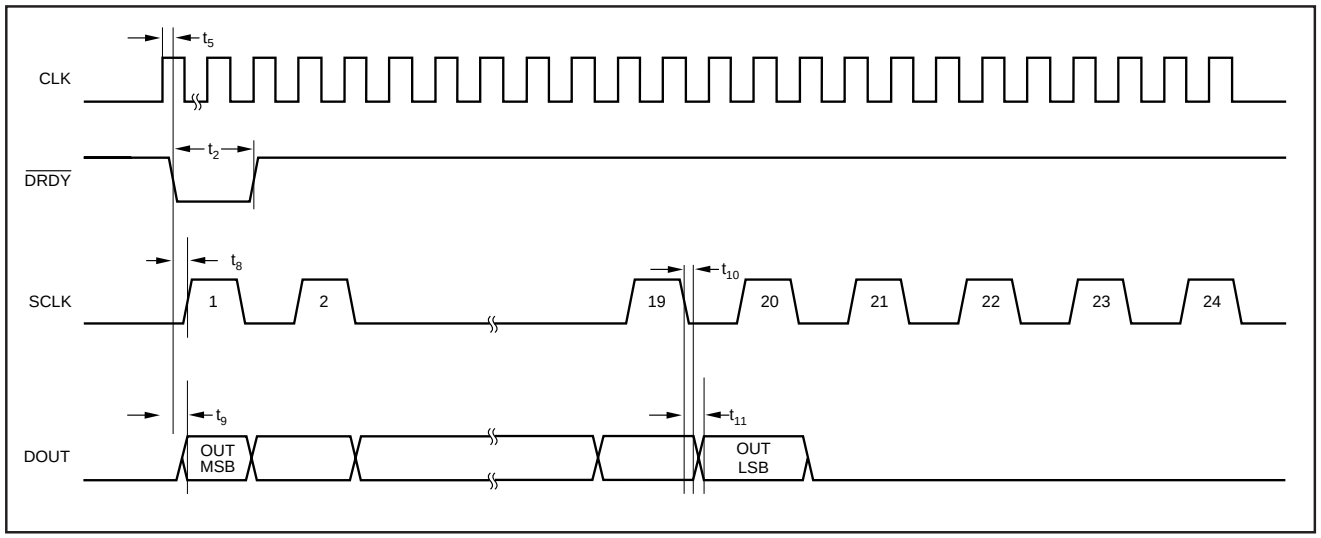


FIGURE 20. Method 3: Two-Wire Interface ($\overline{CS}$ tied LOW).

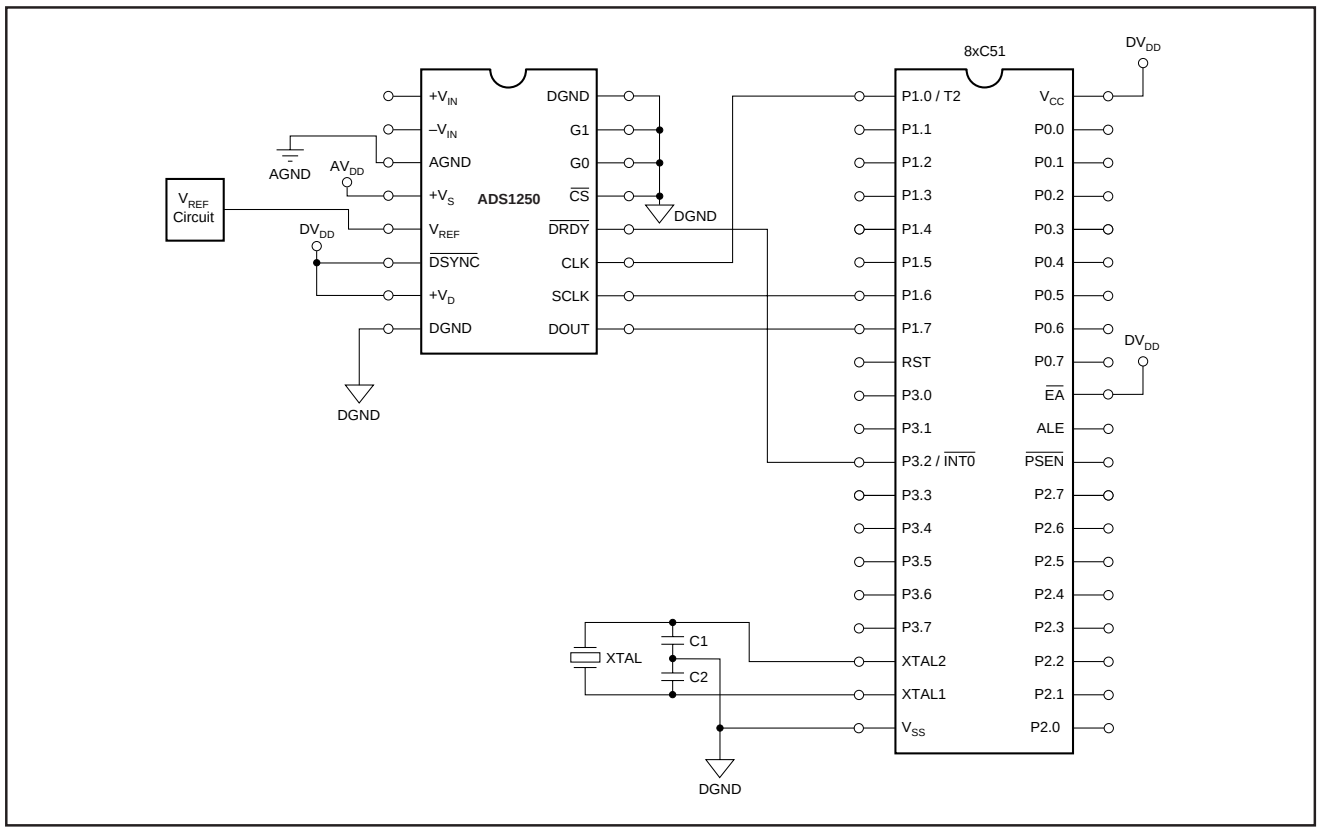


FIGURE 21. Three-Wire Interface to an 8xC51 ($\overline{CS}$ tied LOW).

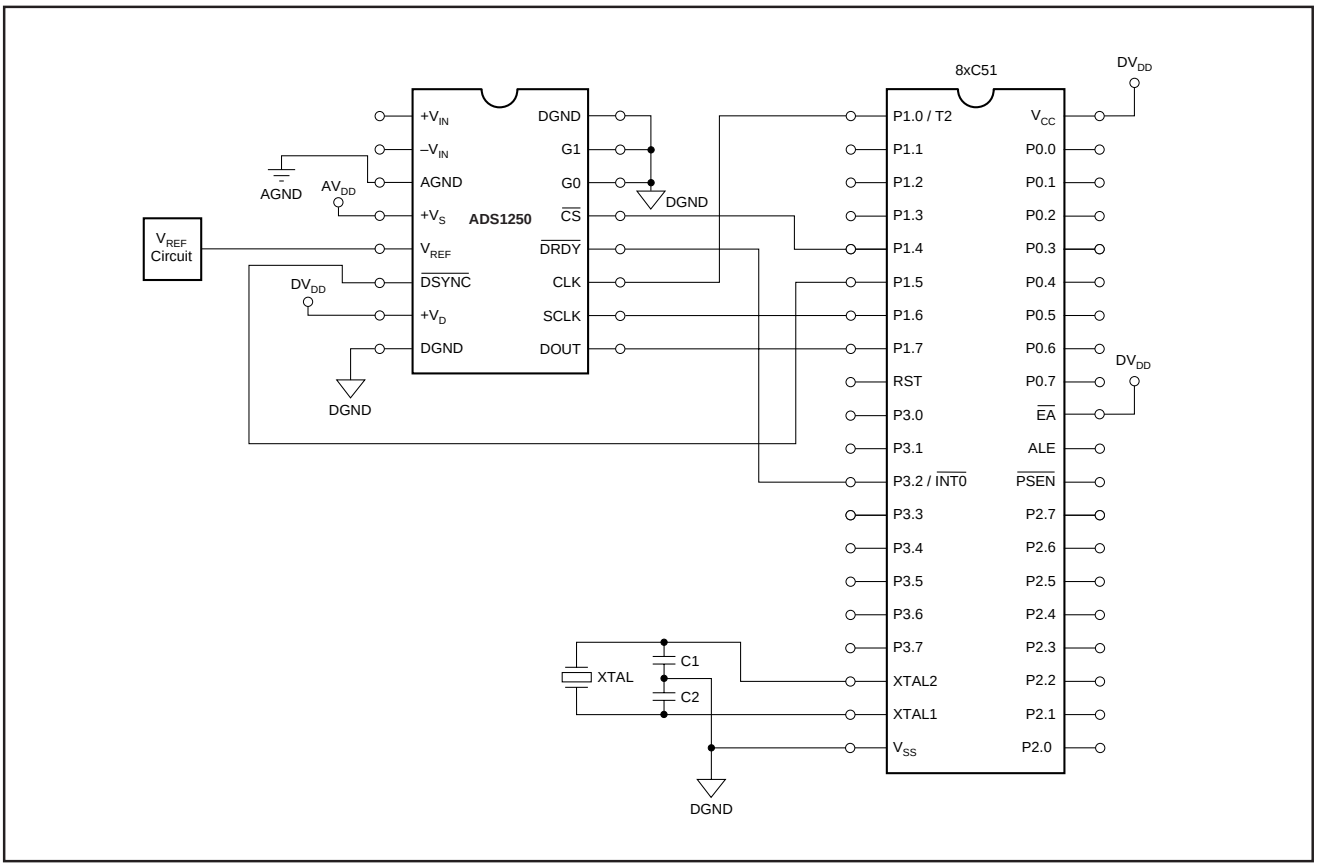


FIGURE 22. Five-Wire Interface to an 8xC51.

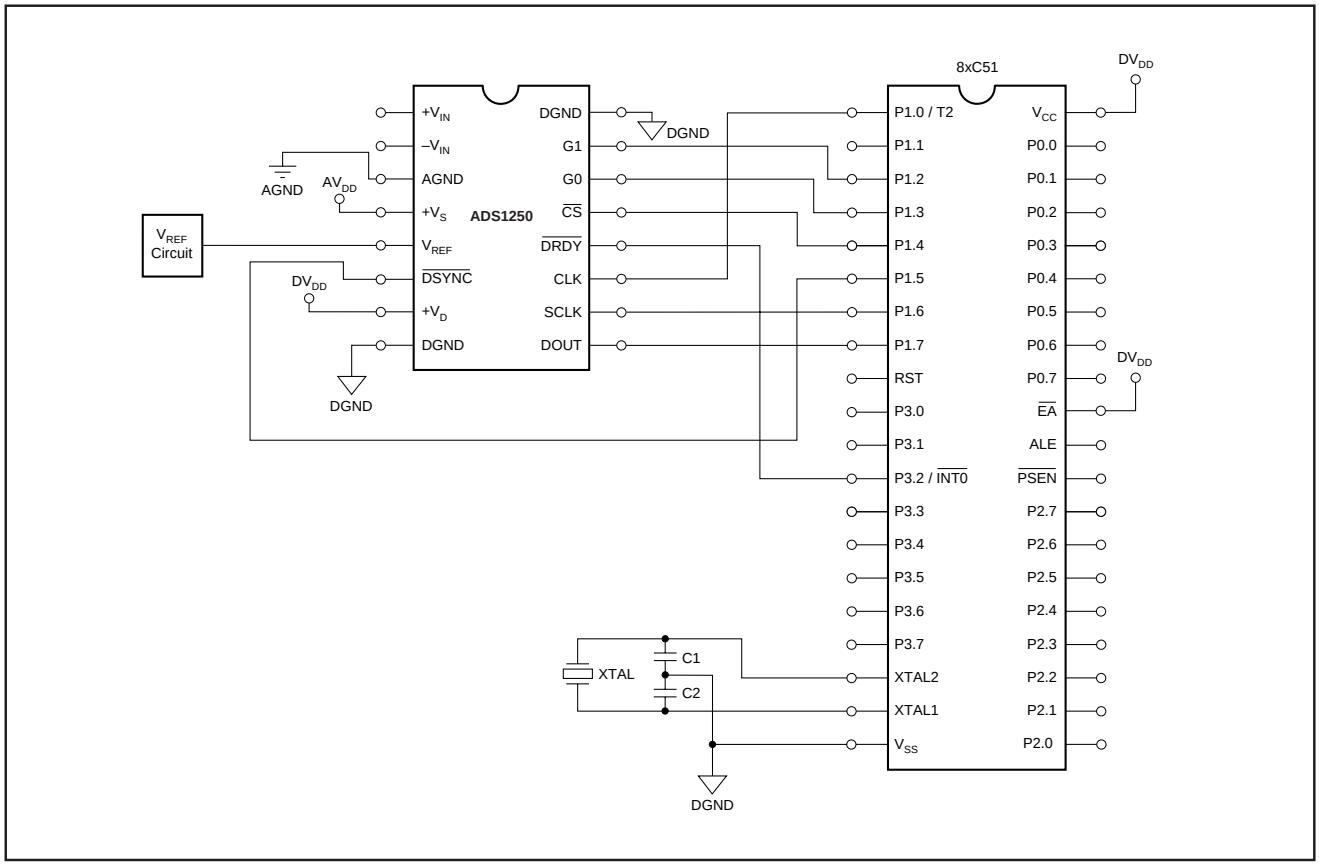


FIGURE 23. Full Interface to an 8xC51.

SOFTWARE GAIN

The excellent performance, flexibility, and low cost of the ADS1250 allows the converter to be considered for designs which would not normally need a 20-bit ADC. For example, many designs utilize a 12-bit converter and a high gain INA or PGA for digitizing low amplitude signals. For some of these applications, the ADS1250 by itself may be a solution. The digital result of the converter can simply be shifted up by "n" bits in the main controller, resulting in a gain of "n" times G, where G is the gain setting. While this type of manipulation of the output data is obvious, it is easy to miss how much the gain can be increased in this manner on a 20-bit converter. For example, shifting the result by 4 bits when the ADS1250 is set to a gain of 8 results in an effective gain of 128.

Isolation

The serial interface of the ADS1250 provides for simple isolation methods. An example of an isolated four-wire interface is shown in Figure 19. The ISO150 is used to transmit the digital clocks over the isolation barrier. In addition, the digital output of the ADS1250 can, in some cases, drive opto-isolators directly. Note that DOUT is tri-stated for the majority of the conversion period and the opto-isolator connection must take this into account.

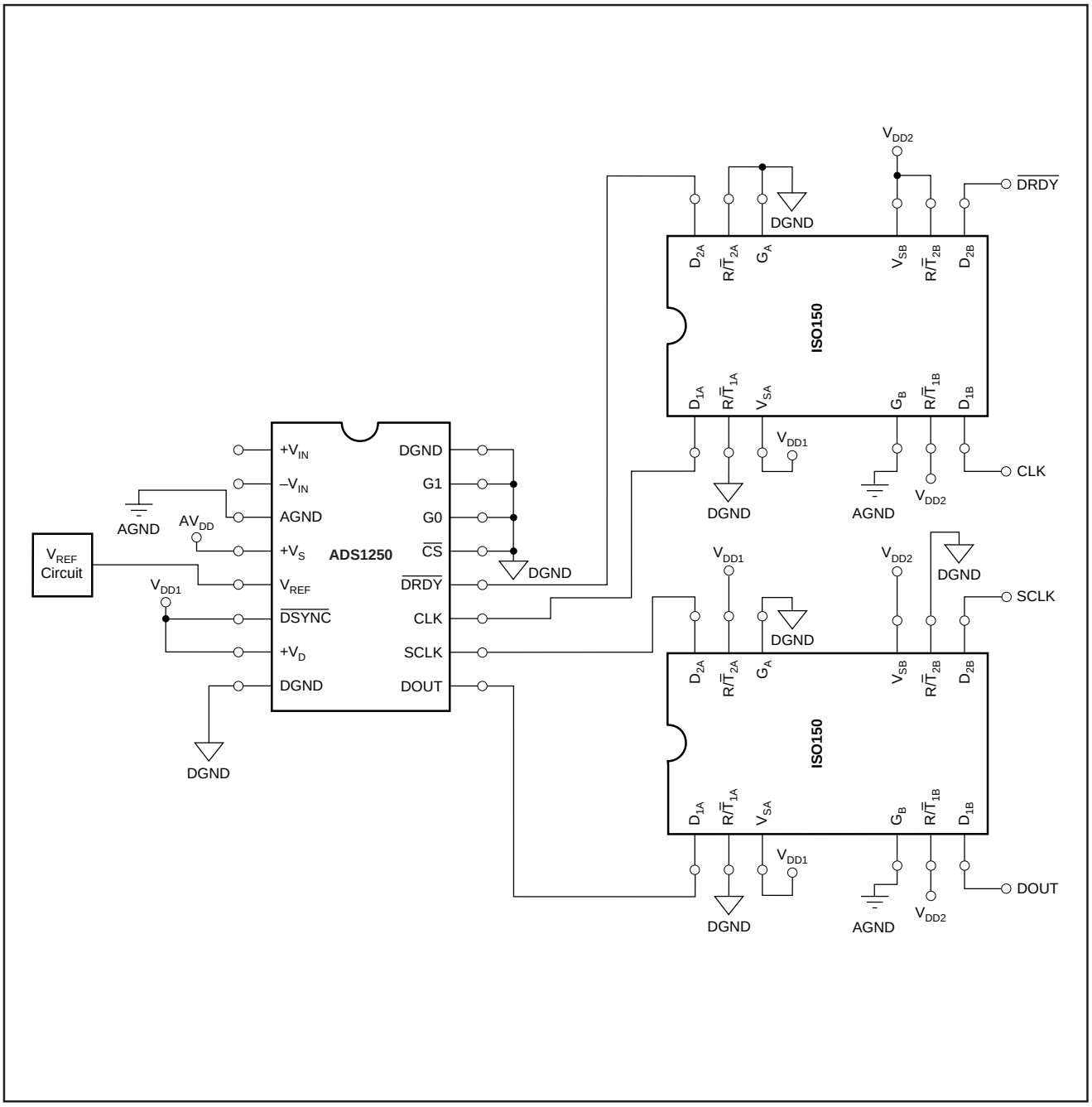


FIGURE 24. Isolated Four-Wire Interface.

LAYOUT

POWER SUPPLIES

The analog supply should be well regulated and low noise. For designs requiring very high resolution from the ADS1250, power supply rejection will be a concern. Avoid running digital lines under the device as they may couple noise onto the die. The requirements for the digital supply are not as strict, however, high frequency noise on V_D can capacitively couple into the analog portion of the ADS1250. This noise can originate from switching power supplies, very fast microprocessors, or digital signal processors. For either supply, high frequency noise will alias back into the pass-band of the digital filter, affecting the conversion result. If one supply must be used to power the ADS1250, the V_S supply should be used to power V_D. This connection can be made via a 10Ω resistor which, along with the decoupling capacitors, will provide some filtering between V_D and V_S. In some systems, a direct connection can be made. Experimentation may be the best way to determine the appropriate connection between V_S and V_D.

GROUNDING

The analog and digital sections of the design should be carefully and cleanly partitioned. Each section should have its own ground plane with no overlap between them. AGND should be connected to the analog ground plane as well as all other analog grounds. DGND should be connected to the digital ground plane and all digital signals referenced to this plane. The ADS1250 pinout is such that the converter is cleanly separated into an analog and digital portion. This should allow simple layout of the analog and digital sections of the design. For a single converter system, AGND and DGND of the ADS1250 should be connected together, underneath the converter. Do not join the ground planes, but connect the two with a moderate signal trace. For multiple converters, connect the two ground planes at one location as central to all of the converters as possible. In some cases, experimentation may be required to find the best point to connect the two planes together. The printed circuit board can be designed to provide different analog/digital ground connections via short jumpers. The initial prototype can be used to establish which connection works best.

DECOUPLING

Good decoupling practices should be used for the ADS1250 and for all components in the design. All decoupling capacitors, but specifically the 0.1µF ceramic capacitors, should be placed as close as possible to the pin being decoupled. A 1µF to 10µF capacitor, in parallel with a 0.1µF ceramic capacitor, should be used to decouple V_S to AGND. At a minimum, a 0.1µF ceramic capacitor should be used to decouple V_D to DGND, as well as for the digital supply on each digital component.

TYPICAL CONNECTION

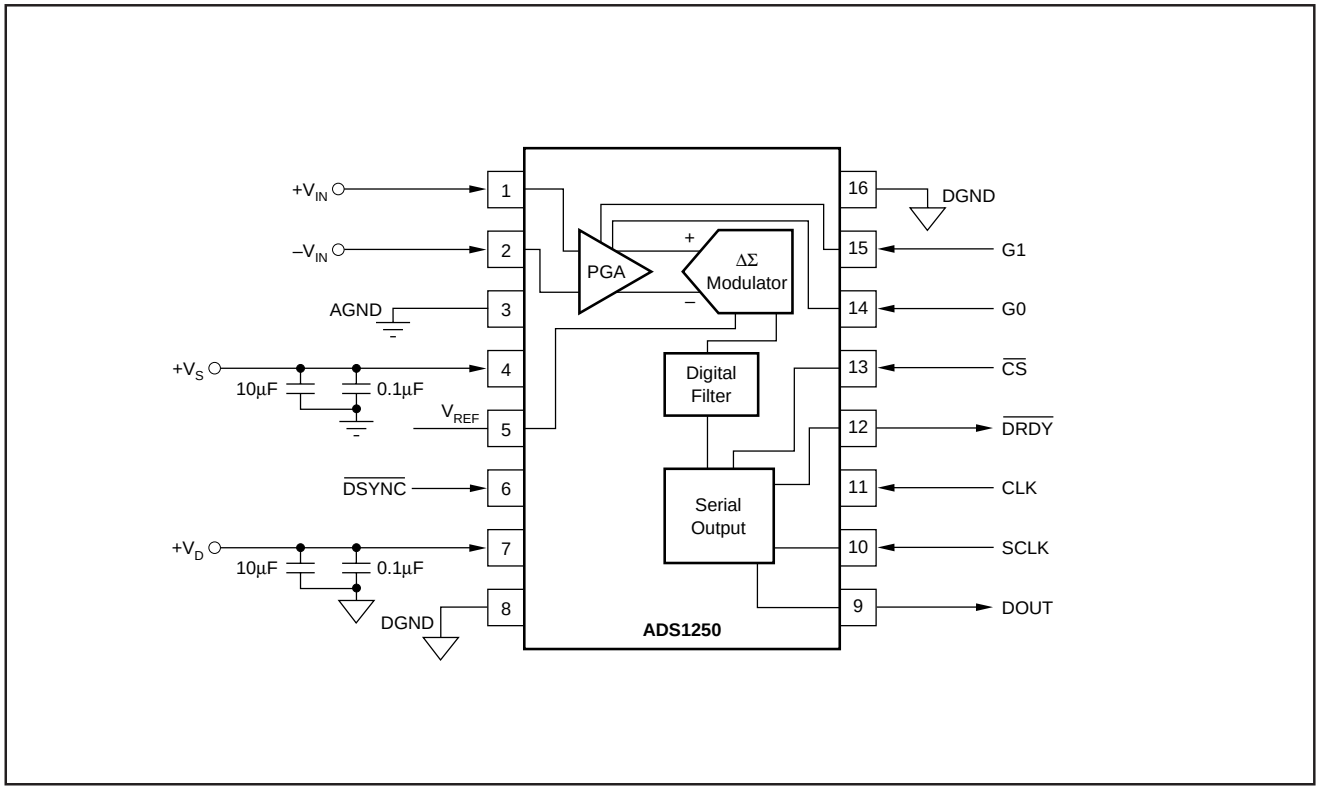


FIGURE 25. Connection Diagram.

SYSTEM CONSIDERATIONS

The recommendations for power supplies and grounding will change depending on the requirements and specific design of the overall system. Achieving 20 bits noise performance is a great deal more difficult than achieving 12 bits of noise performance. In general, a system can be broken up into four different stages:

- Analog Processing
- Analog Portion of the ADS1250
- Digital Portion of the ADS1250
- Digital Processing

For the simplest system consisting of minimal analog signal processing (basic filtering and gain), a microcontroller, and one clock source, high resolution can be achieved by powering all components by a common power supply. In addition, all components can share a common ground plane. Thus, there would be no distinctions between "analog" or "digital" power and ground. The layout should still include a power plane, a ground plane, and careful decoupling. In a more extreme case, the design could include: multiple ADS1250s; extensive analog signal processing; one or more microcontrollers, digital signal processors, or microprocessors; many different clock sources; and interconnections to various other systems. High resolution will be very difficult to achieve for this design. The approach would be to break the system into as many different parts as possible. For example, each ADS1250 may have its own "analog" processing front end, its own analog power and ground (possibly shared with the analog front end), and its own "digital" power and ground. The converter's "digital" power and ground would be separate from the power and ground for the system's processors, RAM, ROM, and "glue" logic.

DEFINITION OF TERMS

An attempt has been made to be consistent with the terminology used in this data sheet. In that regard, the definition of each term is given as follows:

Analog Input Differential Voltage—For an analog signal that is fully differential, the voltage range can be compared to that of an instrumentation amplifier. For example, if both analog inputs of the ADS1250 are at 2.048V, the differential voltage is 0V. If one input is at 0V and the other is at 4.096V, the differential voltage magnitude is 4.096V. This is the case regardless of which input is at 0V and which is at 4.096V. The analog input differential voltage is given by the following equation:

$$+V_{IN} - -V_{IN}$$

A positive digital output is produced whenever the analog input differential voltage is positive, while a negative digital output is produced whenever the differential is negative. For example, with a 4.096V reference and a gain setting of 2, a positive full-scale output is produced when the analog input differential is 2.048V. A negative full-scale output is produced when the differential voltage is –2.048V. In each case, the actual input voltages must remain within the AGND to V_S range (see Table I).

Actual Analog Input Voltage—The voltage at any one analog input relative to AGND.

Full-Scale Range (FSR)—As with most A/D converters, the full-scale range of the ADS1250 is defined as the "input" which produces the positive full-scale digital output minus the "input" which produces the negative full-scale digital output. For example, with a 4.096V reference and a gain setting of 2, the differential full-scale range is 2.048V – (–2.048V) = 4.096V.

Least Significant Bit (LSB) Weight—This is the theoretical amount of voltage that the differential voltage at the analog input would have to change in order to observe a change in the output data of one least significant bit. It is computed as follows:

$$\text{LSB Weight} = \frac{\text{Full–Scale Range}}{2^N}$$

where N is the number of bits in the digital output.

Conversion Cycle—The term conversion cycle, as used here, refers to the time period between $\overline{\text{DRDY}}$ pulses.