



**AFE1144**

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## HDSL/MDSL ANALOG FRONT END

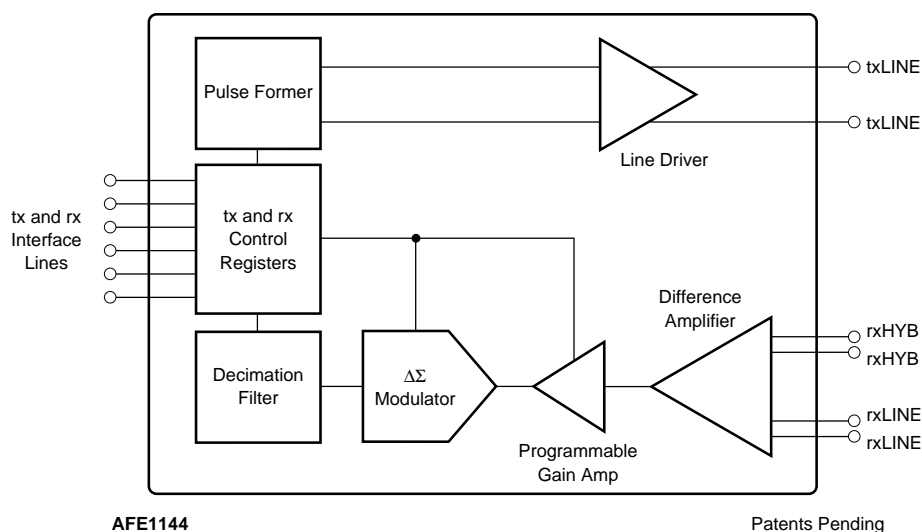
### FEATURES

- LOWER OUT OF BAND PSD
- SSOP-28
- PIN COMPATIBLE WITH AFE1124
- 64kbps TO 1168kbps OPERATION
- SCALABLE DATA RATE
- 250mW POWER DISSIPATION
- +5V POWER (5V or 3.3V Digital)

### DESCRIPTION

Burr-Brown's Analog Front End chip greatly reduces the size and cost of an xDSL (Digital Subscriber Line) system by providing all of the active analog circuitry needed to connect a digital signal processor to an external compromise hybrid and line transformer. The AFE1144 is optimized for HDSL (High bit rate DSL) and for lower speed MDSL (Medium speed DSL) and RADSL (Rate Adaptive DSL) applications. Because the transmit and receive filter responses automatically change with clock frequency, the AFE1144 is particularly suitable for RADSL and multiple rate DSL systems. The device operates over a wide range of data rates from 64kbps to 1168kbps.

Functionally, this unit consists of a transmit and a receive section. The transmit section generates analog signals from 2-bit digital symbol data and filters the analog signals to create 2B1Q symbols. The on board differential line driver provides a 13.5dBm signal to the telephone line. The receive section filters and digitizes the symbol data received on the telephone line. This IC operates on a single 5V supply. The digital circuitry in the unit can be connected to a supply from 3.3V to 5V. It is housed in a SSOP-28 package.



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Twx: 910-952-1111 • Internet: <http://www.burr-brown.com/> • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

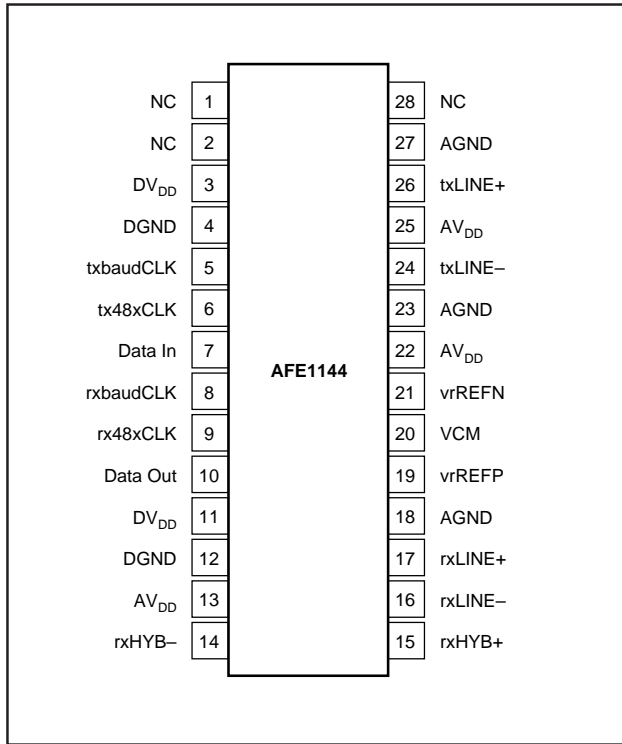
# SPECIFICATIONS

Specifications are at 25°C, AV<sub>DD</sub> = +5V, DV<sub>DD</sub> = +3.3V, f<sub>tx</sub> = 584kHz (E1 rate), unless otherwise noted.

PARAMETER	COMMENTS	AFE1144E			UNITS
		MIN	TYP	MAX	
<b>RECEIVE CHANNEL</b>					
Number of Inputs	Differential	2			
Input Voltage Range	Balanced Differential <sup>(1)</sup>		±3.0		V
Common-Mode Voltage			AV <sub>DD</sub> /2		V
Input Impedance All Inputs			See Typical Performance Curves		
Input Capacitance			10		pF
Input Gain Matching	Line Input vs Hybrid Input		±2		%
Resolution		14			Bits
Programmable Gain	0dB, 3dB, 6dB, 9dB and 12dB	0		+12	dB
Settling Time for Gain Change			6		Symbol Periods
Gain + Offset Error	Tested at Each Gain Range		5		%FSR <sup>(2)</sup>
Output Data Coding	Two's Complement				
Output Symbol Rate, rxSYNC <sup>(3)</sup>		32		584	kHz
Output Bit Rate, rxSYNC <sup>(3)</sup>		64		1168	kbits/sec
<b>TRANSMIT CHANNEL</b>					
Transmit Clock Rate, f <sub>tx</sub>	Symbol Rate	32		584	kHz
T1 Transmit -3dB Point	T1E1 4/99 - 002R4 Draft Compliant		196		kHz
T1 Rate Power <sup>(4, 5)</sup>	txBoost = 0	13		14	dBm
E1 Transmit -3dB Point	ETSI Compliant		292		kHz
E1 Transmit Power <sup>(4, 5)</sup>	txBoost = 0	13		14	dBm
Common-Mode Voltage, V <sub>CM</sub>			AV <sub>DD</sub> /2		V
Output Resistance <sup>(6)</sup>	DC to 1MHz		1		Ω
<b>TRANSCEIVER PERFORMANCE</b>					
Uncancelled Echo <sup>(5)</sup>	rxGAIN = 0dB, Loopback Enabled		-71	-68.5	dB
	rxGAIN = 0dB, Loopback Disabled		-71	-68.5	dB
	rxGAIN = 3dB, Loopback Disabled		-74	-71	dB
	rxGAIN = 6dB, Loopback Disabled		-76	-73.5	dB
	rxGAIN = 9dB, Loopback Disabled		-78	-75.5	dB
	rxGAIN = 12dB, Loopback Disabled		-80	-77.5	dB
<b>DIGITAL INTERFACE</b>					
Logic Levels					
V <sub>IH</sub>	I <sub>IH</sub>   < 10μA	DV <sub>DD</sub> -1		DV <sub>DD</sub> +0.3	V
V <sub>IL</sub>	I <sub>IL</sub>   < 10μA	-0.3		+0.8	V
V <sub>OH</sub>	I <sub>OH</sub> = -20μA	DV <sub>DD</sub> -0.5			V
V <sub>OL</sub>	I <sub>OL</sub> = 20μA			+0.4	V
t <sub>rx1</sub> Interface		9		14	ns
<b>POWER</b>					
Analog Power Supply Voltage	Specification		5		V
Analog Power Supply Voltage	Operating Range	4.75		5.25	V
Digital Power Supply Voltage	Specification		3.3		V
Digital Power Supply Voltage	Operating Range	3.15		5.25	V
Power Dissipation <sup>(4, 5)</sup>	AV <sub>DD</sub> = 5V, DV <sub>DD</sub> = 3.3V,		250		mW
Power Dissipation <sup>(4, 5)</sup>	AV <sub>DD</sub> = DV <sub>DD</sub> = 5V		300		mW
PSRR			55		dB
<b>TEMPERATURE RANGE</b>					
Operating <sup>(6)</sup>		-40		+85	°C

NOTES: (1) With a balanced differential signal, the positive input is 180° out of phase with the negative input, therefore the actual voltage swing about the common-mode voltage on each pin is ±1.5V to achieve a total input range of ±3.0V or 6Vp-p. (2) FSR is Full-Scale Range. (3) The output data is available at twice the symbol rate with interpolated values. (4) With a pseudorandom equiprobable sequence of HDSL pulses; 13.5dBm applied to the transformer (16.5dBm output from txLINEP and txLINEN). (5) See the Discussion of Specifications section of this data sheet for more information. (6) Functionality is guaranteed over temperature range.

## PIN CONFIGURATION



## ABSOLUTE MAXIMUM RATINGS

Analog Inputs: Current .....	±100mA, Momentary ±10mA, Continuous
Voltage .....	AGND -0.3V to AV <sub>DD</sub> +0.3V
Analog Outputs Short Circuit to Ground (+25°C) .....	Continuous
AV <sub>DD</sub> to AGND .....	-0.3V to 6V
DV <sub>DD</sub> to DGND .....	-0.3V to 6V
Digital Input Voltage to DGND .....	-0.3V to DV <sub>DD</sub> +0.3V
Digital Output Voltage to DGND .....	-0.3V to DV <sub>DD</sub> +0.3V
AGND, DGND, Differential Voltage .....	0.3V
Junction Temperature (T <sub>J</sub> ) .....	+150°C
Storage Temperature Range .....	-40°C to +125°C
Lead Temperature (soldering, 3s) .....	+260°C
Power Dissipation .....	700mW



## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER <sup>(1)</sup>	TRANSPORT MEDIA
AFE1144	SSOP-28	324	-40°C to +85°C	AFE1144E	AFE1144E	Rails
"	"	"	"	"	AFE1144E/1K	Tape and Reel

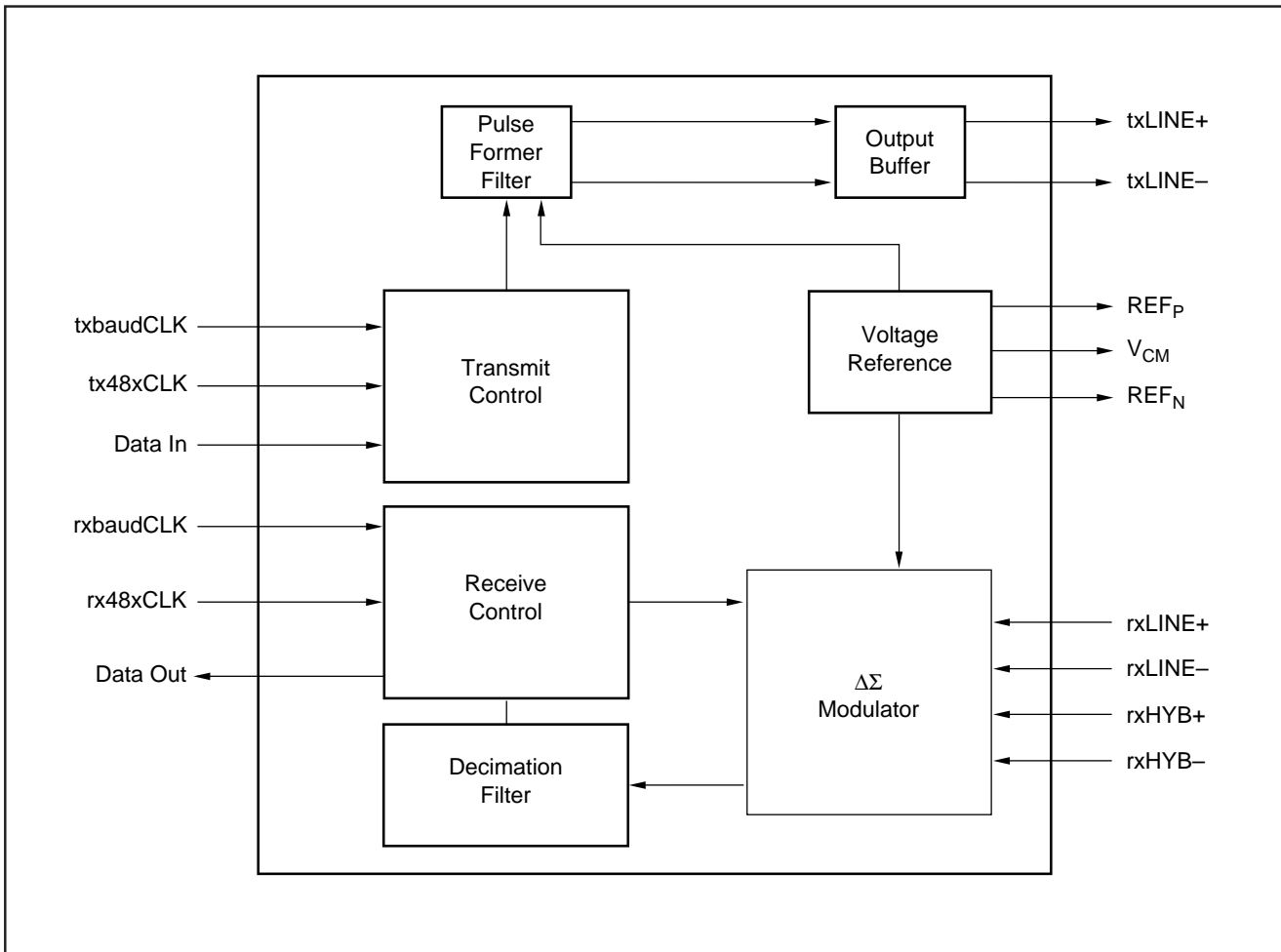
NOTE: (1) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /1K indicates 1000 devices per reel). Ordering 1000 pieces of "AFE1144E/1K" will get a single 1000-piece Tape and Reel.

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## PIN DESCRIPTIONS

PIN #	TYPE	NAME	DESCRIPTION
1	No Connection	NC	
2	No Connection	NC	
3	Power	DV <sub>DD</sub>	Digital Supply (+3.3 to +5V)
4	Ground	DGND	Digital Ground
5	Input	txbaudCLK	Transmit Baud Clock (584kHz for E1)
6	Input	tx48xCLK	Transmit Clock at 48x baud clock (28.032MHz for E1)
7	Input	Data In	Input Data Word
8	Input	rxbaudCLK	Receive baud clock (584kHz for E1)
9	Input	rx48xCLK	Receive clock at 48x baud clock (28.032MHz for E1)
10	Output	Data Out	Output Data Word
11	Power	DV <sub>DD</sub>	Digital Supply (+3.3 to +5V)
12	Ground	DGND	Digital Ground
13	Power	AV <sub>DD</sub>	Analog Supply (+5V)
14	Input	rxHYB-	Negative input from hybrid network
15	Input	rxHYB+	Positive input from hybrid network
16	Input	rxLINE-	Negative line input
17	Input	rxLINE+	Positive line input
18	Ground	AGND	Analog Ground
19	Output	vrREFP	Positive reference output
20	Output	VCM	Common-mode voltage (buffered)
21	Output	vrREFN	Negative reference output
22	Power	AVDD	Analog Supply (+5V)
23	Ground	AGND	Analog Ground
24	Output	txLINE-	Negative line output
25	Power	AV <sub>DD</sub>	Output buffer supply (+5V)
26	Output	txLINE+	Positive line output
27	Ground	AGND	Output buffer ground
28	No Connection	NC	

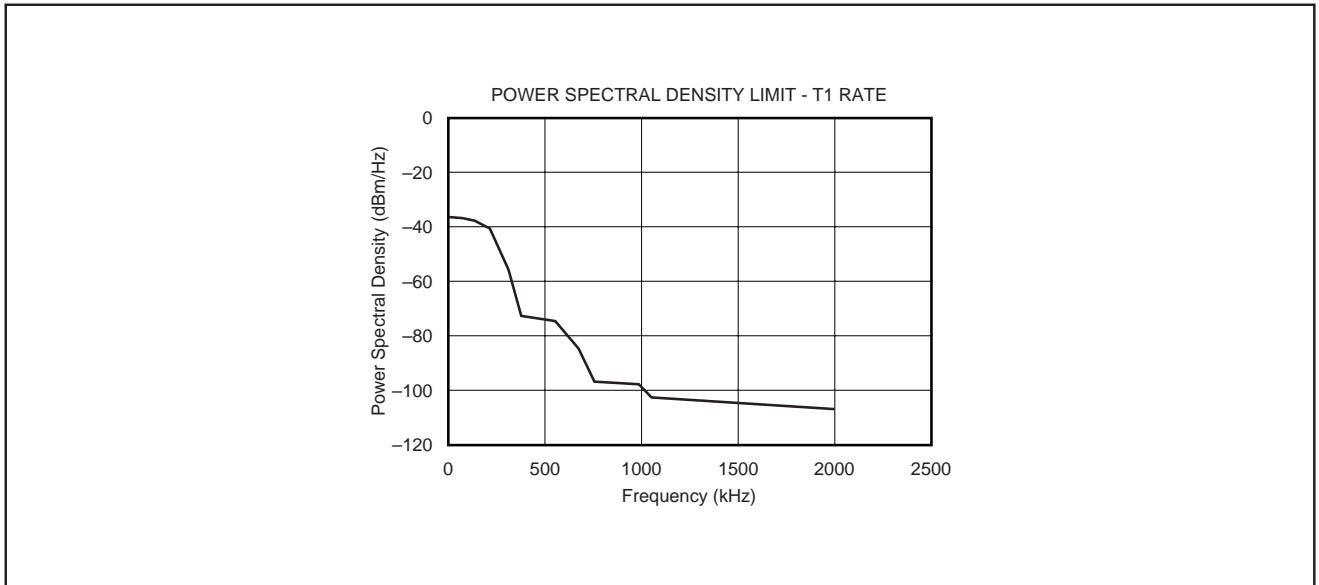
## BLOCK DIAGRAM



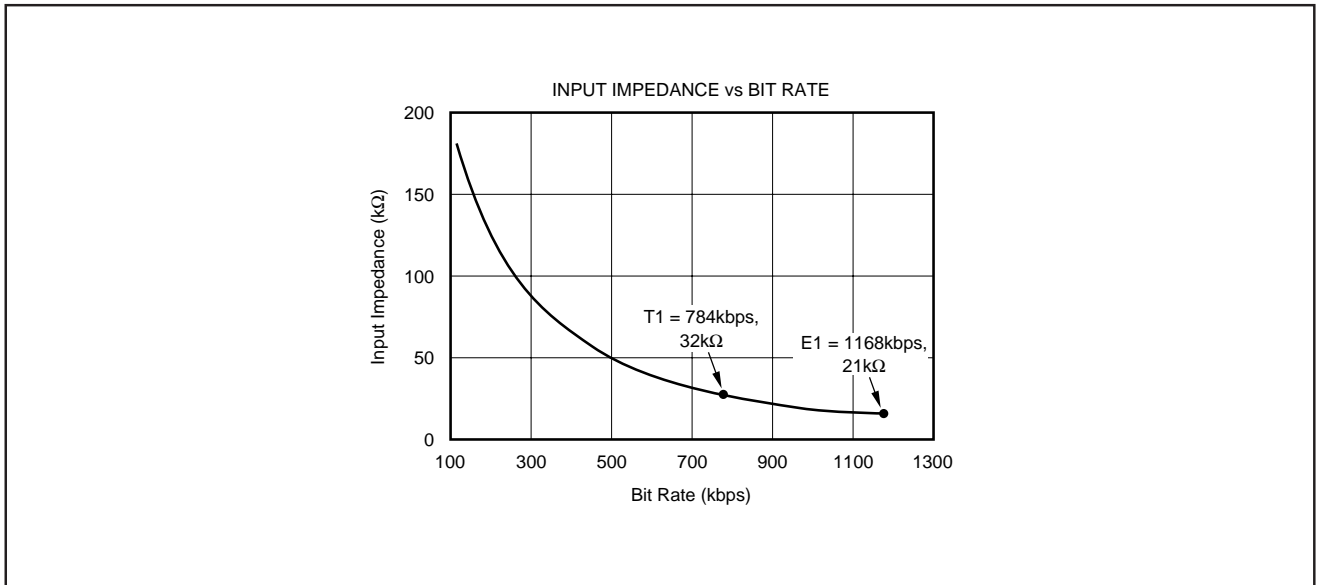
# TYPICAL PERFORMANCE CURVES

## At Output of HDSL Pulse Transformer

The curves shown below are measured at the line output of the HDSL transformer. Typical at 25°C, AV<sub>DD</sub>+ = +5V, DV<sub>DD</sub>+ = +3.3V, f<sub>TX</sub> = 1168kHz, unless otherwise specified.



CURVE 1. Upper Bound of Power Spectral Density Measured at Output of HDSL Transformer.



CURVE 2. Input Impedance of rxLINE and rxHYB.

# THEORY OF OPERATION

The AFE1144 consists of a transmit and a receive channel. It interfaces to the HDSL DSP through a six wire serial interface, three wires for the transmit channel and three wires for the receive channel. It interfaces to the HDSL telephone line transformer and external compromise hybrid through transmit and receive analog connections.

The transmit channel consists of a switched-capacitor pulse forming network followed by a differential line driver. The pulse forming network receives 2-bit digital symbol data and generates a filtered 2B1Q analog output waveform. The differential line driver uses a composite output stage combining class B operation (for high efficiency driving large signals) with class AB operation (to minimize crossover distortion).

The receive channel is designed around a fourth-order delta sigma A/D converter. It includes a difference amplifier designed to be used with an external compromise hybrid for first order analog echo cancellation. A programmable gain amplifier with gains of 0dB to +12dB is also included. The delta sigma modulator operating at a 24X oversampling ratio produces a 14-bit output at rates up to 584kHz (1.168Mbps).

The receive channel operates by summing the two differential inputs, one from the line (rxLINE) and the other from the

compromise hybrid (rxHYB). The connection of these two inputs so that the hybrid signal is subtracted from the line signal is described in the paragraph titled "Echo Cancellation in the AFE". The equivalent gain for each input in the difference amp is one. The resulting signal then passes to a programmable gain amplifier which can be set for gains of 0dB through +12dB. Following the PGA, the ADC converts the signal to a 14-bit digital word.

The serial interface consists of three wires for transmit and three wires for receive. The three wire transmit interface is transmit baud rate clock, transmit 48x oversampling clock and Data Out. The three wire receive interface is receive baud rate clock, receive 48x oversampling clock and Data In. The transmit and receive clocks are supplied to the AFE1144 from the DSP and are completely independent.

## DIGITAL DATA INTERFACE

Data is received by the AFE1144 from the DSP on the Data In line. Data is transmitted from the AFE1144 to the DSP on the Data Out line. The paragraphs below describe the timing of these signals and data structure.

Data is transmitted and received in synchronization with the 48x transmit and receive clocks (tx48xCLK and rx48xCLK). There are 48-bit times in each baud period. Data In is

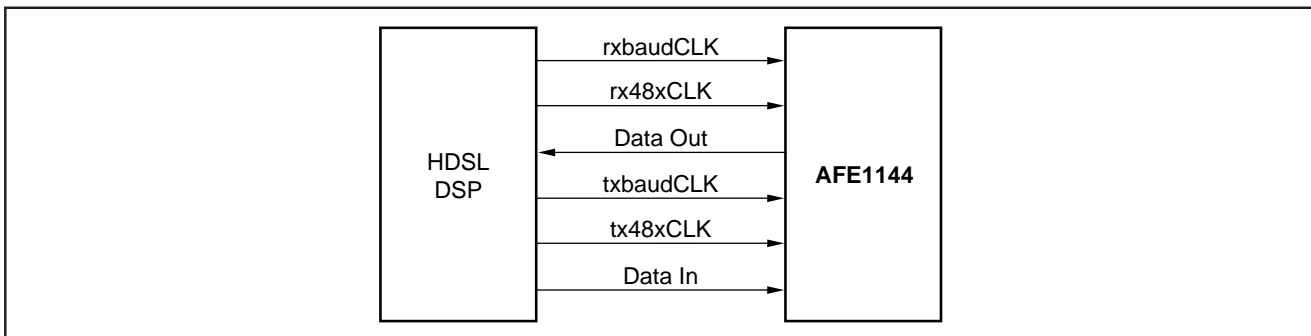


FIGURE 1. DSP Interface.

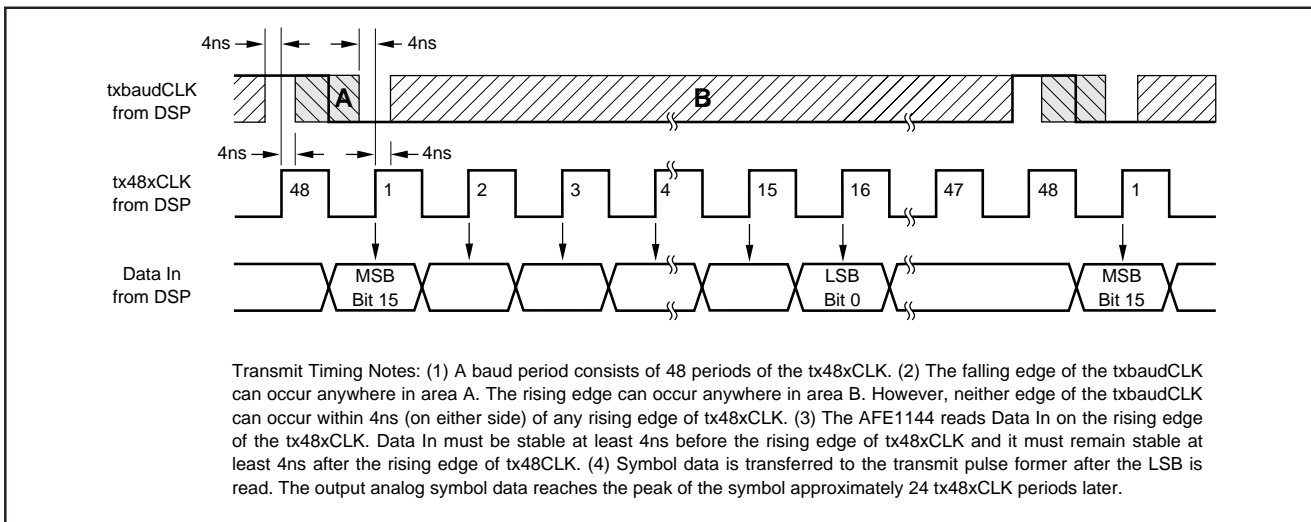


FIGURE 2. Transmit Timing Diagram.

received in the first 16 bits of each baud period. The remaining 32-bit periods are not used for Data In. Data Out is transmitted during the first 16 bits of the baud period. A second interpolated value is transmitted in subsequent bits of the baud period.

**txbaudCLK:** The transmit data baud rate, generated by the DSP. It is 392kHz for T1 or 584kHz for E1. It may vary from 32kHz (64kbps) to 584kHz (1.168Mbps).

**tx48xCLK:** The transmit pulse former oversampling sampling clock, generated by the DSP. It is 48x the transmit symbol rate or 28.032MHz for 584kHz symbol rate. This clock should run continuously.

**Data In:** This is a 16-bit output data word sent from the DSP to the AFE. The sixteen bits include tx symbol information and other control bits, as described below. The data should be clocked out of the DSP on the falling edge and it should

be valid on the rising edge of the tx48xCLK. The AFE1144 reads Data In on the rising edge of the tx48xCLK. The bits are defined in Table I. Data In is read by the AFE1144 during the first 16 bits periods of each baud period. Only the first 8 bits are used in the AFE1144. The second 8 bits are reserved for use in the future products. The remaining 32 bits periods of the baud period are not used for Data In.

Data In Bits:

**tx enable signal**—This bit controls the tx Symbol definition bits. If this bit is 0, only a 0 symbol is transmitted regardless of the state of the tx Symbol definition bits. If this bit is 1, the tx Symbol definition bits determine the output symbol.

**tx Symbol Definition**—These two bits determine the output 2B1Q symbol transmitted.

**Rx Gain Settings**—These bits set the gain of the receive channel programmable gain amplifier.

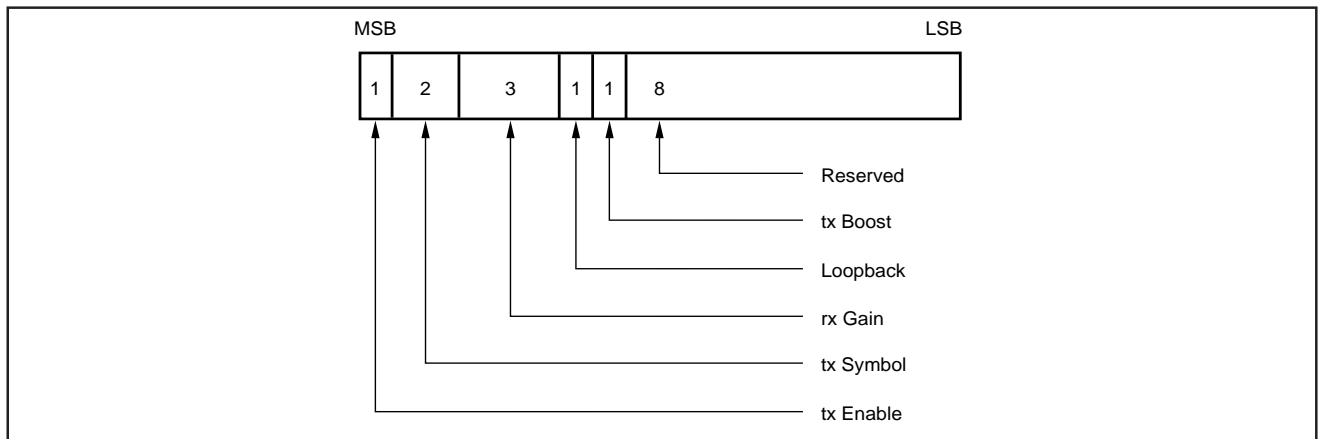


FIGURE 3. Data In Word.

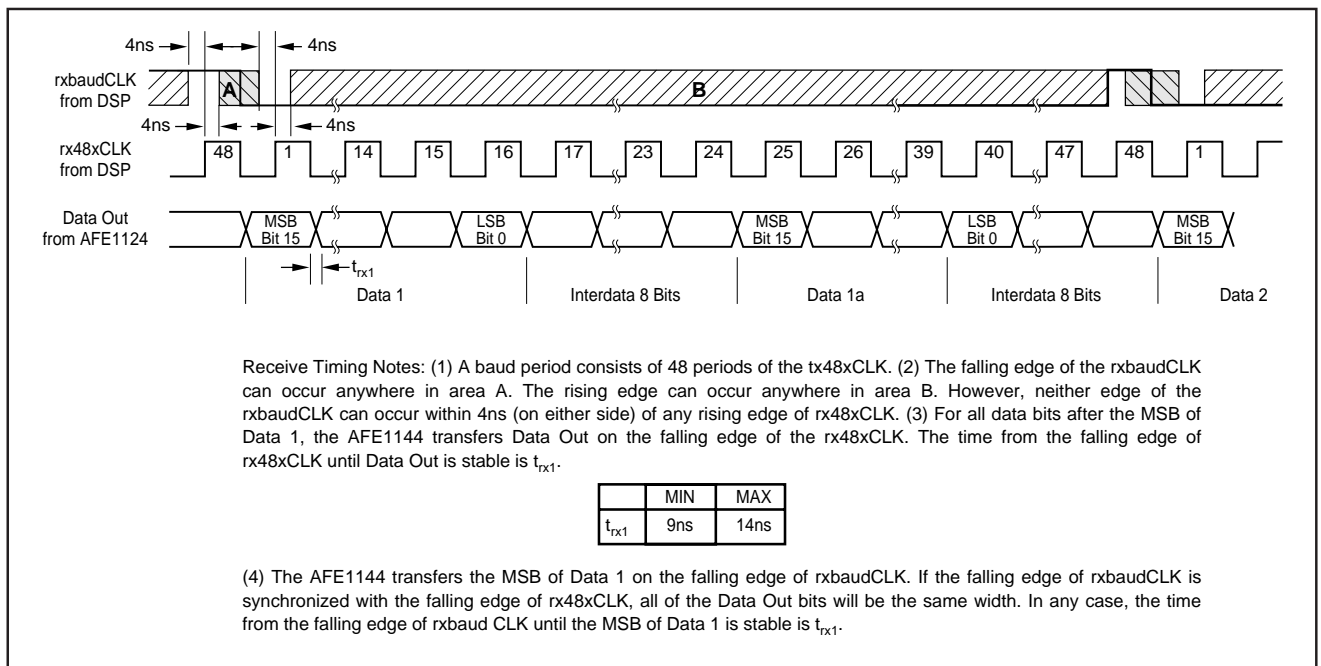


FIGURE 4. Receive Timing Diagram.

**Loopback Control**—This bit controls the operation of loopback. When enabled (logic 1), the rxLINE+ and rxline– inputs are disconnected from the AFE. The rxHYB+ and rxHYB– inputs remain connected. When disabled, the rxLINE+ and rxLINE– inputs are connected.

**txBoost**—This bit controls the addition of 0.5dB additional power to the output line driver.

BIT	DESCRIPTION	BIT STATE	OUTPUT STATE
15 (MSB)	tx Enable Signal	0	AFE Transmits a 0 Symbol
		1	AFE Transmits HDSL Symbol as defined by bits 14 and 13
14 and 13	tx Symbol Definition	00	–3 Transmit Symbol
		01	–1 Transmit Symbol
		11	+1 Transmit Symbol
		10	+3 Transmit Symbol
12 - 10	rx Gain Settings	000	rx gain in AFE 0dB
		001	rx gain in AFE 3dB
		010	rx gain in AFE 6dB
		011	rx gain in AFE 9dB
		100	rx gain in AFE 12dB
		101	rx gain in AFE Reserved
		110	rx gain in AFE Reserved
		111	rx gain in AFE Reserved
9	Loopback Control	1	Loopback Mode
		0	Normal Operation
8	tx Boost	0	Normal Transmit Power
		1	+0.5dB Transmit Power Boost
7 - 0	SPARE		NA

TABLE I. Data In.

**rxbaudCLK:** This is the receive data baud rate (symbol clock), generated by the DSP. It is 392kHz for T1 or 584kHz for E1. It can vary from 32kHz (64kbps) to 584kHz (1.168Mbps).

**rx48xCLK:** This is the A/D converter over-sampling clock, generated by the DSP. It is 48x the receive symbol rate or 28.032MHz for 584kHz symbol rate. This clock should run continuously.

**Data Out:** This is the 14-bit A/D converter output data (+2 spare bits) sent from the AFE to the DSP. The 14 bits from the A/D Converter will be the upper bits of the 16-bit word (bits 15-2). The spare bits (1 and 0) will be always be low. Eight additional (interdata) bits follow which are always high. The data is clocked out on the falling edge of rx48xCLK. The bandwidth of the A/D converter decimation filter is equal to one half of the symbol rate. The nominal output rate of the A/D converter is one conversion per symbol period. For more flexible post processing, there is a second interpolated A/D conversion available in each symbol period. In Figure 4, the first conversion is shown as Data 1 and the second conversion is shown as Data 1a. It is suggested that rxbaudCLK is used with the rx48xCLK to read Data 1 while Data 1a is ignored. However, either or both outputs may be used for more flexible post-processing.

DATA OUT PER SYMBOL PERIOD

DATA	BITS
Data 1	16
Interdata Bits	8
Data 1a	16
Interdata bits	8
Total Bits/Symbol Period	48

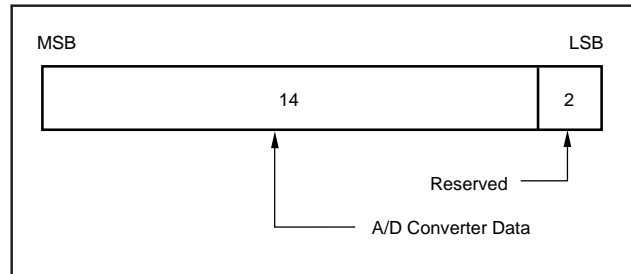


FIGURE 5. Data Out Word.

### ANALOG-TO-DIGITAL CONVERTER DATA

The A/D converter data from the receive channel is coded in twos complement.

ANALOG INPUT	A/D CONVERTER DATA	
	MSB	LSB
Positive Full Scale	01111111111111	
Mid Scale	00000000000000	
Negative Full Scale	10000000000000	

### ECHO CANCELLATION IN THE AFE

The rxHYB input is subtracted from the rxLINE input for first order echo cancellation. For correct operation, be certain that the rxLINE input is connected to the same polarity signal at the transformer (+ to + and – to –) while the rxHYB input is connected to opposite polarity through the compromise hybrid (– to + and + to –) as shown in the Basic Connection Diagram.

### SCALABLE TIMING

The AFE1144 scales operation with the clock frequency. All internal filters and the pulse former change frequency with the clock speed so that the unit can be used at different frequencies just by changing the clock speed.

For the receive channel, the digital filtering of the delta sigma converter scales directly with the clock speed. The bandwidth of the converter’s decimation filter is always one-half of the symbol rate. The only receive channel issue in changing baud rate is the passive single pole anti-alias filter (see the following section). For systems implementing a broad range of speeds, selectable cutoff frequencies for the passive anti-alias filter should be used.



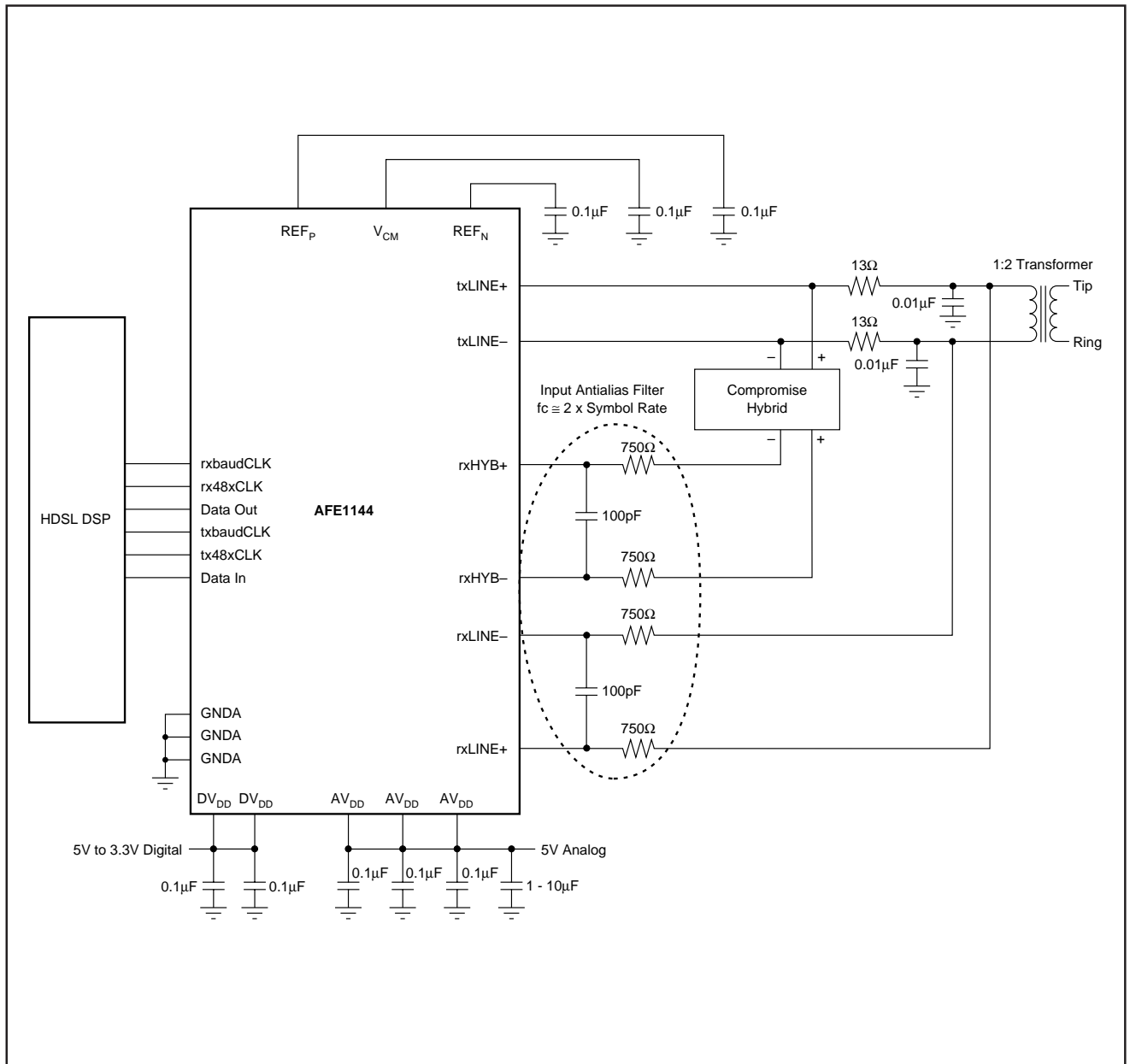


FIGURE 6. Basic Connection Diagram.

For the transmit channel, the pulse shape and the power spectral density scale directly with the clock rate. The power spectral density shown in Curve 1 and the pulse template shown in Curve 2 are measured at the output of the transformer. The transformer and the RC circuit on the output provide some smoothing for the output transmission. At lower bit rates, the amount of smoothing will be less.

### RXHYB AND RXLINE INPUT ANTI-ALIASING FILTERS

An external input anti-aliasing filter is needed on the hybrid and line inputs as shown in the Basic Connection Diagram above. The  $-3\text{dB}$  frequency of the input anti-aliasing filter

for the rxLINE and rxHYB differential inputs should be approximately  $1\text{MHz}$  for T1 and E1 symbol rates. Suggested values for the filter are  $750\Omega$  for each of the two input resistors and  $100\text{pF}$  for the capacitor. Together the two  $750\Omega$  resistors and the  $100\text{pF}$  capacitor result in a  $3\text{dB}$  frequency of just over  $1\text{MHz}$ . The  $750\Omega$  input resistors will result in minimal voltage divider loss with the input impedance of the AFE1144.

The antialiasing filters will give best performance with  $3\text{dB}$  frequency approximately equal to the bit rate. For instance, a  $3\text{dB}$  frequency of  $320\text{kHz}$  may be used for a single line bit rate of  $320\text{k}$  bits per second.

# DISCUSSION OF SPECIFICATIONS

## UNCANCELLED ECHO

A key measure of transceiver performance is uncancelled echo. Uncancelled echo is the summation of all of the errors in the transmit and receive paths of the AFE1144. It includes effects of linearity, distortion and noise. Uncancelled echo is tested in production by Burr-Brown with a circuit that is similar to the one shown in Figure 7, Uncancelled Echo Test Diagram.

The measurement of uncancelled echo is made as follows.

The AFE is connected to an output circuit including a typical 1:2 line transformer. The line is simulated by a 135Ω resistor. Symbol sequences are generated by the tester and applied both to the AFE and to the input of an adaptive filter. The output of the adaptive filter is subtracted from the AFE output to form the uncanceled echo signal. Once the filter taps have converged, the RMS value of the uncancelled echo is calculated. Since there is no far-end signal source or additive line noise, the uncanceled echo contains only noise and linearity errors generated in the transmit and receive sections of the AFE1144.

The data sheet value for uncancelled echo is the ratio of the RMS uncanceled echo (referred to the receiver input through the receiver gain) to the nominal transmitted signal (13.5dBm into 135Ω, or 1.74Vrms). This echo value is measured under a variety of conditions: with loopback enabled (line input disconnected); with loopback disabled under all receiver gain ranges; and with the line shorted ( $S_1$  closed in Figure 7).

## POWER DISSIPATION

Approximately 80% of the power dissipation in the AFE1144 is in the analog circuitry, and this component does not change with clock frequency. However, the power dissipation in the digital circuitry does decrease with lower clock frequency. In addition, the power dissipation in the digital section is decreased when operating from a smaller supply voltage, such as 3.3V. (The analog supply,  $AV_{DD}$ , must remain in the range 4.75V to 5.25V).

The power dissipation listed in the specifications section applies under these normal operating conditions: 5V Analog Power Supply; 3.3V Digital Power Supply; standard 13.5dBm delivered to the line; and a pseudorandom equiprobable sequence of HDSL output pulses. The power dissipation specifications includes all power dissipated in the AFE1144, it does not include power dissipated in the external load. The external power is 16.5dBm: 13.5dBm to the line and 13.5dBm to the impedance matching resistors. The external load power of 16.5dBm is 45mW. The typical power dissipation in the AFE1144 under various conditions is shown in Table II.

The T1 and E1 power measurements in the Specifications are made with the output circuit shown in Figure 7. This

BIT RATE PER AFE1144 (Symbols/sec)	DVDD (V)	TYPICAL POWER DISSIPATION IN THE AFE1144 (mW)
584 (E1)	3.3	250
584 (E1)	5	300
392 (T1)	3.3	240
392 (T1)	5	270
146 (E1/4)	3.3	230
146 (E1/4)	5	245

TABLE II. Typical Power Dissipation.

circuit uses a 1:2 transformer. The power measurements shown in Table II use an equivalent resistive load instead of the transformer to eliminate frequency dependent impedances of the transformer.

## LAYOUT

The analog front end of an HDSL system has two conflicting requirements. It must accept and deliver moderately high rate digital signals and it must generate, drive, and convert precision analog signals. To achieve optimal system performance with the AFE1144, both the digital and the analog sections must be treated carefully in board layout design.

The power supply for the digital section of the AFE1144 can range from 3.3V to 5V. This supply should be decoupled to digital ground with ceramic 0.1μF capacitors placed as close to DGND and  $DV_{DD}$  as possible. One capacitor should be placed between pins 3 and 4 and the second capacitor between pins 11 and 12. Ideally, both a digital power supply plane and a digital ground plane should run up to and underneath the digital pins of the AFE1144 (pins 5 through 10). However,  $DV_{DD}$  may be supplied by a wide printed circuit board (PCB) trace. A digital ground plane underneath all digital pins is strongly recommended.

The remaining portion of the AFE1144 should be considered analog. All AGND pins should be connected directly to a common analog ground plane and all  $AV_{DD}$  pins should be connected to an analog 5V power plane. Both of these planes should have a low impedance path to the power supply. The analog power supply pins should be decoupled to analog ground with ceramic 0.1μF capacitors placed as close to the AFE1144 as possible. One 10μF tantalum capacitor should also be used with each AFE1144 between the analog supply and analog ground.

Ideally, all ground planes and traces and all power planes and traces should return to the power supply connector before being connected together (if necessary). Each ground and power pair should be routed over each other, should not overlap any portion of another pair, and the pairs should be separated by a distance of at least 0.25 inch (6mm). One exception is that the digital and analog ground planes should be connected together underneath the AFE1144 by a small trace.

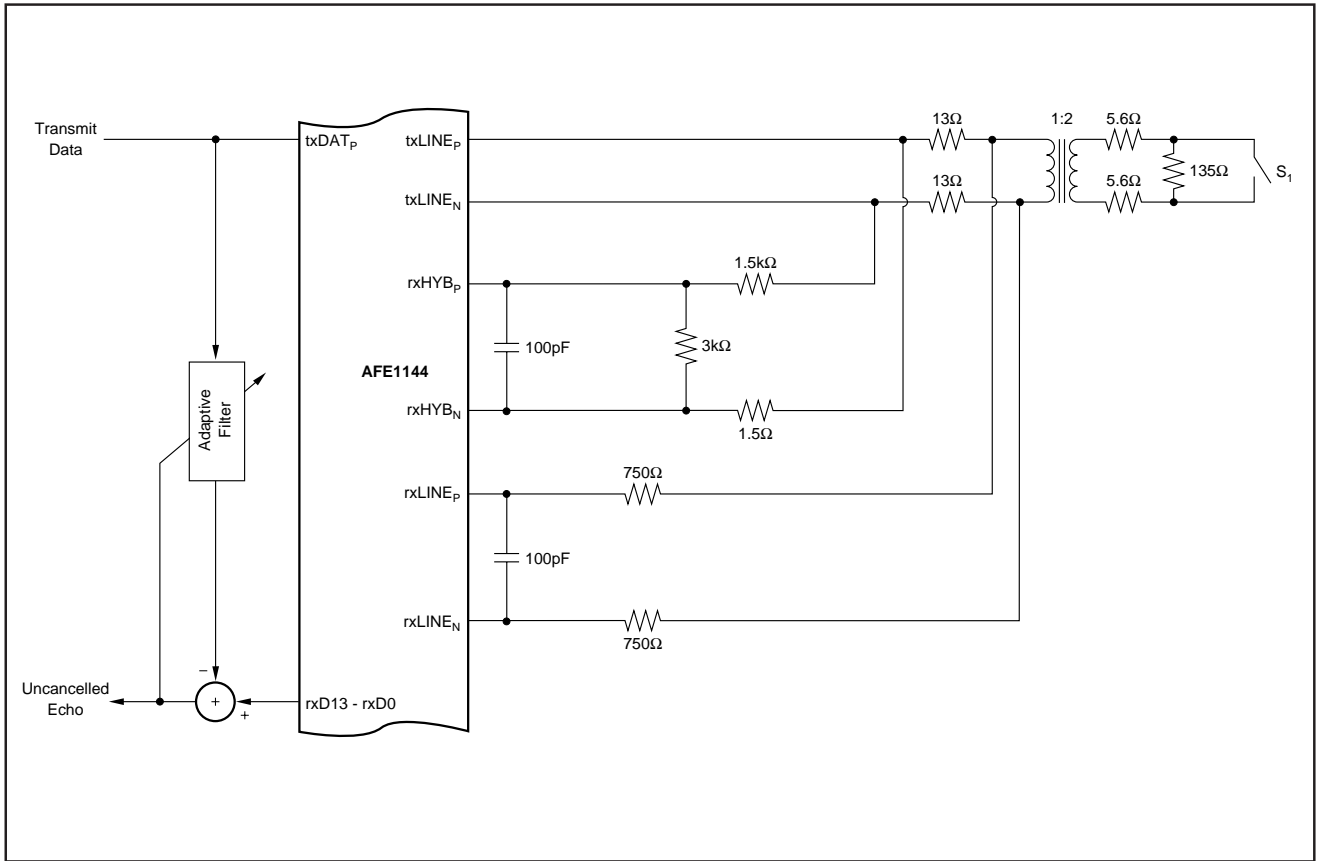


FIGURE 7. Uncancelled Echo Test Diagram.