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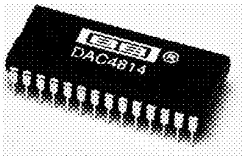


DAC4814

Quad 12-Bit Digital-to-Analog Converter (Serial Interface)

FEATURES

- COMPLETE QUAD DAC — INCLUDES INTERNAL REFERENCES AND OUTPUT AMPLIFIERS
- GUARANTEED SPECIFICATIONS OVER TEMPERATURE
- GUARANTEED MONOTONIC OVER TEMPERATURE
- HIGH-SPEED SERIAL INTERFACE (10MHz CLOCK)
- LOW POWER: 600mW (150mW/DAC)
- LOW GAIN DRIFT: 5ppm/°C
- LOW NONLINEARITY: ±1/2 LSB max
- UNIPOLAR OR BIPOLAR OUTPUT
- CLEAR/RESET TO UNIPOLAR OR BIPOLAR ZERO

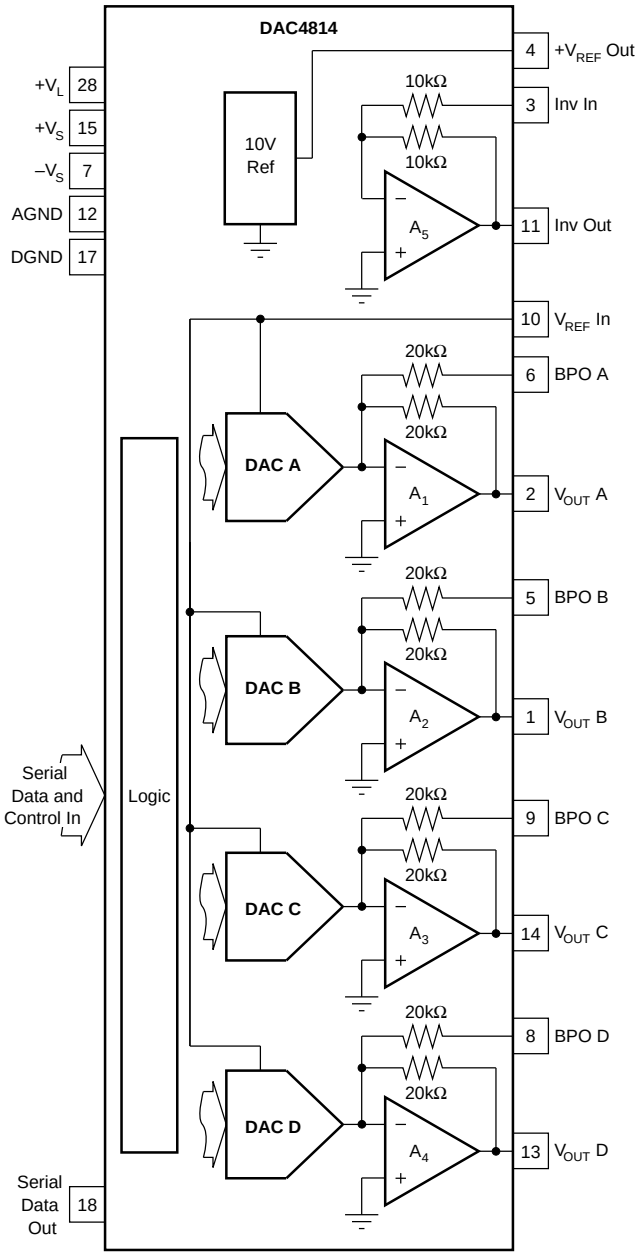
DESCRIPTION

The DAC4814 is one in a family of dual and quad 12-bit digital-to-analog converters. Serial, 8-bit, 12-bit interfaces are available.

The DAC4814 is complete. It contains CMOS logic, switches, a high-performance buried-zener reference, and low-noise bipolar output amplifiers. No external components are required for either unipolar 0 to 10V, 0 to –10V, or bipolar ±10V output ranges.

The DAC4814 has a high-speed serial interface capable of being clocked at 10MHz. Serial data are clocked DAC D MSB first into a 48-bit shift register, then strobed into each DAC separately or simultaneously as required. The DAC has an asynchronous clear control for reset to unipolar or bipolar zero depending on the mode selected. This feature is useful for power-on reset or system calibration. The DAC4814 is packaged in a 28-pin plastic DIP rated for the –40°C to +85°C extended industrial temperature range.

High-stability laser-trimmed thin film resistors assure high reliability and true 12-bit integral and differential linearity over the full specified temperature range.



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Printed in U.S.A. April, 1995

SPECIFICATIONS, Guaranteed over T_A = –40°C to +85°C unless otherwise specified.

ELECTRICAL

Specifications as shown for V_S = ±12V or ±15V, V_L = +5V, and R_L = 2kΩ unless otherwise noted.

PARAMETER	CONDITIONS	DAC4814AP			DAC4814BP			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
DIGITAL INPUTS								
Resolution		12			*			Bits
V_{IH} (Input High Voltage)		+2		+5	*		*	V
V_{IL} (Input Low Voltage)		0		+0.8	*		*	V
I_{IN} (Input Current)	T_A = 25°C			±1			*	µA
	T_A = –40°C to +85°C			±10			*	µA
C_{IN} (Input Capacitance)			0.8			*		pF
DIGITAL OUTPUT								
Data Out V_{OL}	I_{SINK} = 1.6mA	0		+0.4	*		*	V
V_{OH}	I_{SOURCE} = 500µA	+2.4		+5	*		*	V
ACCURACY								
Integral, Relative Linearity[1]				±1			±1/2	LSB
Differential Nonlinearity[2]	T_A = 25°C			±1			*	LSB
	T_A = –40°C to +85°C		+1.5/–1				±1	LSB
Unipolar Offset Error	T_A = +25°C			±1			±0.5	mV
	T_A = –40°C to +85°C			±3			*	mV
Bipolar Zero Error				±20			±10	mV
Gain Error Unipolar, Bipolar	With Internal or External 10.0V Ref			±0.2			±0.15	%
Power Supply Sensitivity[3]	V_S = ±11.4V to ±18V			30			*	ppmFSR/V
	V_L = +4.5V to +5.5V							
TEMPERATURE DRIFT								
Gain Drift Unipolar, Bipolar			±5	±30		*	±20	ppm/°C
Unipolar Offset Drift			±0.1	±5		*	*	ppmFSR/°C
Bipolar Zero Drift			±5	±15		*	±8	ppmFSR/°C
REFERENCE OUTPUT								
Output Voltage		+9.980	+10	+10.020	+9.985	*	+10.015	V
Reference Drift			±2	±30		*	±20	ppm/°C
Output Current	T_A = 25°C	+10/–5			*			mA
	T_A = –40°C to +85°C	+6.5/–5			*			mA
Max Load Capacitance (For Stability)			500			*		pF
Short Circuit Current			±20			*		mA
Load Regulation				40			*	ppm/mA
(ΔV_{OUT} vs ΔI_{LOAD})								
Supply Regulation				±5			*	ppm/V
(ΔV_{OUT} vs ΔV_S)								
INVERTER								
–10V Reference[4], Inverter Output		–10.020	–10	–9.980	–10.015	*	–9.985	V
–10V Reference Drift				±30			±20	ppm/°C
DC Output Impedance			0.1			*		Ω
Output Current		±7			*			mA
Max Load Capacitance (For Stability)			200			*		pF
Short Circuit Current			±30			*		mA
REFERENCE INPUT								
Reference Input Resistance		1.75	2.5		*	*		kΩ
Inverter Input Resistance		7	10		*	*		kΩ
BPO Input Resistance		14	20		*	*		kΩ
Reference Input Range				±10			*	V
ANALOG SIGNAL OUTPUTS								
Voltage Range		$–V_S$ + 1.4		$+V_S$ – 1.4	*		*	V
DC Output Impedance			0.1			*		Ω
Output Current		±5			*			mA
Max Load Capacitance (For Stability)	V_{OUT}		500			*		pF
Short Circuit Current			±30			*		mA
DYNAMIC PERFORMANCE[5]	C_L = 100pF							
Unipolar Mode Settling Time	To 1/2 LSB of Full Scale		2.5	10		*	*	µs
Bipolar Mode Settling Time	To 1/2 LSB of Full Scale		3.5	10		*	*	µs
Slew Rate			10			*		V/µs
Small-Signal Bandwidth			3			*		MHz
ANALOG GROUND CURRENT								
(Code Dependent)			±4			*		mA
DIGITAL CROSSTALK	Full Scale Transition		3			*		nV-s
	C_L= 100pF							
D/A GLITCH IMPULSE			30			*		nV-s

SPECIFICATIONS (CONT), Guaranteed over T_A = –40°C to +85°C unless otherwise specified.

ELECTRICAL

Specifications as shown for V_S = ±12V or ±15V, V_L = +5V, and R_L = 2kΩ unless otherwise noted.

PARAMETER	CONDITIONS	DAC4814AP			DAC4814BP			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY								
$+V_S$ and $-V_S$		±11.4	±15	±18	*	*	*	V
$+V_L$		4.5	5	5.5	*	*	*	V
$+I_S$			+20	+24		*	*	mA
$-I_S$			–20	–25.5		*	*	mA
$+I_L$	Digital Inputs = 0V or $+V_L$		0.4	2		*	*	mA
$+I_L$	Digital Inputs = V_{IL} or V_{IH}			10			*	mA
Total Power, All DACs			600	753		*	*	mW
TEMPERATURE RANGE								
Specified		–40		+85	*		*	°C
Operating		–40		+85	*		*	°C
Thermal Resistance, θ_{JA}			75			*		°C/W

NOTES: (1) End point linearity. (2) Guaranteed monotonic. (3) Change in bipolar full scale output. Includes voltage output DAC, voltage reference, and reference inverter. (4) Inverter output with inverter input connected to $+V_{REF}$. (5) Guaranteed to but not tested.

ABSOLUTE MAXIMUM RATINGS

$+V_L$ to AGND	0V, +7V
$+V_L$ to DGND	0V, +7V
$+V_S$ to AGND	0V, +18V
$-V_S$ to AGND	0V,–18V
AGND to DGND	±0.3V
Any digital input to DGND	–0.3V, $+V_L$ +0.3V
Ref In to AGND	±25V
Ref In to DGND	±25V
Storage Temperature Range	–55°C to +125°C
Operating Temperature Range	–40°C to +85°C
Lead Temperature (soldering, 10s)	+300°C
Junction Temperature	+155°C
Output Short Circuit	Continuous to common or $\pm V_S$
Reference Short Circuit	Continuous to common or $+V_S$

ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

PACKAGE INFORMATION

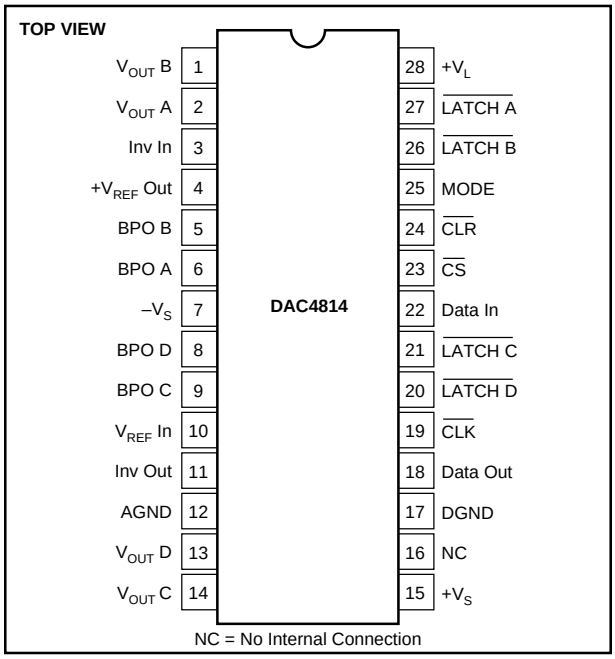
MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
DAC4814AP	28-Pin Plastic DBL Wide DIP	215
DAC4814BP	28-Pin Plastic DBL Wide DIP	215

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

PIN DESIGNATIONS

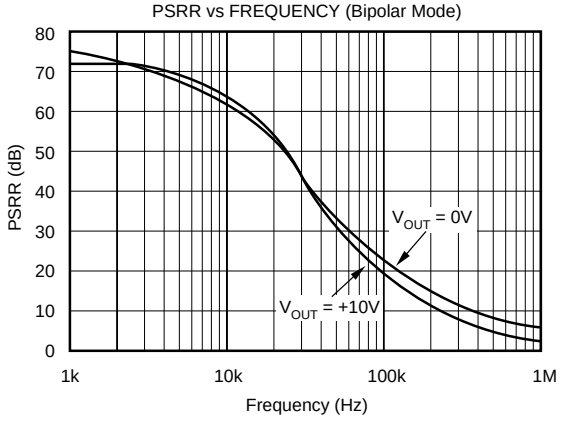
PIN	DESCRIPTOR	FUNCTION	PIN	DESCRIPTOR	FUNCTION
1	V_{OUT} B	Analog output voltage, DAC B	28	$+V_L$	Positive logic power supply, +5V input
2	V_{OUT} A	Analog output voltage, DAC A	27	$\overline{\text{LATCH A}}$	Latch data update, logic input, DAC A
3	Inv In	Inverter (A_5) input	26	$\overline{\text{LATCH B}}$	Latch data update, logic input, DAC B
4	$+V_{REF}$ Out	Positive reference voltage output (+10V output)	25	MODE	Selection input for unipolar or bipolar reset to zero
5	BPO B	Biplolar offset input, DAC B	24	$\overline{\text{CLR}}$	Asynchronous input reset to zero
6	BPO A	Bipolar offset input, DAC A	23	$\overline{\text{CS}}$	Chip select enable, DAC A, B, C, and D
7	$-V_S$	Negative analog power supply , –15V input	22	Data In	Serial data input
8	BPO D	Bipolar offset input, DAC D	21	$\overline{\text{LATCH C}}$	Latch data update, logic input, DAC C
9	BPO C	Bipolar offset input, DAC C	20	$\overline{\text{LATCH D}}$	Latch data update, logic input, DAC D
10	V_{REF} In	± Reference voltage input	19	$\overline{\text{CLK}}$	Clock input
11	Inv Out	Inverter (A_5) output	18	Data Out	Serial data output
12	AGND	Analog common	17	DGND	Digital common
13	V_{OUT} D	Analog output voltage, DAC D	16	NC	No internal connection
14	V_{OUT} C	Analog output voltage, DAC C	15	$+V_S$	Positive analog power supply, +15V input

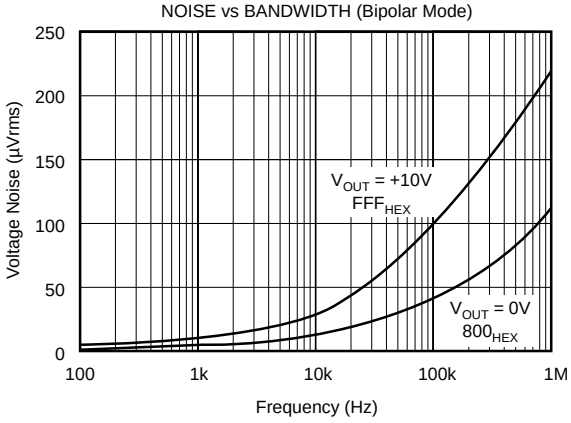
PIN CONFIGURATION



TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_S = ±12V or ±15V, V_L = +5V unless otherwise noted.

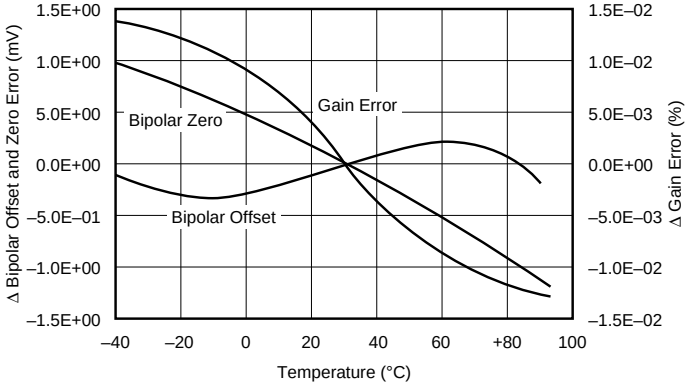




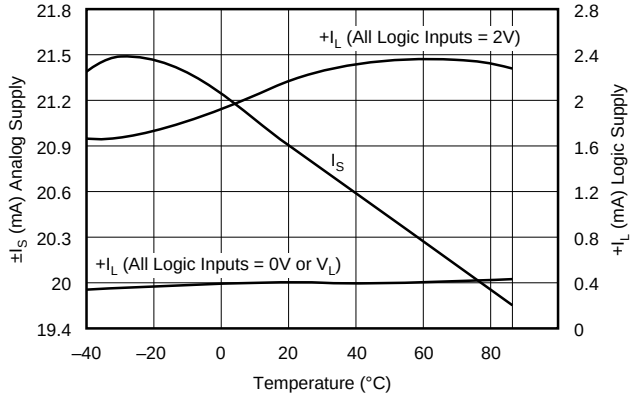
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±12V or ±15V, V_L = +5V unless otherwise noted.

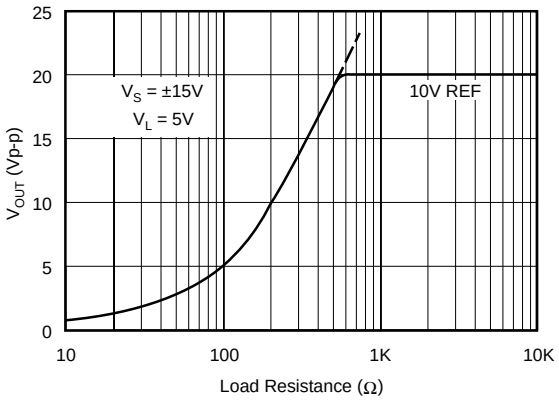
CHANGE OF GAIN, BIPOLAR OFFSET AND ZERO ERROR vs TEMPERATURE



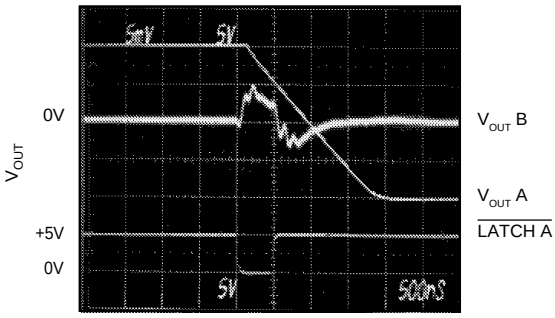
POWER SUPPLY CURRENT vs TEMPERATURE



OUTPUT VOLTAGE SWING vs RESISTOR LOAD



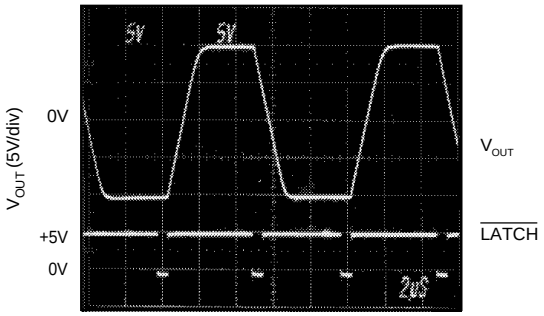
CROSSTALK (Bipolar Mode)



Time (500ns/div)

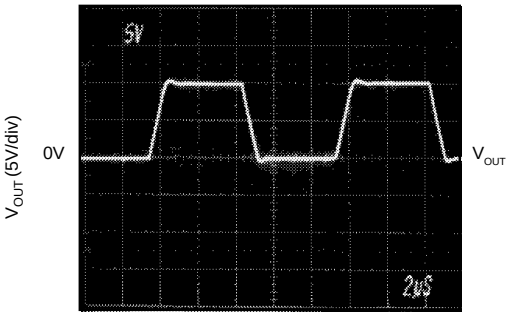
NOTE: Crosstalk is dominated by digital crosstalk/ feedthrough of the $\overline{\text{LATCH}}$ signal.

FULL-SCALE OUTPUT SWING BIPOLAR (20V Step)



Time (2µs/div)

FULL-SCALE OUTPUT SWING UNIPOLAR (10V Step)

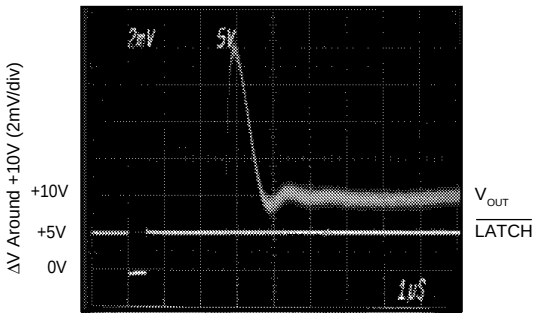


Time (2µs/div)

TYPICAL PERFORMANCE CURVES (CONT)

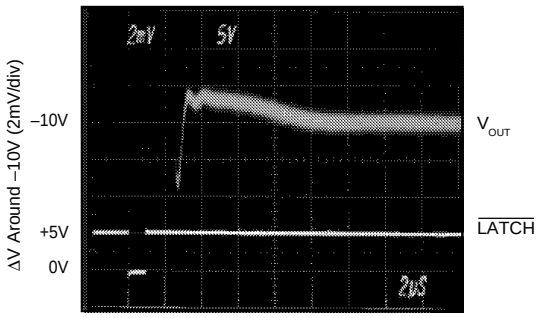
T_A = +25°C, V_S = ±12V or ±15V, V_L = +5V unless otherwise noted.

SETTLING TIME
BIPOLAR (–10V to +10V)



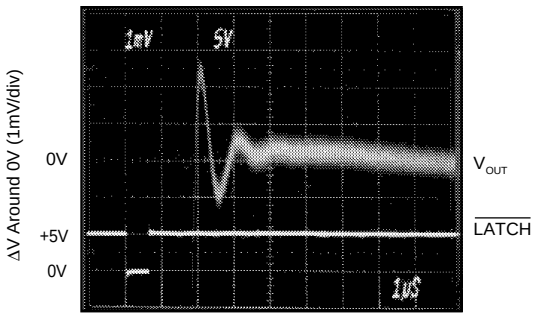
Time (1µs/div)

SETTLING TIME
BIPOLAR (+10V to –10V Step)



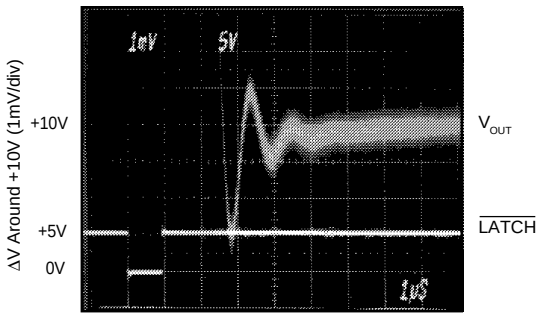
Time (2µs/div)

SETTLING TIME
UNIPOLAR (+10V to 0V STEP)



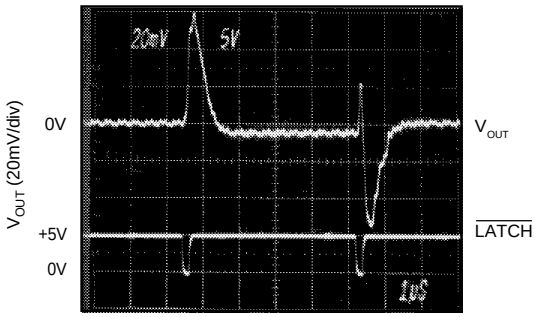
Time (1µs/div)

SETTLING TIME
UNIPOLAR (0V to +10V Step)



Time (1µs/div)

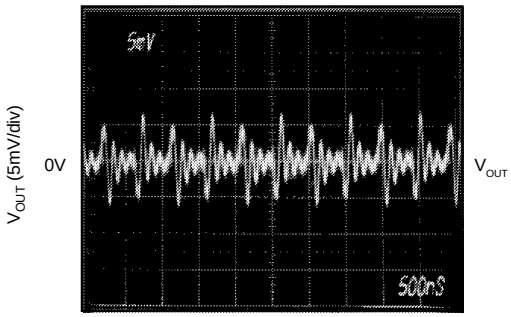
MAJOR CARRY GLITCH



Time (1µs/div)

NOTE: Data transition 800_{HEX} to $7FF_{HEX}$.

DIGITAL FEEDTHROUGH



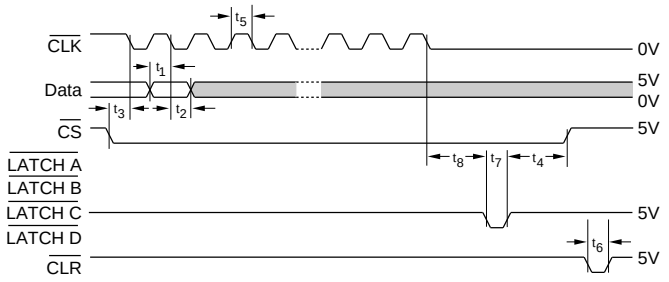
Time (500ns/div)

DAC output noise due to activity on digital inputs with latch disabled.

TIMING CHARACTERISTICS

V_S = ±15V, V_L = +5V, T_A = –40°C to +85°C.

PARAMETER	MINIMUM
t_1—Data Setup Time	15ns
t_2—Data Hold Time	15ns
t_3—Chip Select to $\overline{CLK}$, Latch, Data Setup Time	15ns
t_4—Chip Select to $\overline{CLK}$, Latch, Data Hold Time	40ns
t_5—$\overline{CLK}$ Pulse Width	40ns
t_6—Clear Pulse Width	40ns
t_7—Latch Pulse Width	40ns
t_8—$\overline{CLK}$ Edge to $\overline{LATCH\ A}$, $\overline{LATCH\ B}$, $\overline{LATCH\ C}$, or $\overline{LATCH\ D}$	15ns



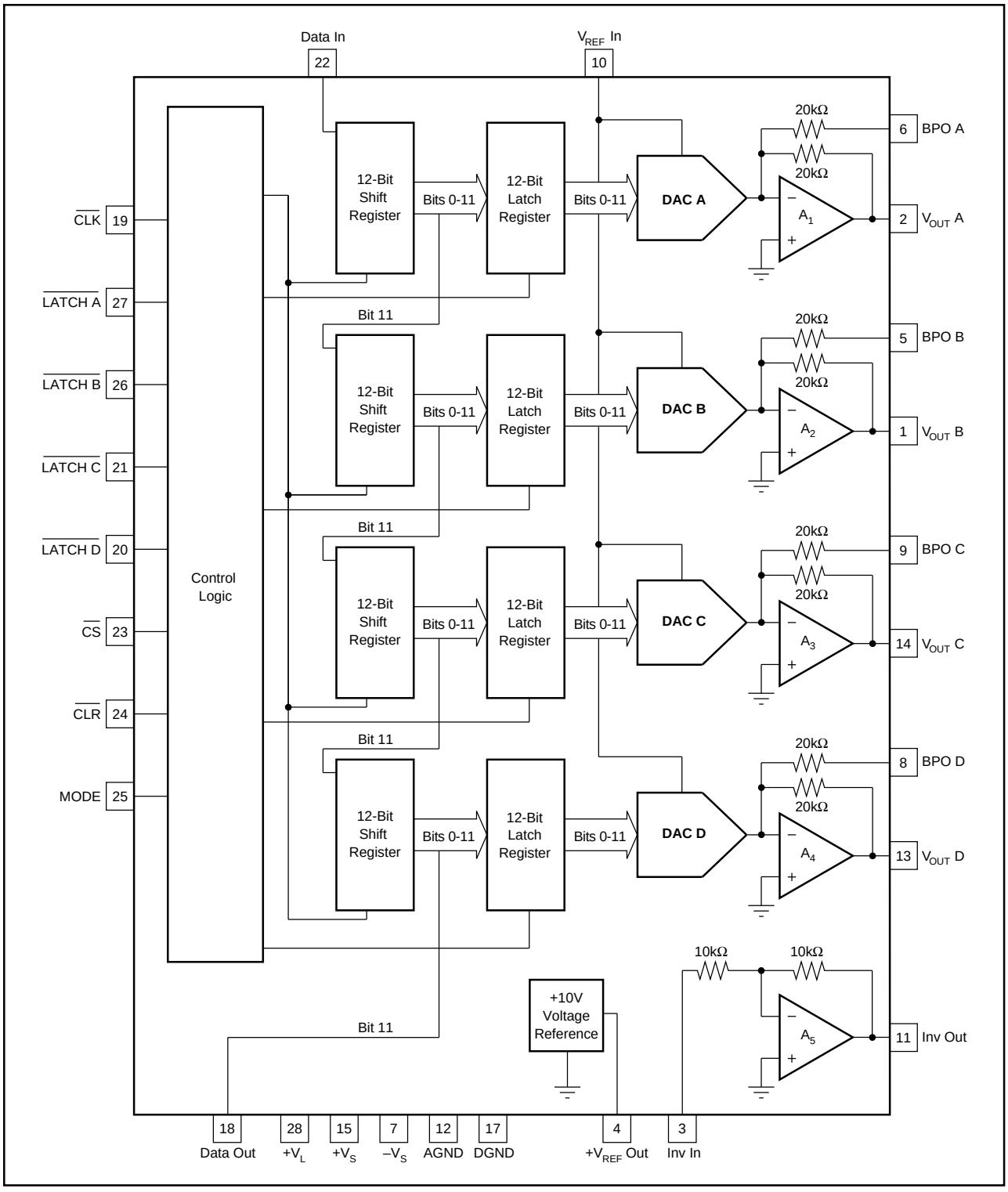
NOTES: (1) All input signal rise and fall times are measured from 10% to 90% of +5V • $t_R = t_F$ = 5ns.
(2) Timing measurement reference level is $\frac{V_{IH} + V_{IL}}{2}$.

INTERFACE LOGIC TRUTH TABLE

MODE	$\overline{CLR}$	$\overline{CLK}$	$\overline{CS}$	$\overline{LATCH\ A}$	$\overline{LATCH\ B}$	$\overline{LATCH\ C}$	$\overline{LATCH\ D}$	FUNCTION
X	1	↓	0	X	X	X	X	Data clocked in
X	1	X	1	X	X	X	X	No data transfer
X	1	X	0	0	1	1	1	DAC A register updated
X	1	X	0	1	0	1	1	DAC B register updated
X	1	X	0	1	1	0	1	DAC C register updated
X	1	X	0	1	1	1	0	DAC D register updated
X	1	X	0	0	0	0	0	All DAC registers updated simultaneously
0	0	X	X	X	X	X	X	All registers cleared
1	0	X	X	X	X	X	X	Shift registers cleared = 000_{HEX}, DAC registers = 800_{HEX}

Note: X = Don't Care. ↓ = Falling edge triggered.

FUNCTIONAL BLOCK DIAGRAM, DAC4814 — Quad 12-bit DAC, Serial Port



DISCUSSION OF SPECIFICATIONS

INPUT CODES

All digital inputs of the DAC4814 are TTL and 5V CMOS compatible. Input codes for the DAC4814 are either USB (Unipolar Straight Binary) or BOB (Bipolar Offset Binary) depending on the mode of operation. See Figure 3 for ±10V bipolar connection. See Figures 4 and 5 for 0 to 10V and 0 to –10V unipolar connections.

UNIPOLAR AND BIPOLAR OUTPUTS FOR SELECTED INPUT

DIGITAL INPUT	UNIPOLAR (USB)	BIPOLAR (BOB)
FFF_{HEX}	+Full scale	+Full scale
800_{HEX}	+1/2 Full scale	Zero
$7FF_{HEX}$	+1/2 Full scale – 1 LSB	Zero – 1 LSB
000_{HEX}	Zero	–Full scale

INTEGRAL OR RELATIVE LINEARITY

This term, also known as end point linearity, describes the transfer function of analog output to digital input code. Integral linearity error is the deviation of the analog output versus code transfer function from a straight line drawn through the end points.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is the deviation from an ideal 1 LSB change in the output voltage when the input code changes by 1 LSB. A differential nonlinearity specification of ±1 LSB maximum guarantees monotonicity.

UNIPOLAR OFFSET ERROR

The output voltage for code 000_{HEX} when the DAC is in unipolar mode of operation.

BIPOLAR ZERO ERROR

The output voltage for code 800_{HEX} when the DAC is in the bipolar mode of operation.

GAIN ERROR

The deviation of the output voltage span ($V_{MAX} - V_{MIN}$) from the ideal span of 10V – 1 LSB (unipolar mode) or 20V – 1 LSB (bipolar mode). The gain error is specified with and without the internal +10V reference error included.

OUTPUT SETTLING TIME

The time required for the output voltage to settle within a percentage-of-full-scale error band for a full scale transition. Settling to ±0.012% (1/2 LSB) is specified for the DAC4814.

DIGITAL-TO-ANALOG GLITCH

Ideally, the DAC output would make a clean step change in response to an input code change. In reality, glitches occur during the transition. See Typical Performance Curves.

DIGITAL CROSSTALK

Digital crosstalk is the glitch impulse measured at the output of one DAC due to a full scale transition on the other DAC—see Typical Performance Curves. It is dominated by digital coupling. Also, the integrated area of the glitch pulse is specified in nV–s. See table of electrical specifications.

DIGITAL FEEDTHROUGH

Digital feedthrough is the noise at a DAC output due to activity on the digital inputs—see Typical Performance Curves.

OPERATION

DACs can be updated simultaneously or independently as required. Data are transferred on falling clock edges into a 48-bit shift register. DAC D MSB is loaded first. Data are transferred to the DAC registers when the $\overline{\text{LATCH}}$ signals are brought low. The data are latched when the $\overline{\text{LATCH}}$ signals are brought high. All $\overline{\text{LATCH}}$ signals may be tied together to allow simultaneous update of the DACs if required. The output of the DAC shift register is provided to allow cascading of several DACS on the same bit stream. By using separate signals for $\overline{\text{LATCH A}}$, $\overline{\text{LATCH B}}$, $\overline{\text{LATCH C}}$, and $\overline{\text{LATCH D}}$ it is possible to update one of the four DACs every 12 clock cycles.

When $\overline{\text{CLR}}$ is brought low, the input shift registers are cleared to 000_{HEX} while the DAC registers = 800_{HEX}. If $\overline{\text{LATCH}}$ is brought low after $\overline{\text{CLR}}$, the DACs are updated with 000_{HEX} resulting in –10V (bipolar) or 0V (unipolar) on the output.

CIRCUIT DESCRIPTION

Each of the four DACs in the DAC4814 consists of a CMOS logic section, a CMOS DAC cell, and an output amplifier. One buried-zener +10.0V reference and a reference inverter (for a –10.0V reference) are shared by all DACs.

Figure 1 is a simplified circuit for a DAC cell. An R, 2R ladder network is driven by a voltage reference at V_{REF}. Current from the ladder is switched either to I_{OUT} or AGND by 12 single-pole double-throw CMOS switches. This maintains constant current in each leg of the ladder regardless of digital input code. This makes the resistance at V_{REF} constant (it can be driven by either a voltage or current reference). The reference can be either positive or negative polarity with a range of up to ±10V.

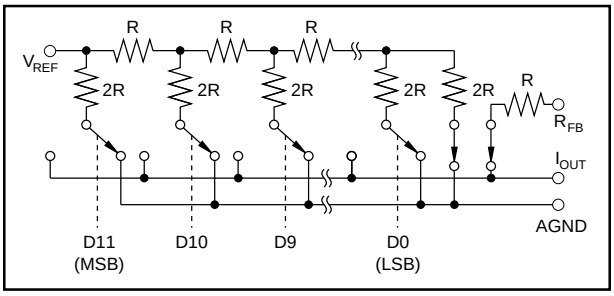


FIGURE 1. Simplified Circuit Diagram of DAC Cell.

CMOS switches included in series with the ladder terminating resistor and the feedback resistor, R_{FB}, compensate for the temperature drift of the ladder switch ON resistance.

The output op amps are connected as transimpedance amplifiers to convert the DAC-cell output current into an output voltage. They have been specially designed and compensated for precision and fast settling in this application.

POWER SUPPLY CONNECTIONS

The DAC4814 is specified for operation with power supplies of V_L = +5V and V_S = either ±12V or ±15V. Even with the V_S supplies at ±11.4V the DACs can swing a full ±10V. Power supply decoupling capacitors (1µF tantalum) should be located close to the DAC power supply connections.

Separate digital and analog ground pins are provided to permit separate current returns. They should be connected together at one point. Proper layout of the two current returns will prevent digital logic switching currents from degrading the analog output signal. The analog ground current is code dependent so the impedance to the system reference ground must be kept to a minimum. Connect DACs as shown in Figure 2 or use a ground plane to keep ground impedance less than 0.1Ω for less than 0.1LSB error.

–10V REFERENCE

An internal inverting amplifier (Gain = –1.0V/V) is provided to invert the +10V reference. Connect $+V_{REF}$ Out to Inv In for a –10V reference at Inv Out.

OUTPUT RANGE CONNECTIONS

±10V Output Range

For a ±10V bipolar output connect the DAC4814 as shown in Figure 3. Connect the MODE to logic high (+5V) for reset to bipolar zero. With MODE connected low (GND) reset will be to –Full-Scale.

0 To +10V Output Range

For 0 to +10V unipolar outputs connect the DAC4814 as shown in Figure 4. Connect the MODE to logic low (GND) for reset to unipolar zero.

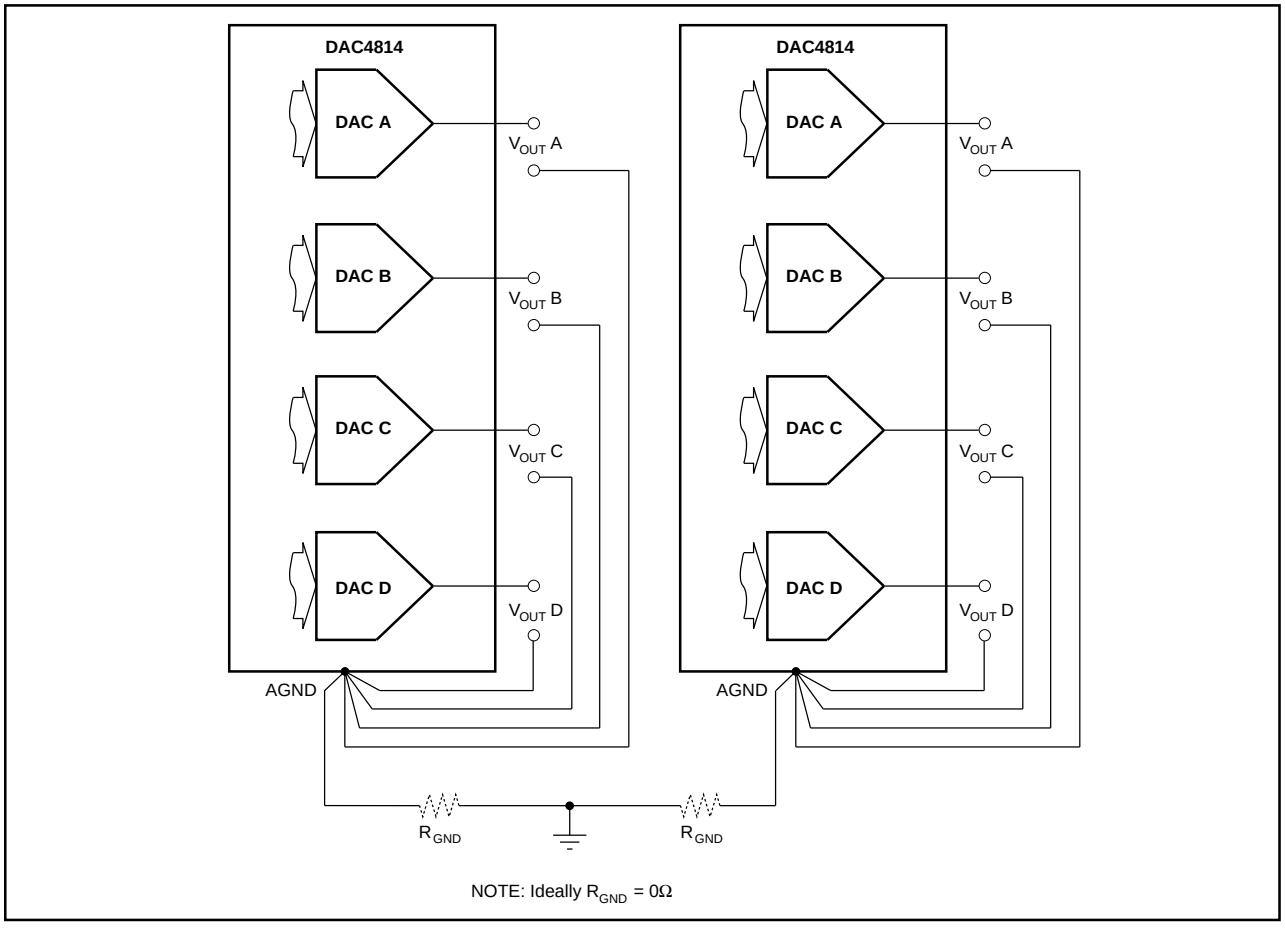


FIGURE 2. Recommended Ground Connections for Multiple DAC Packages.

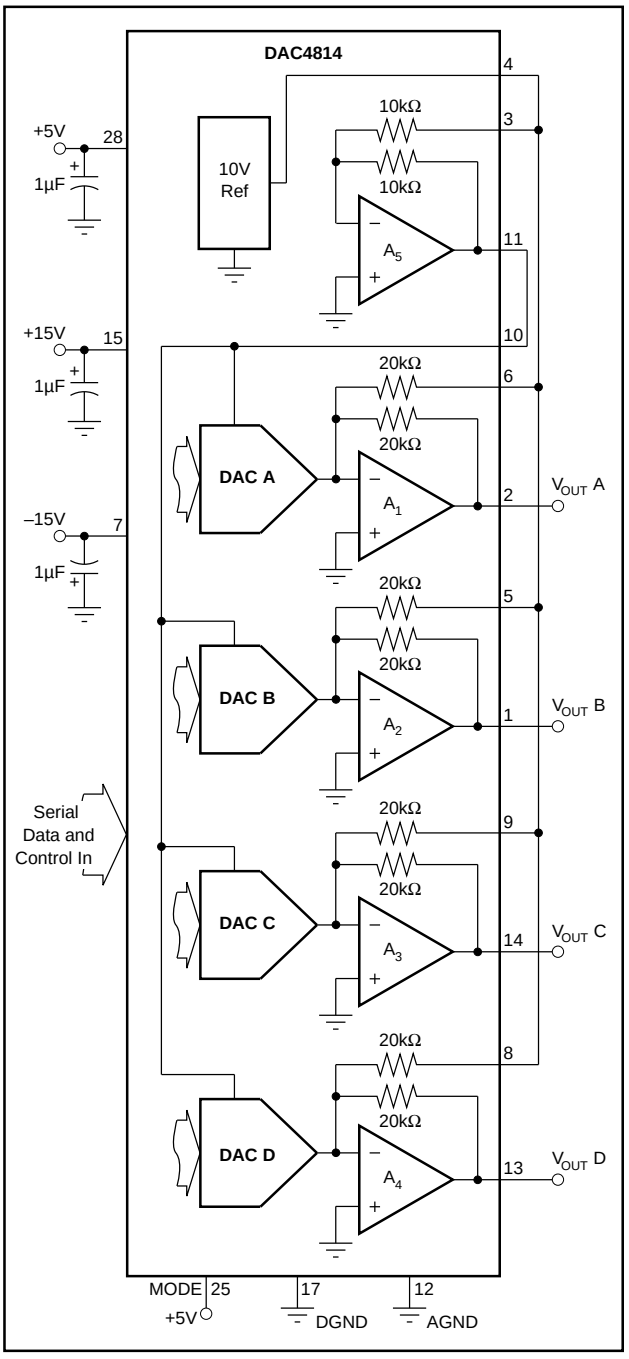


FIGURE 3. Analog Connections for ±10V DAC Output.

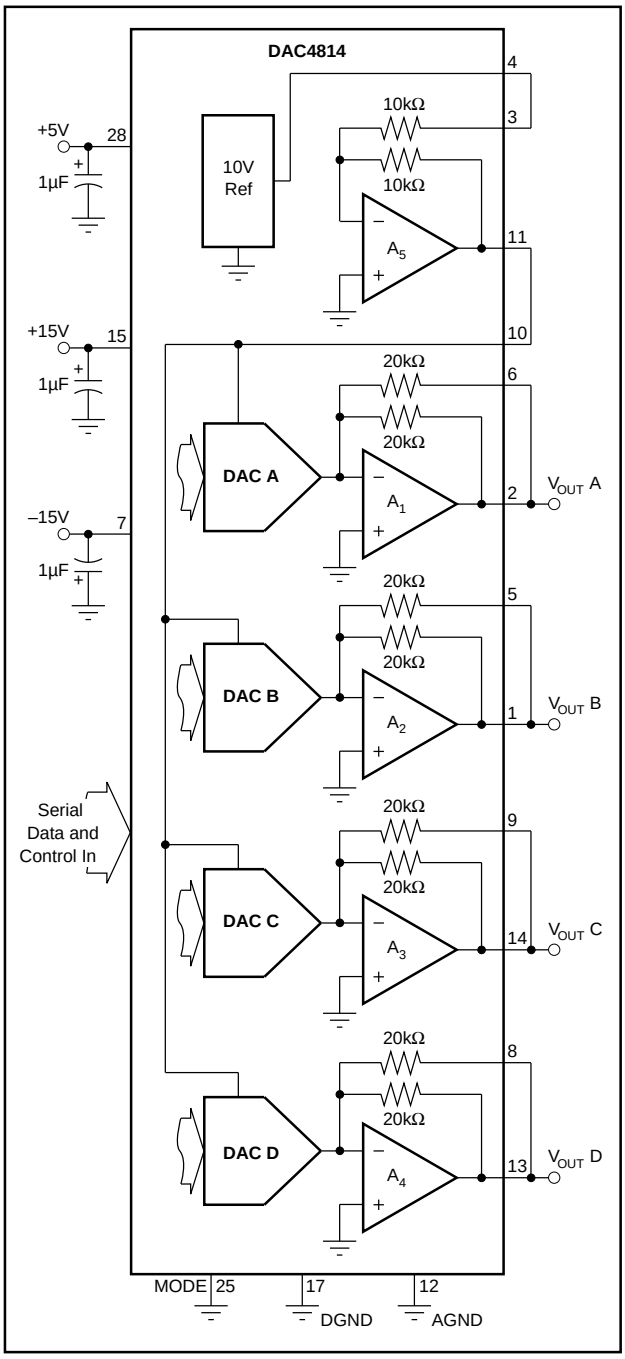


FIGURE 4. Analog Connections for 0 to +10V DAC Output.

0 To –10V Output Range

For 0 to –10V unipolar outputs connect the DAC4814 as shown in Figure 5. Connect the MODE to logic low (GND) for reset to unipolar zero.

CONNECTION TO DIGITAL BUS

Cascaded Bus Connection

Multiple DAC4814s can be connected to the same $\overline{CLK}$ and DATA input lines in two ways. Since the output of the DAC shift register is available, any number of DAC4814s can be cascaded on the same input bit stream as shown in Figure 6. This arrangement allows all DACs in the system to be updated simultaneously and requires a minimum number of control signal inputs. However, up to 48N $\overline{CLK}$ cycles may be required to update any given DAC, where N = number of DAC4814s.

Parallel Bus Connection

Several DAC4814s can also have their DATA inputs connected in parallel as shown in Figure 7. This allows any DAC in the system to be updated in a maximum of 48 $\overline{CLK}$ cycles.

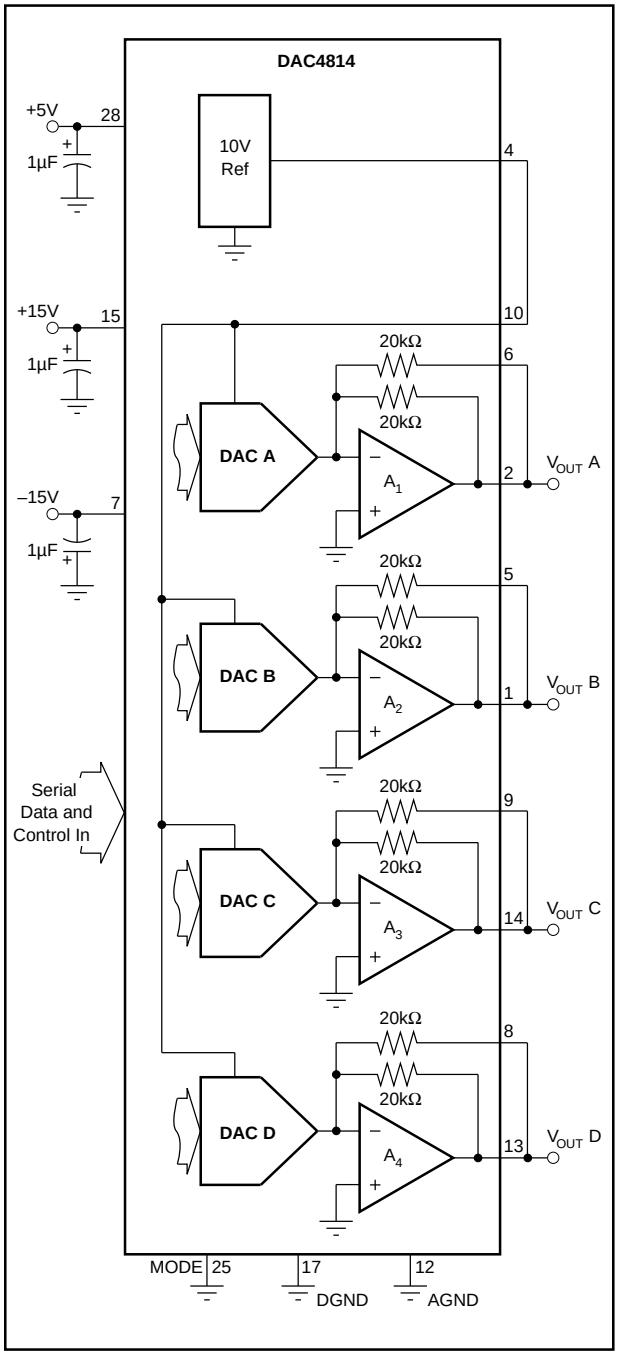


FIGURE 5. Analog Connections for 0 to –10V DAC Output.

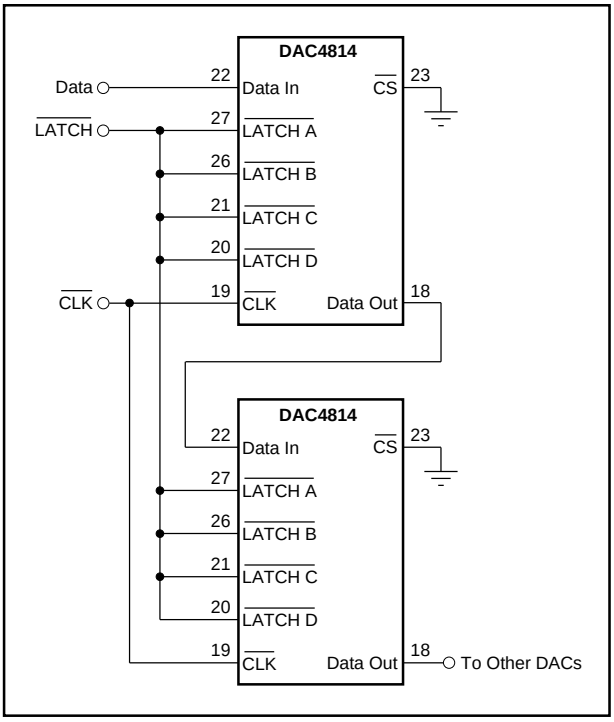


FIGURE 6. Cascaded Serial Bus Connection for Multiple DAC Packages.

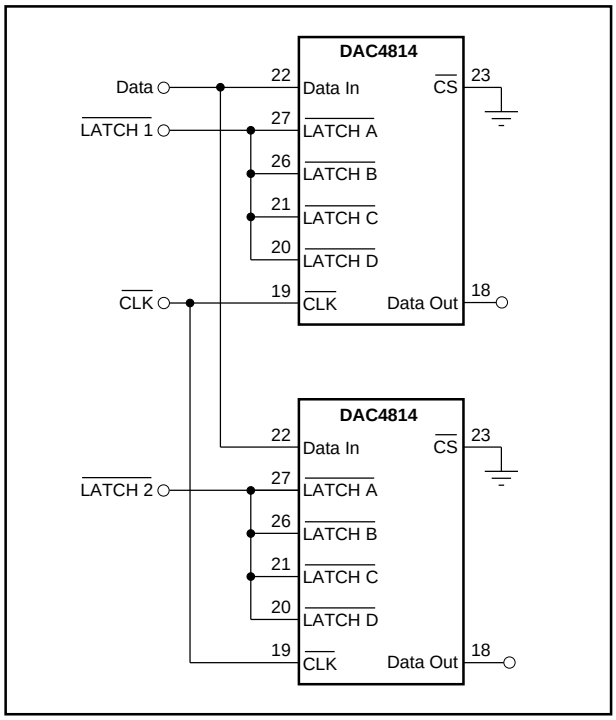


FIGURE 7. Parallel Bus Connection for Multiple DAC Packages.