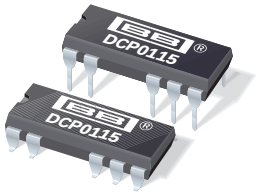
BURR - BROWN®



DCP0115 Series

Miniature 15V Input, 1W Isolated UNREGULATED DC/DC CONVERTERS

FEATURES

- STANDARD JEDEC PLASTIC PACKAGE
- LOW PROFILE: 0.15" (3.8mm)
- SYNCHRONIZABLE
- OUTPUT SHORT CIRCUIT PROTECTION
- THERMAL SHUTDOWN
- STARTS INTO ANY CAPACITIVE LOAD
- EFFICIENCY: 76% (at Full Load)
- 1000Vrms ISOLATION
- 400kHz SWITCHING
- 93 MILLION HOURS MTTF
- AVAILABLE IN TAPE AND REEL

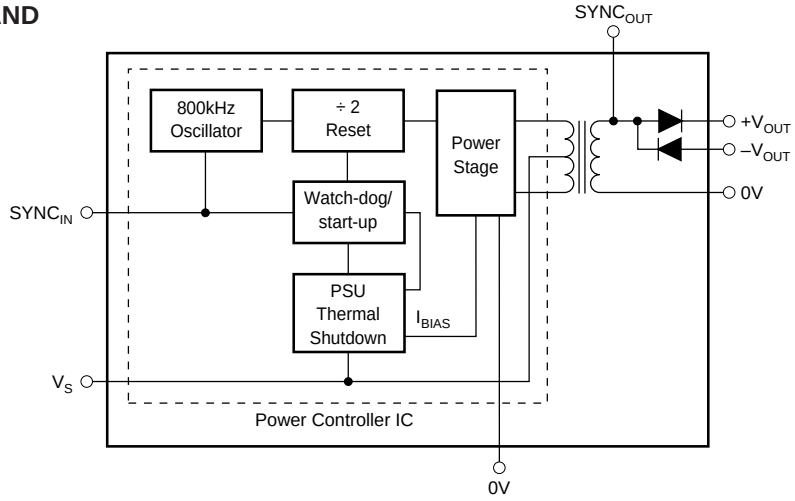
APPLICATIONS

- POINT OF USE POWER CONVERSION
- GROUND LOOP ELIMINATION
- DATA ACQUISITION
- INDUSTRIAL CONTROL AND INSTRUMENTATION
- TEST EQUIPMENT

DESCRIPTION

The DCP0115 family is a series of high efficiency, 15V input isolated DC/DC converters. In addition to 1W nominal galvanically isolated output power capability, the range of DC/DCs are also fully synchronizable. The devices feature thermal shutdown, and overload protection is implemented via watchdog circuitry. Advanced power-on reset techniques give superior reset performance and the devices will start into any capacitive load up to full power output.

The DCP01 family is implemented in standard-molded IC packaging, giving outlines suitable for high volume assembly.



International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

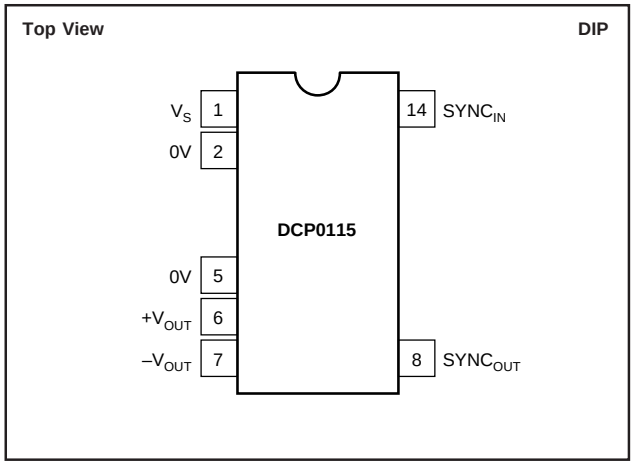
SPECIFICATIONS

At T_A = +25°C, V_S = +15V, unless otherwise specified.

PARAMETER	CONDITIONS	DCP0115 SERIES			UNITS
		MIN	TYP	MAX	
OUTPUT					
Power	V_S + 4%		1		W
	100% Full Load		0.92		W
Voltage (V_{NOM})[1]					
DCP011512D	75% Full Load	±10	±12	±12.6	V
DCP011515D	75% Full Load	±13	±15	±15.75	V
Voltage vs Temperature			±0.08		%/°C
Short Circuit Duration	V_S ± 10%	Indefinite			
Ripple	C_L = O/P Capacitor = 10µF		6		mVp-p
	100% Full Load				
INPUT					
Nominal Voltage (V_S)			15		V
Voltage Range		–10		10	%
Supply Current	100% Full Load		83		mA
Reflected Ripple Current	C_{IN} = I/P Capacitor = 1µF		8		mArms
	50% Full Load				
ISOLATION					
Voltage[2]	1s Flash Test	1			kVrms
Continuous Voltage[3]			1		kVrms
Insulation Resistance			>1		GΩ
Input/Output Capacitance			2.5		pF
LOAD REGULATION					
DCP011512D	10% to 100% Load		20	39	%
	10% to 25% Load		10		%
	25% to 75% Load		5		%
	75% to 100% Load		–7		%
DCP011515D	10% to 100% Load		20	39	%
	10% to 25% Load		10		%
	25% to 75% Load		9		%
	75% to 100% Load		–4		%
SWITCHING/SYNCHRONIZATION					
Oscillator Frequency (f_{OSC})	Switching Frequency = f_{OSC}/2		800		kHz
Sync Input Low		0		0.8	V
Sync Input Current	V_{SYNC} = +2V		48		µA
Reset Time			3.8		µs
$SYNC_{OUT}$ Frequency			400		kHz
GENERAL					
No Load Current					
DCP011512D	0% Load		14		mA
DCP011515D	0% Load		17		mA
Efficiency					
DCP011512D	100% Full Load		76		%
	10% Full Load		48		%
DCP011515D	100% Full Load		76		%
	10% Full Load		42		%
MTTF[3]	T_A = +85°C	136,000			hrs
	T_A = +55°C	2,630,000			hrs
	T_A = +25°C	92,600,000			hrs
Weight	14-Pin PDIP		1.08		g
THERMAL SHUTDOWN					
Die Temperature		115		140	°C
Shutdown Current			3		mA
TEMPERATURE RANGE					
Operating		–40		100	°C

NOTES: (1) 100 % load current = 1W/V_{NOM} typical. (2) Rated working voltage = 130Vrms (IEC950 convention). (3) Life test data.

PIN CONFIGURATION (Dual Out)



ABSOLUTE MAXIMUM RATINGS

Input Voltage	18V
Storage Temperature	–60°C to +150°C
Lead Temperature (soldering, 10s)	300°C

ORDERING INFORMATION

DCP01 15 15 D ( )

- Basic Model Number: 1W Product
- Voltage Input: 15V In
- Voltage Output: 15V Out
- Dual Output:
- Package Code:
  - P = 14-Pin Plastic DIP
  - P-U = 14-Pin Plastic DIP Gull Wing

PIN DEFINITION

PIN #	PIN NAME	DESCRIPTION
1	V_S	Voltage Input.
2	0V	Input Side Common.
5	0V	Output Side Common.
6	$+V_{OUT}$	+Voltage Out.
7	$-V_{OUT}$	–Voltage Out.
8	$SYNC_{OUT}$	Unregulated 400kHz Output from Transformer.
14	$SYNC_{IN}$	Synchronization Pin.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

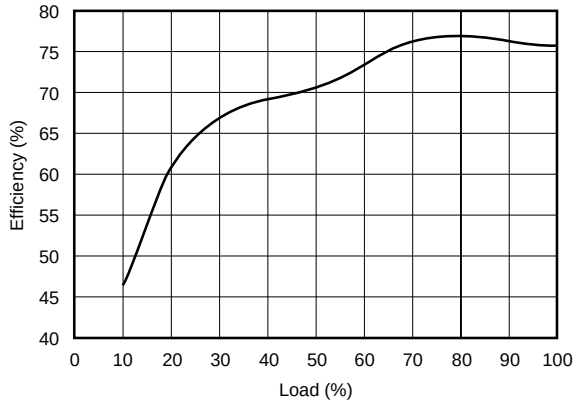
PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER(1)	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER(2)	TRANSPORT MEDIA
Dual						
DCP011512D	14-Pin PDIP	010-1	–40°C to +100°C	DCP011512DP	DCP011512DP	Rails
DCP011512D	14-Pin PDIP Gull Wing	010-2	–40°C to +100°C	DCP011512DP-U	DCP011512DP-U	Rails
"	"	"	"	"	DCP011512DP-U/700	Tape and Reel
DCP011515D	14-Pin PDIP	010-1	–40°C to +100°C	DCP011515DP	DCP011515DP	Rails
DCP011515D	14-Pin PDIP Gull Wing	010-2	–40°C to +100°C	DCP011515DP-U	DCP011515DP-U	Rails
"	"	"	"	"	DCP011515DP-U/700	Tape and Reel

NOTES: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book. (2) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /700 indicates 700 devices per reel). Ordering 700 pieces of DCP011512DP-U/700 will get a single 700-piece Tape and Reel. For detailed Tape and Reel mechanical information, refer to Appendix B of Burr-Brown IC Data Book.

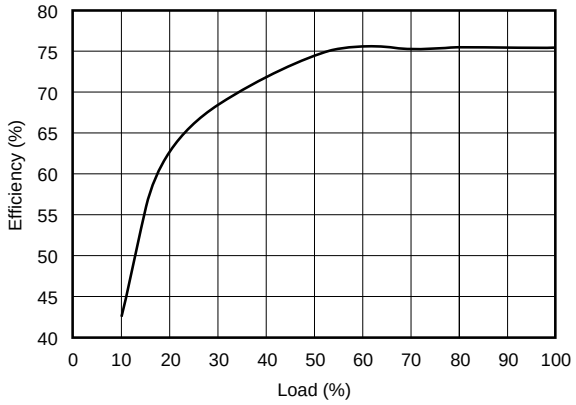
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, unless otherwise noted.

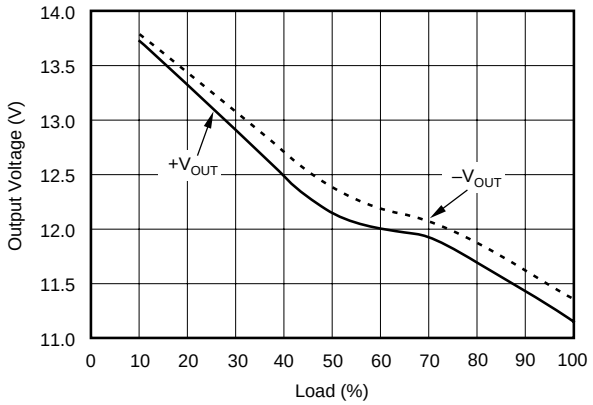
DCP011512D
EFFICIENCY vs LOAD



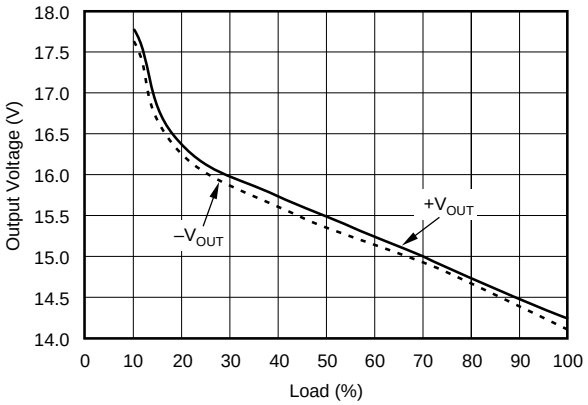
DCP011515D
EFFICIENCY vs LOAD



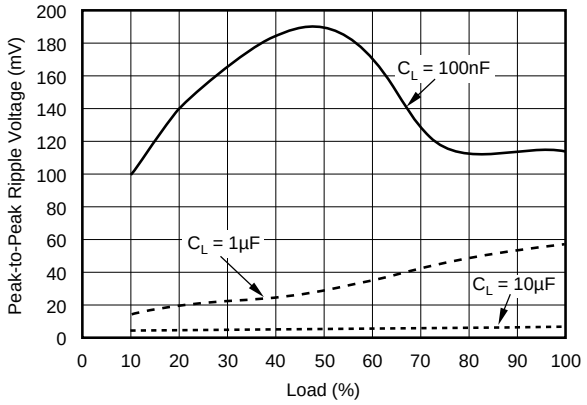
DCP011512D
OUTPUT VOLTAGE vs LOAD



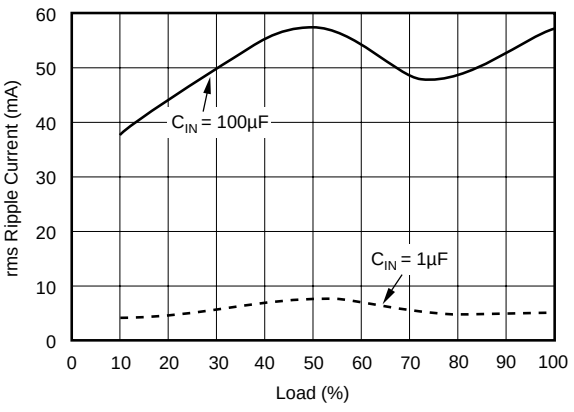
DCP011515D
OUTPUT VOLTAGE vs LOAD



PEAK-TO-PEAK RIPPLE VOLTAGE vs LOAD



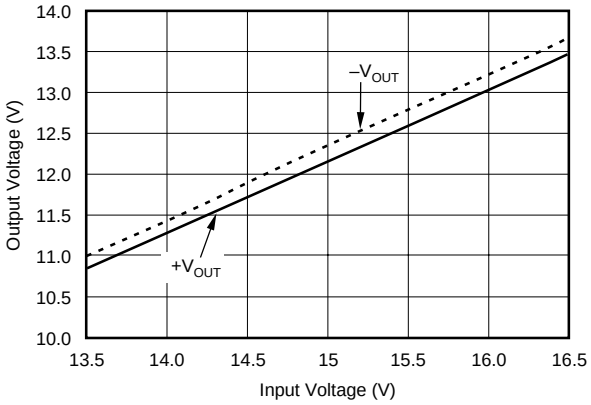
REFLECTED rms RIPPLE CURRENT vs LOAD



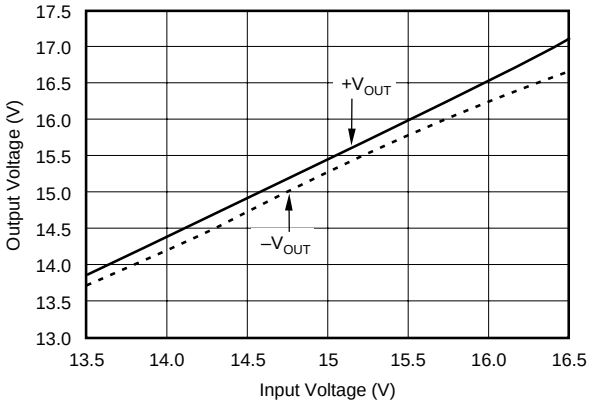
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, unless otherwise noted.

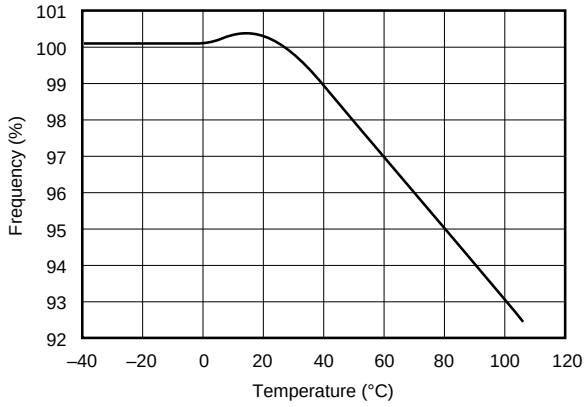
DCP011512D
OUTPUT VOLTAGE vs INPUT VOLTAGE (75% Load)



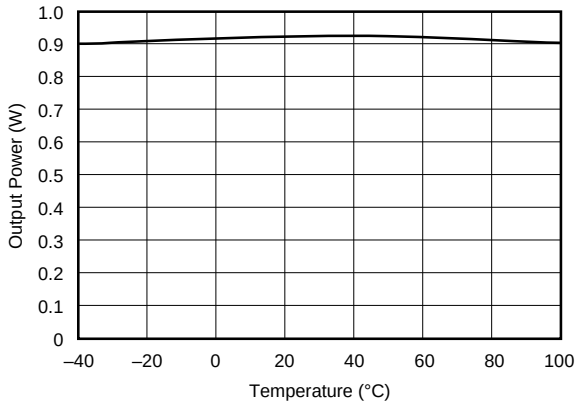
DCP011515D
OUTPUT VOLTAGE vs INPUT VOLTAGE (75% Load)



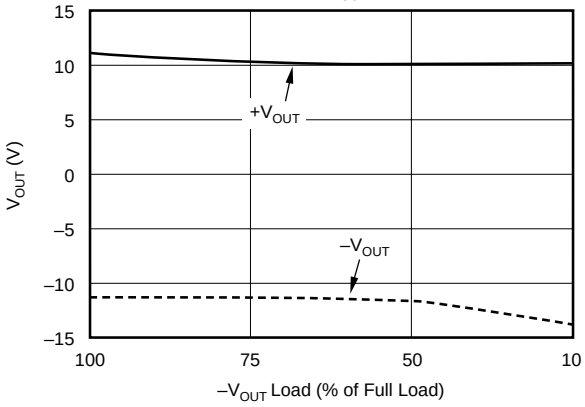
SWITCHING FREQUENCY vs TEMPERATURE



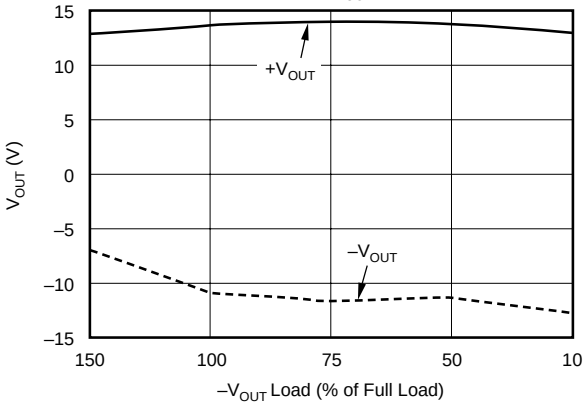
OUTPUT POWER vs TEMPERATURE



DCP011512D
LOAD BALANCE (+V_{OUT} LOAD = 100%)



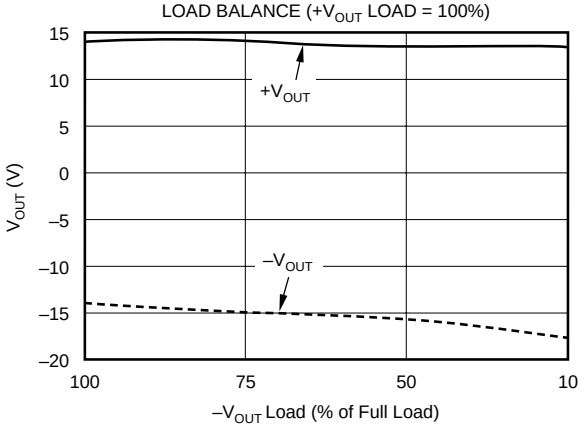
DCP011512D
LOAD BALANCE (+V_{OUT} LOAD = 10%)



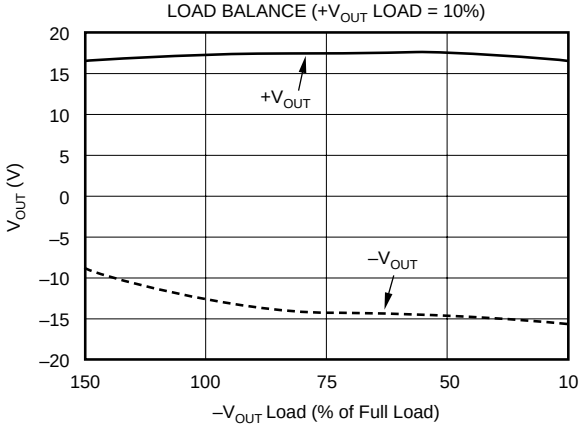
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, unless otherwise noted.

DCP011515D
LOAD BALANCE ($+V_{OUT}$ LOAD = 100%)



DCP011515D
LOAD BALANCE ($+V_{OUT}$ LOAD = 10%)



FUNCTIONAL DESCRIPTION

OVERVIEW

The DCP0115 offers up to 1W of unregulated output power from a 15V input source with a typical efficiency of 76%. This is achieved through highly integrated packaging technology and the implementation of a custom power stage and control IC.

POWER STAGE

This uses a pull-pull, center-tapped topology switching at 400kHz (divide by 2 from 800kHz oscillator).

OSCILLATOR AND WATCHDOG

The on-board 800kHz oscillator provides the switching frequency via a divide by 2 circuit and allows synchronization via the $SYNC_{IN}$ pins. To synchronize any number of DCP0115 family of devices, simply tie the $SYNC_{IN}$ pins together (see the Synchronization section). The watchdog circuitry protects the DC/DC against a stopped oscillator and checks the oscillator frequency which will shut down the output stage if it drops below a certain threshold—i.e., it will be tri-stated after approximately 10µs.

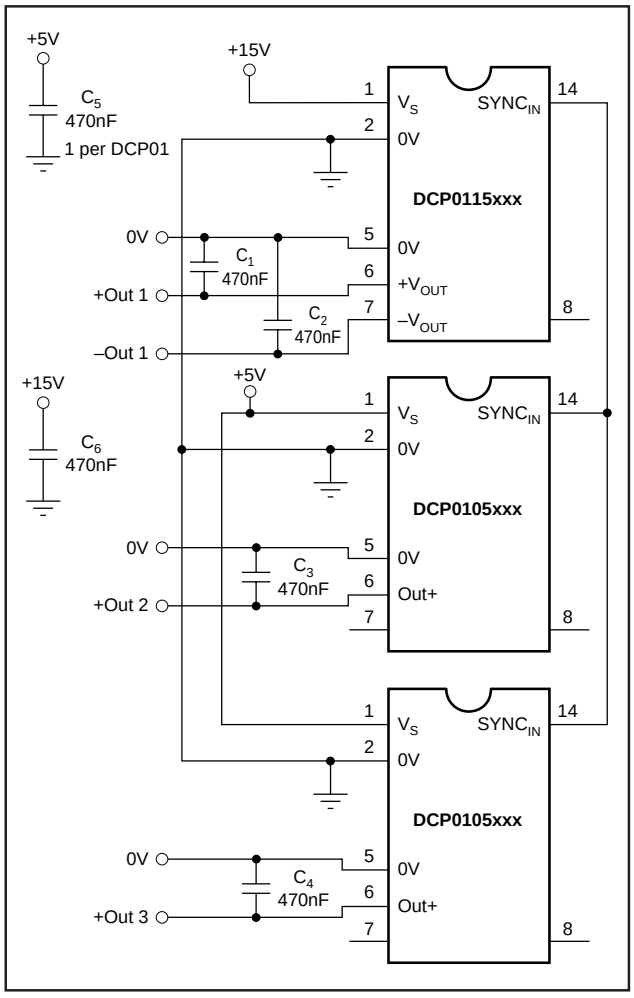


FIGURE 1. Standard Interface.

THERMAL SHUTDOWN

The DCP0115 is also protected by thermal shutdown. If the on-chip temperature reaches a predetermined value, the DC/DC will shutdown. This effectively gives indefinite short circuit protection for the DC/DC.

SYNCHRONIZATION

Any number of DCP01 family devices can be synchronized by connecting the $SYNC_{IN}$ pins on the devices together (see Figure 1). All the DCP01 devices will then self-synchronize.

This same synchronization method applies to any V_{IN} version of the DCP01 family, allowing synchronization of various V_{OUT} and V_{IN} DC/DCs.

The $SYNC_{OUT}$ pin gives an unrectified 400kHz signal from the transformer. This can be used to set the timing of external circuitry on the output side. In noise sensitive applications any pick-up from the $SYNC_{OUT}$ pin can be minimized by putting a guard ring round the pin (see Figure 2).

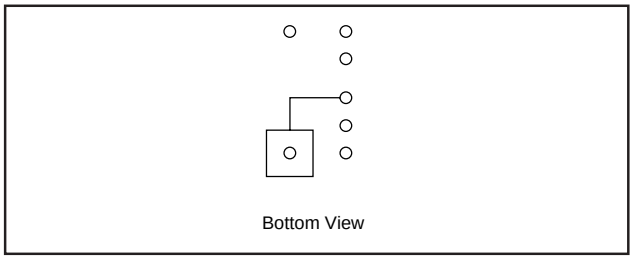


FIGURE 2. $SYNC_{OUT}$ Guard Ring.

DIVIDE BY 2 RESET

Isolated DC/DC converter performance normally suffers after power reset. This is because a change in the steady state transformer flux creates an offset after power-up. The DCP01 family does not suffer from this problem. This is achieved through a patented[1] technique employed on the divide by 2 reset circuitry resulting in no change in output phase after power interruption.

CONSTRUCTION

The DCP0115's basic construction is the same as standard ICs. There is no substrate within the molded package. The DCP0115 is constructed using an IC, rectifier diodes, and a wound magnetic toroid on a leadframe. As there is no solder within the package, the DCP0115 does not require any special PCB assembly processing. This results in an isolated DC/DC with inherently high reliability.

ADDITIONAL FUNCTIONS

DISABLE/ENABLE

The DCP0115 can be disabled or enabled by driving the $SYNC_{IN}$ pin with an open drain CMOS gate. If the $SYNC_{IN}$ pin is pulled low, the DCP0115 will disable. The disable time depends on the output loading but the internal shutdown takes

up to 10µs. Making the gate open drain will re-enable the DCP0115. However, there is a trade-off in using this function; the DCP0115 quiescent current may increase and the on-chip oscillator may run slower. This degradation in performance is dependent on the external CMOS gate capacitance, therefore the smaller the capacitance, the lower the performance decrease. Driving the $SYNC_{IN}$ pin with a CPU type tri-state output, which has a low output capacitance, offers the lowest reduction in performance.

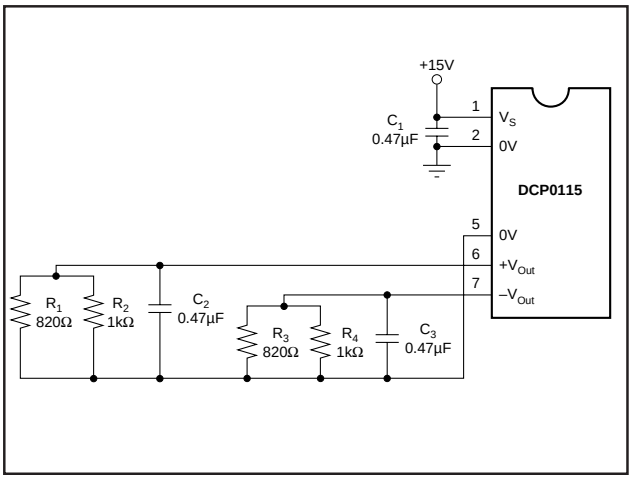


FIGURE 3. DCP011515 Fully Loaded.

DECOUPLING

Ripple Reduction

The high switching frequency of 400kHz allows simple filtering. To reduce ripple, it is recommended that 0.47µF capacitors are used on V_S and V_{OUT} (see Figure 3). Dual outputs should both be decoupled to pin 5. In applications where power is supplied over long lines and output loading is high, or, there is significant inductance at the output, it may be necessary to use a 2.2µF capacitor on the input to insure startup.

There is no restriction on the size of the output capacitor used to reduce ripple. The DCP0115 will start into any capacitive load. Low ESR capacitors will give the best reduction.

EXTERNAL SYNCHRONIZATION

The DCP0115 can be synchronized externally if required using a simple external interface. Figure 4 shows a universal interface using a 4066 quad switch. The CTL and $SYNC_{ON}$ pins are used to select external synchronization or self-synchronization.

This interface can also be used to stop (disable) the DCP0115.

CTL	$SYNC_{ON}$	FUNCTION
1	1	External Sync
—	0	Self-Sync
0	1	Device Stop

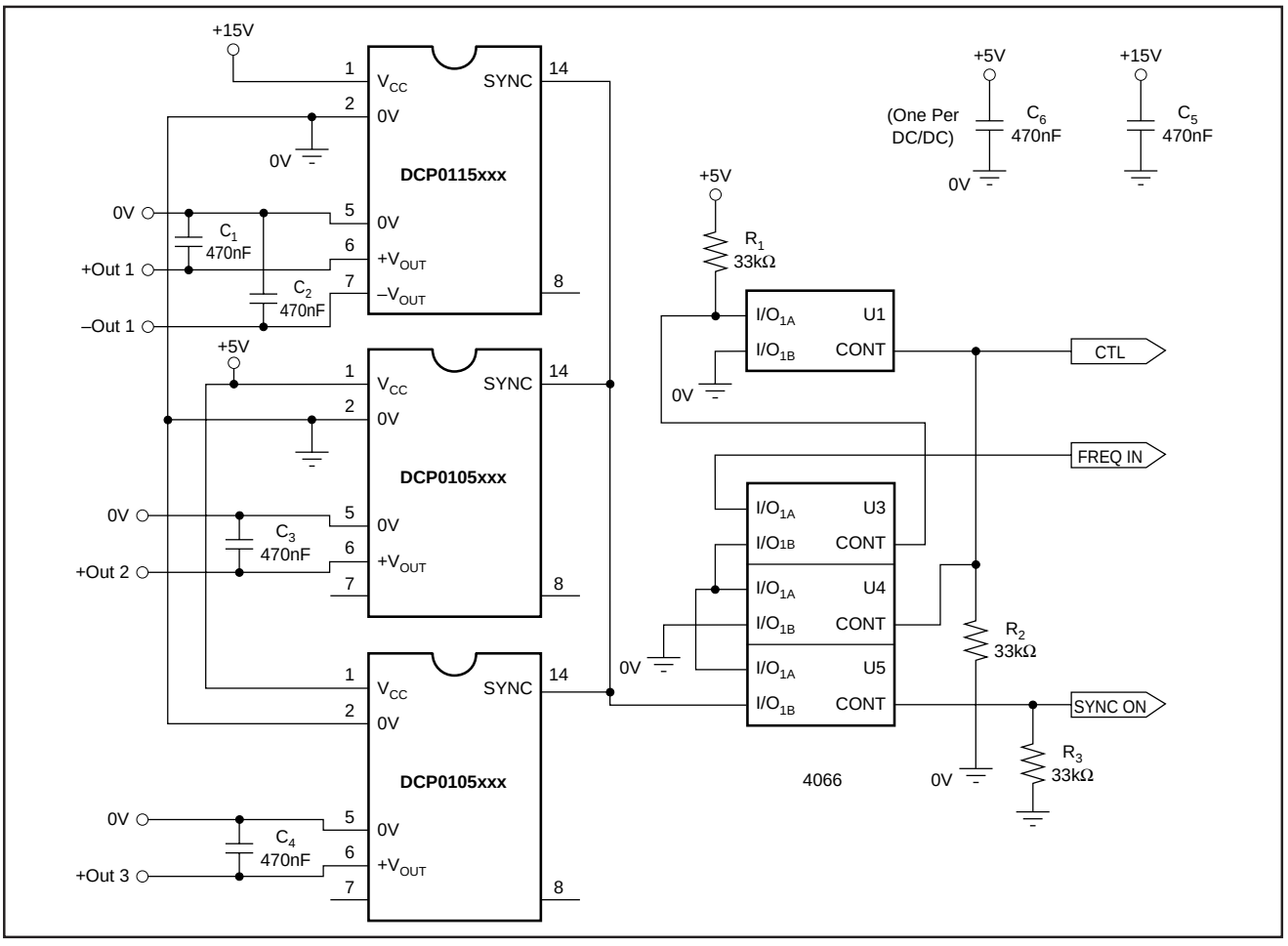


FIGURE 4. Universal Interface.

Connecting the DCP0115 in Series

Multiple DCP01 isolated 1W DC/DC converters can be connected in series to provide non-standard voltage rails. This is possible by utilizing the floating outputs provided by the DCP01's galvanic isolation. For example, the output on dual output DCP01 versions can be connected in series to provide 2 times the magnitude of V_{OUT} (see Figure 5). In this example, a dual 12V DCP011512D is connected to provide a 24V rail.

Connecting the DCP0115 in Parallel

If the output power from one DCP0115 is not sufficient, it is possible to parallel the outputs of multiple DCP0115s (see Figure 6). Again, the SYNC feature allows easy synchronization to prevent power-rail beat frequencies at no additional filtering cost.

PREDICTING OUTPUT VOLTAGE VERSUS LOAD

The Load Regulation specifications are calculated as follows:

CONDITION	CALCULATION
10% to 100% Load	(V_{OUT} at 10% load – V_{OUT} at 100% load)/ V_{OUT} at 75% load
10% to 25% Load	(V_{OUT} at 10% load – V_{OUT} at 25% load)/ V_{OUT} at 25% load
10% to 75% Load	(V_{OUT} at 10% load – V_{OUT} at 75% load)/ V_{OUT} at 75% load
75% to 100% Load	(V_{OUT} at 75% load – V_{OUT} at 100% load)/ V_{OUT} at 75% load

1. To predict the output voltage at 100% load take the measured or specified voltage at 75% load and multiply by (1 + Load Reg 75% to 100%). For example a DCP011512DP typical $+V_{OUT}$ at 100% load will be 12V x (1 – 7%) = 11.2V.
2. To predict the output voltage at 25% load take the measured or specified voltage at 75% load and multiply by (1 + Load Reg 25% to 75%). For example a DCP011512DP typical $+V_{OUT}$ at 25% load will be 12V x (1 + 5%) = 12.6V. To then estimate the voltage at 10% load take the previously calculated $+V_{OUT}$ at 25% load and multiply by (1 + Load Reg 10% to 25%). In this case the typical $+V_{OUT}$ at 10% load will be 12.6V x (1 + 10%) = 13.9V.

To obtain predictions for loads other than those specified assume the V_{OUT} versus load characteristic is linear between the load points and calculate accordingly. The 10% to 100% load specification guarantees the maximum voltage excursion for any load between 10% to 100% with respect to V_{OUT} at 75% load.

The above does not take into consideration line regulation and assumes a nominal input voltage. The 1:1 line regulation of the DCP01 family means that a percentage change in the input will give a corresponding percentage change in the output.

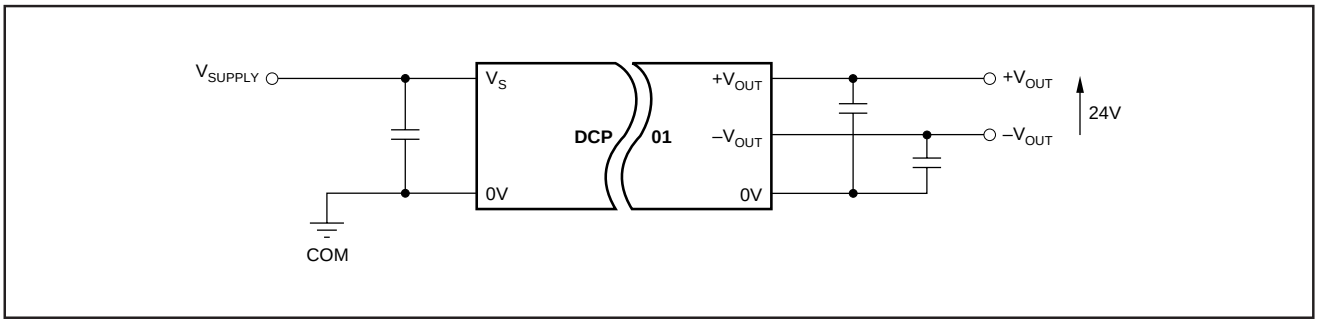


FIGURE 5. Connecting the DCP0115 in Series.

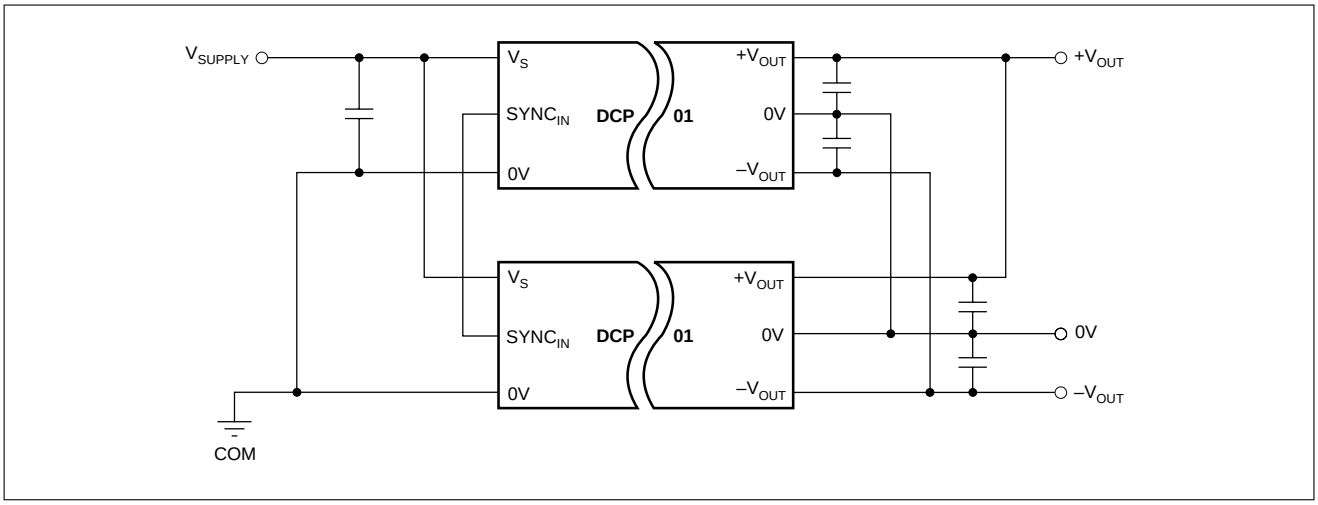


FIGURE 6. Connecting Multiple DCP0115s in Parallel.

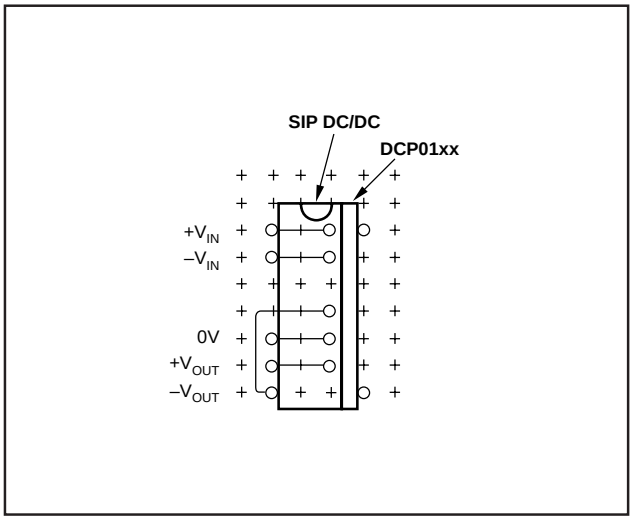


FIGURE 7. PCB Layout for DCP0115 and Competitive SIP DC/DC.

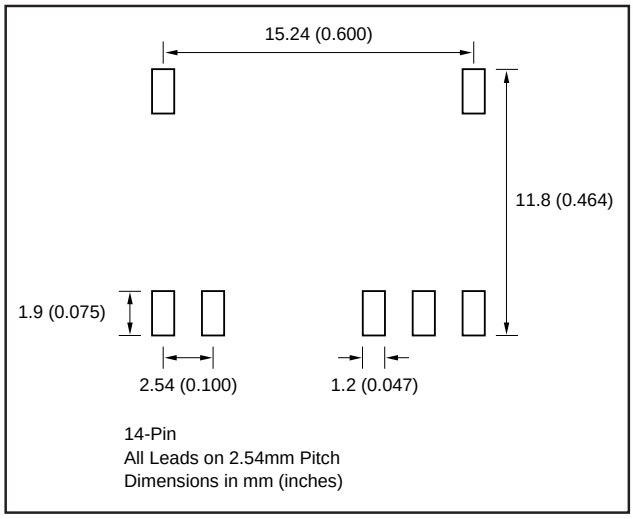


FIGURE 8. PCB Pad Size and Placement for “U” Package.