BURR - BROWN®

OPA121

Low Cost Precision *Difet*® OPERATIONAL AMPLIFIER

FEATURES

- LOW NOISE: 6nV/√Hz typ at 10kHz
- LOW BIAS CURRENT: 5pA max
- LOW OFFSET: 2mV max
- LOW DRIFT: 3µV/°C typ
- HIGH OPEN-LOOP GAIN: 110dB min
- HIGH COMMON-MODE REJECTION: 86dB min

APPLICATIONS

- OPTOELECTRONICS
- DATA ACQUISITION
- TEST EQUIPMENT
- MEDICAL EQUIPMENT
- RADIATION HARD EQUIPMENT

DESCRIPTION

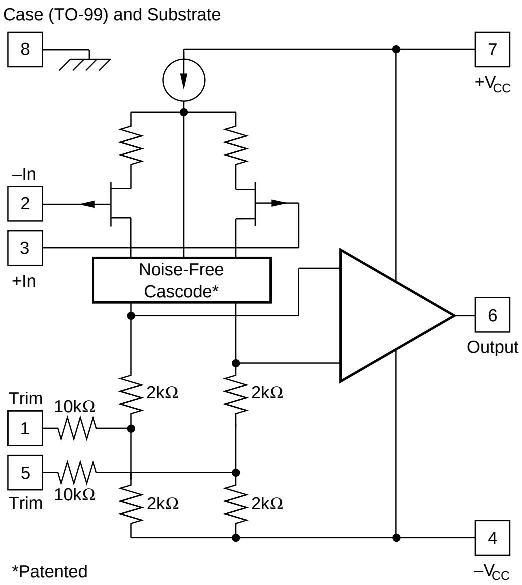
The OPA121 is a precision monolithic dielectrically-isolated FET (***Difet***®) operational amplifier. Outstanding performance characteristics are now available for low-cost applications.

Noise, bias current, voltage offset, drift, open-loop gain, common-mode rejection, and power supply rejection are superior to BIFET® amplifiers.

Very low bias current is obtained by dielectric isolation with on-chip guarding.

Laser-trimming of thin-film resistors gives very low offset and drift. Extremely low noise is achieved with new circuit design techniques (patented). A new cascode design allows high precision input specifications and reduced susceptibility to flicker noise.

Standard 741 pin configuration allows upgrading of existing designs to higher performance levels.



OPA121 Simplified Circuit

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BIFET®, National Semiconductor Corp.

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SPECIFICATIONS

ELECTRICAL

At V_{CC} = ±15VDC and T_A = +25°C unless otherwise noted. Pin 8 connected to ground.

PARAMETER	CONDITIONS	OPA121KM MIN	OPA121KM TYP	OPA121KM MAX	OPA121KP, KU MIN	OPA121KP, KU TYP	OPA121KP, KU MAX	UNITS
INPUT								
NOISE								
Voltage, f_O = 10Hz	(1)		40			50		nV/√Hz
f_O = 100Hz	(1)		15			18		nV/√Hz
f_O = 1kHz	(1)		8			10		nV/√Hz
f_O = 10kHz	(1)		6			7		nV/√Hz
f_B = 10Hz to 10kHz	(1)		0.7			0.8		μVrms
f_B = 0.1Hz to 10 Hz	(1)		1.6			2		μVp-p
Current, f_B = 0.1Hz to 10Hz	(1)		15			21		fA, p-p
f_O = 0.1Hz thru 20kHz	(1)		0.8			1.1		fA/√Hz
OFFSET VOLTAGE(2)								
Input Offset Voltage	V_{CM} = 0VDC		±0.5	±2		±0.5	±3	mV
Average Drift	T_A = T_{MIN} to T_{MAX}		±3	±10		±3	±10	μV/°C
Supply Rejection		86	104		86	104		dB
			±6	±50		±6	±50	μV/V
BIAS CURRENT(2)								
Input Bias Current	V_{CM} = 0VDC Device Operating		±1	±5		±1	±10	pA
OFFSET CURRENT(2)								
Input Offset Current	V_{CM} = 0VDC Device Operating		±0.7	±4		±0.7	±8	pA
IMPEDANCE								
Differential			10^{13} || 1			10^{13} || 1		Ω || pF
Common-Mode			10^{14} || 3			10^{14} || 3		Ω || pF
VOLTAGE RANGE								
Common-Mode Input Range		±10	±11		±10	±11		V
Common-Mode Rejection	V_{IN} = ±10VDC	86	104		82	100		dB
OPEN-LOOP GAIN, DC								
Open-Loop Voltage Gain	R_L ≥ 2kΩ	110	120		106	114		dB
FREQUENCY RESPONSE								
Unity Gain, Small Signal			2			2		MHz
Full Power Response	20Vp-p, R_L = 2kΩ		32			32		kHz
Slew Rate	V_O = ±10V, R_L = 2kΩ		2			2		V/μs
Settling Time, 0.1%	Gain = –1, R_L = 2kΩ		6			6		μs
0.01%	10V Step		10			10		μs
Overload Recovery, 50% Overdrive(3)	Gain = –1		5			5		μs
RATED OUTPUT								
Voltage Output	R_L = 2kΩ	±11	±12		±11	±12		V
Current Output	V_O = ±10VDC	±5.5	±10		±5.5	±10		mA
Output Resistance	DC, Open Loop		100			100		Ω
Load Capacitance Stability	Gain = +1		1000			1000		pF
Short Circuit Current		10	40		10	40		mA
POWER SUPPLY								
Rated Voltage			±15			±15		VDC
Voltage Range, Derated Performance		±5		±18	±5		±18	VDC
Current, Quiescent	I_O = 0mADC		2.5	4		2.5	4.5	mA
TEMPERATURE RANGE								
Specification	Ambient Temperature	0		+70	0		+70	°C
Operating	Ambient Temperature	–40		+85	–25		+85	°C
Storage	Ambient Temperature	–65		+150	–55		+125	°C
θ Junction-Ambient			200			150(4)		°C/W

NOTES: (1) Sample tested. (2) Offset voltage, offset current, and bias current are specified with the units fully warmed up. (3) Overload recovery is defined as the time required for the output to return from saturation to linear operation following the removal of a 50% input overdrive. (4) 100°C/W for KU grade.

ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

At V_{CC} = ±15VDC and T_A = T_{MIN} to T_{MAX} unless otherwise noted.

PARAMETER	CONDITIONS	OPA121KM			OPA121KP, KU			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
TEMPERATURE RANGE								
Specification Range	Ambient Temperature	0		+70	0		+70	°C
INPUT								
OFFSET VOLTAGE(1)								
Input Offset Voltage	V_{CM} = 0VDC		±1	±3		±1	±5	mV
Average Drift			±3	±10		±3	±10	µV/°C
Supply Rejection		82	94		82	94		dB
			±20	±80		±20	±80	µV/V
BIAS CURRENT(1)								
Input Bias Current	V_{CM} = 0VDC Device Operating		±23	±115		±23	±250	pA
OFFSET CURRENT(1)								
Input Offset Current	V_{CM} = 0VDC Device Operating		±16	±100		±16	±200	pA
VOLTAGE RANGE								
Common-Mode Input Range		±10	±11		±10	±11		V
Common-Mode Rejection	V_{IN} = ±10VDC	82	98		80	96		dB
OPEN-LOOP GAIN, DC								
Open-Loop Voltage Gain	R_L ≥ 2kΩ	106	116		100	110		dB
RATED OUTPUT								
Voltage Output	R_L = 2kΩ	±10.5	±11		±10.5	±11		V
Current Output	V_O = ±10VDC	±5.25	±10		±5.25	±10		mA
Short Circuit Current	V_O = 0VDC	10	40		10	40		mA
POWER SUPPLY								
Current, Quiescent	I_O = 0mADC		2.5	4.5		2.5	5	mA

NOTE: (1) Offset voltage, offset current, and bias current are measured with the units fully warmed up.

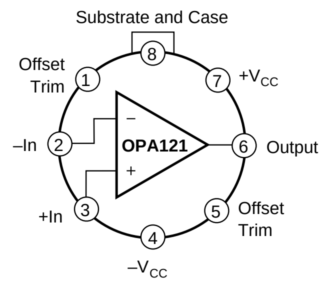
ABSOLUTE MAXIMUM RATINGS

Supply .... ±18VDC
Internal Power Dissipation(1) 500mW
Differential Input Voltage .... ±36VDC
Input Voltage Range .... ±18VDC
Storage Temperature Range
  M package .... –65°C to +150°C
  P, U packages .... –55°C to +125°C
Operating Temperature Range
  M package .... –40°C to +85°C
  P, U packages .... –25°C to +85°C
Lead Temperature
  M, P packages (soldering, 10s) .... +300°C
  U package (soldering, 3s) .... +260°C
Output Short-Circuit Duration(2) .... Continuous
Junction Temperature .... +175°C

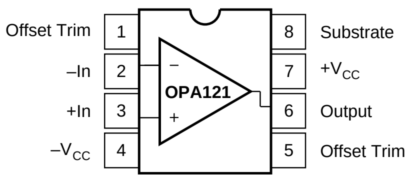
NOTES: (1) Packages must be derated based on θ_{JA} = 150°C/W (P package); θ_{JA} = 200°C/W (M package); θ_{JA} = 100°C/W (U package). (2) Short circuit may be to power supply common only. Rating applies to +25°C ambient. Observe dissipation limit and T_J.

CONNECTION DIAGRAMS

Top View **M-Package** TO-99 (Hermetic)



Top View **P-Package** Plastic Mini-DIP
U-Package Plastic SOIC



PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
OPA121KM	TO-99	001
OPA121KP	8-Pin Plastic DIP	006
OPA121KU	8-Pin SOIC	182

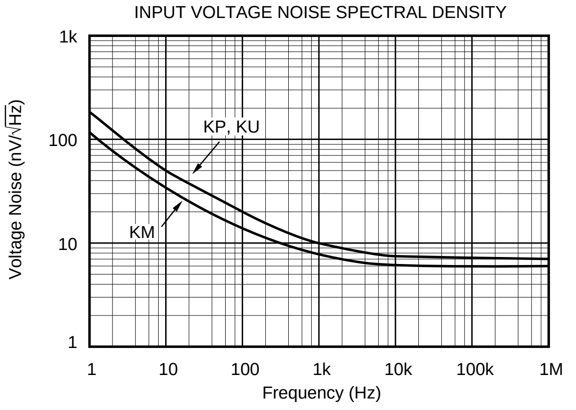
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

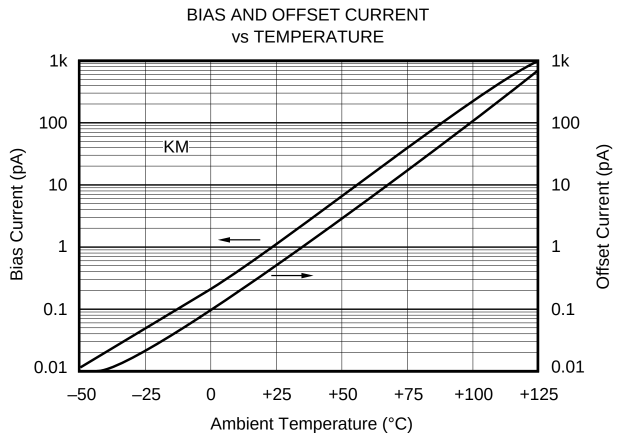
ORDERING INFORMATION

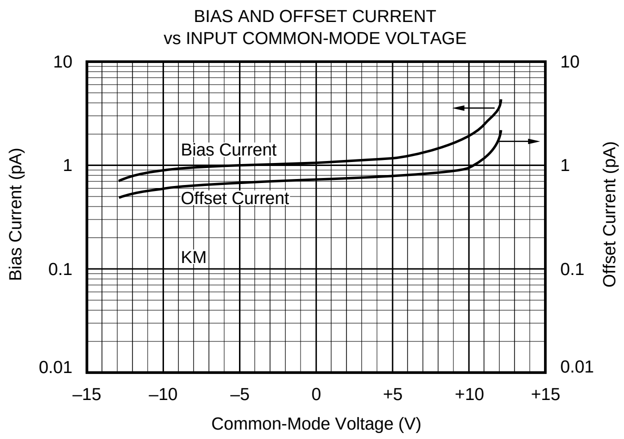
MODEL	PACKAGE	TEMPERATURE RANGE
OPA121KM	TO-99	0°C to +70°C
OPA121KP	8-Pin Plastic DIP	0°C to +70°C
OPA121KU	8-Pin SOIC	0°C to +70°C

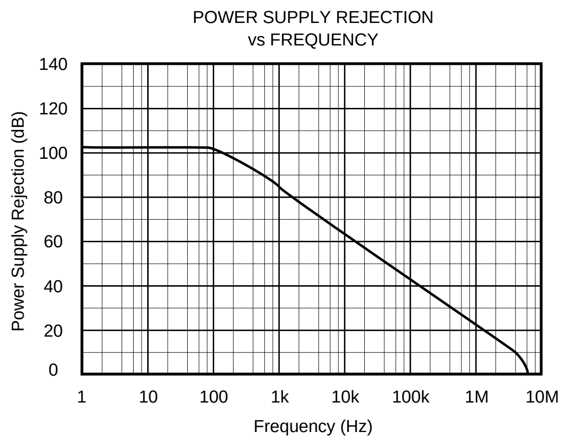
TYPICAL PERFORMANCE CURVES

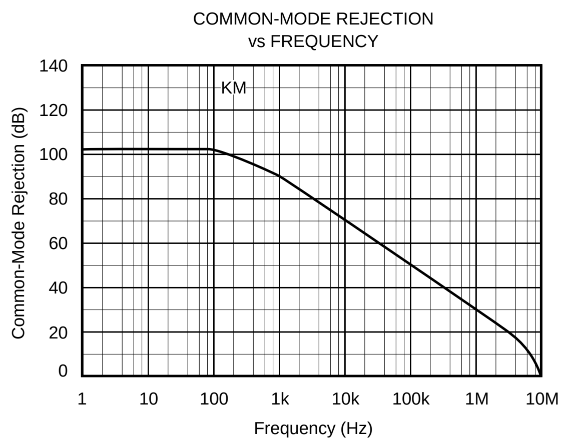
T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted.

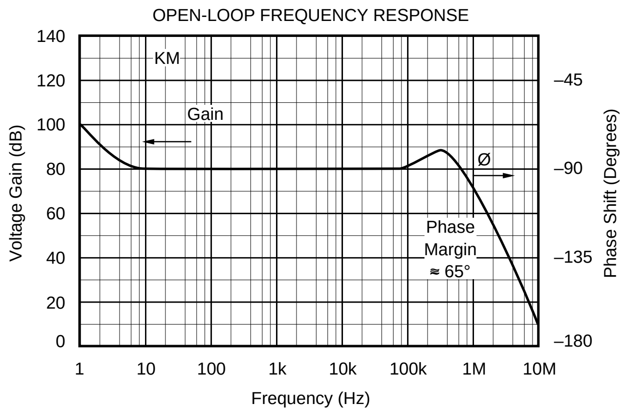






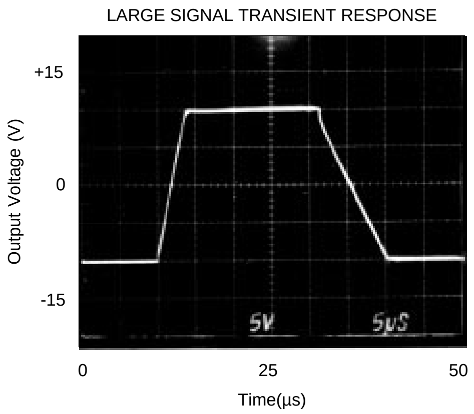


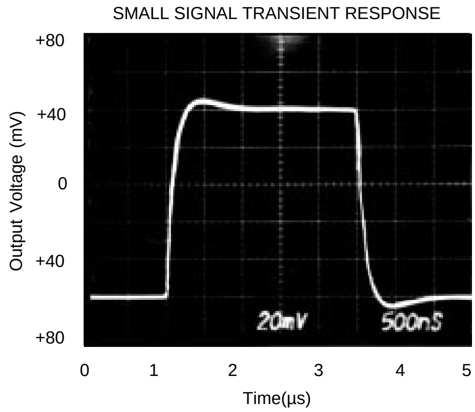


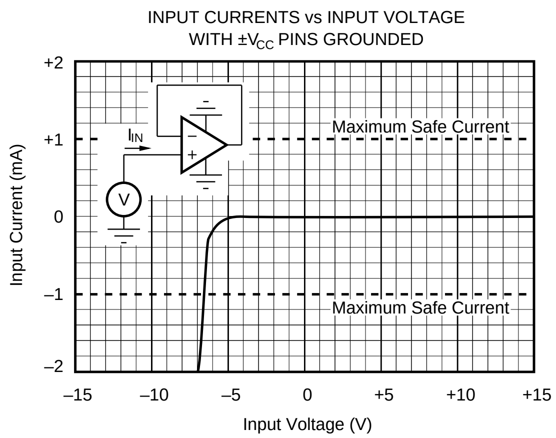


TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted.







APPLICATIONS INFORMATION

OFFSET VOLTAGE ADJUSTMENT

The OPA121 offset voltage is laser-trimmed and will require no further trim for most applications. As with most amplifiers, externally trimming the remaining offset can change drift performance by about 0.3µV/°C for each 100µV of adjusted offset. Note that the trim (Figure 1) is similar to operational amplifiers such as 741 and AD547. The OPA121 can replace most BIFET amplifiers by leaving the external null circuit unconnected.

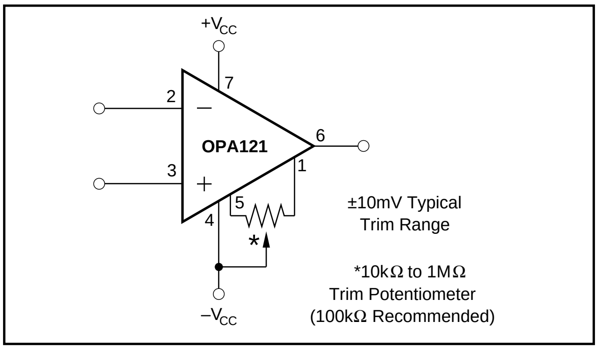


FIGURE 1. Offset Voltage Trim.

INPUT PROTECTION

Conventional monolithic FET operational amplifiers require external current-limiting resistors to protect their inputs against destructive currents that can flow when input FET gate-to-substrate isolation diodes are forward-biased. Most BIFET amplifiers can be destroyed by the loss of $-V_{CC}$.

Unlike BIFET amplifiers, the ***Difet*** OPA121 requires input current limiting resistors only if its input voltage is greater than 6V more negative than $-V_{CC}$. A 10kΩ series resistor will limit input current to a safe level with up to ±15V input levels even if both supply voltages are lost.

Static damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers (both bipolar and FET types), this may cause a noticeable degradation of offset voltage and drift.

Static protection is recommended when handling any precision IC operational amplifier.

GUARDING AND SHIELDING

As in any situation where high impedances are involved, careful shielding is required to reduce "hum" pickup in input leads. If large feedback resistors are used, they should also be shielded along with the external input circuitry.

Leakage currents across printed circuit boards can easily exceed the bias current of the OPA121. To avoid leakage problems, it is recommended that the signal input lead of the OPA121 be wired to a Teflon™ standoff. If the OPA121 is to be soldered directly into a printed circuit board, utmost care must be used in planning the board layout. A "guard" pattern should completely surround the high-impedance input leads and should be connected to a low-impedance point which is at the signal input potential.

The amplifier case should be connected to any input shield or guard via pin 8. This insures that the amplifier itself is fully surrounded by guard potential, minimizing both leakage and noise pickup (see Figure #2).

If guarding is not required, pin 8 (case) should be connected to ground.

BIAS CURRENT CHANGE VERSUS COMMON-MODE VOLTAGE

The input bias currents of most popular BIFET operational amplifiers are affected by common-mode voltage (Figure 3). Higher input FET gate-to-drain voltage causes leakage and ionization (bias) currents to increase. Due to its cascode input stage, the extremely-low bias current of the OPA121 is not compromised by common-mode voltage.

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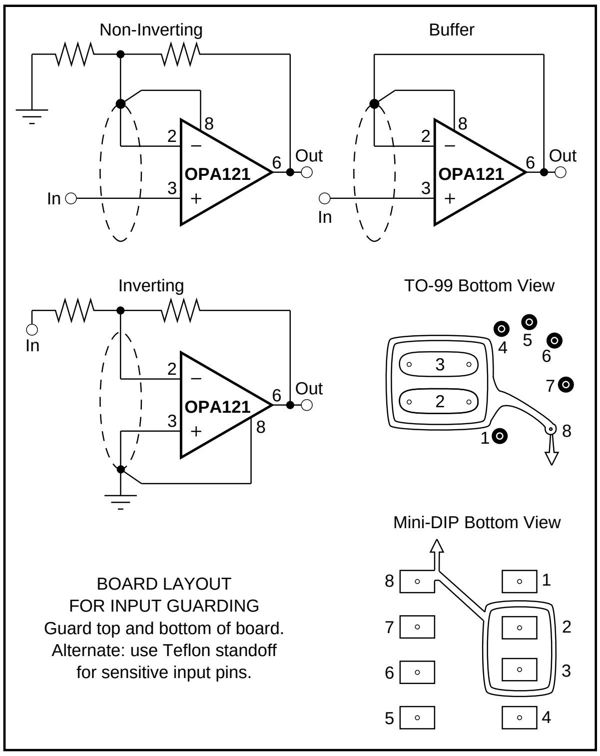

FIGURE 2. Connection of Input Guard.

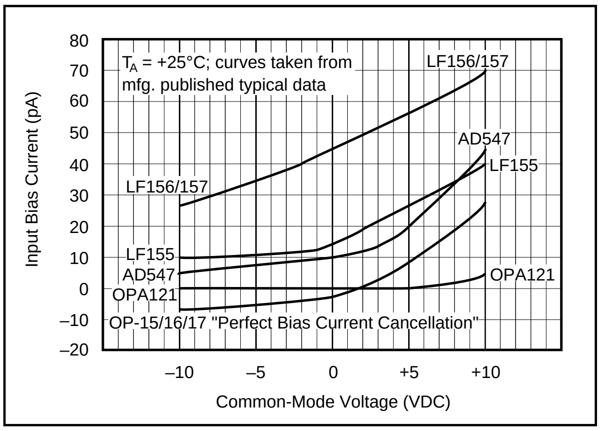

FIGURE 3. Input Bias Current vs Common-Mode Voltage.