

OPA651

Wideband, Low Power Voltage Feedback OPERATIONAL AMPLIFIER

FEATURES

- STABLE IN GAINS: $\geq 2V/V$
- LOW POWER: 50mW
- BANDWIDTH: 470MHz at $G = 2$
- FAST SETTLING TIME: 16ns to 0.01%
- LOW HARMONICS: -78dB at 5MHz
- LOW INPUT BIAS CURRENT: $4\mu\text{A}$
- DIFFERENTIAL GAIN/PHASE ERROR: $0.01\%/0.025^\circ$
- LOW VOLTAGE NOISE: $4.6\text{nV}/\sqrt{\text{Hz}}$

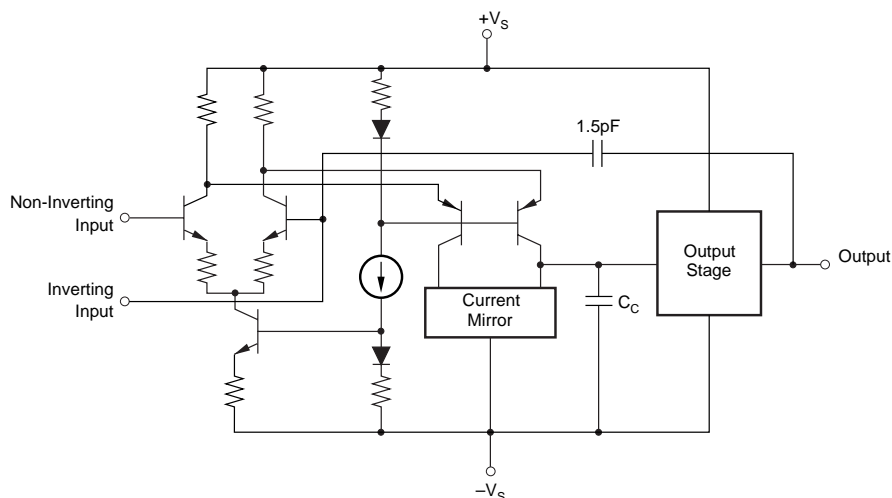
APPLICATIONS

- HIGH RESOLUTION VIDEO
- MONITOR PREAMPLIFIER
- CCD IMAGING AMPLIFIER
- ULTRASOUND SIGNAL PROCESSING
- ADC/DAC GAIN AMPLIFIER
- BASEBAND SIGNAL PROCESSING

DESCRIPTION

The OPA651 is a low power, wideband voltage feedback operational amplifier. It features a bandwidth at $G = +2$ of 470MHz as well as a 12-bit settling time of only 16ns. The wide bandwidth and true differential input stage make it suitable for use in a variety of applications. Its low distortion gives exceptional performance for telecommunications, medical imaging and video applications.

The OPA651 is compensated for stability in gains of two or more, differentiating it from the unity gain stable OPA650. Its unusual combination of speed, accuracy and low power make it an outstanding choice for many portable, multi-channel and other high speed applications, where power is at a premium.



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SPECIFICATIONS

At $T_A = +25^\circ\text{C}$, $V_S = \pm 5\text{V}$, $R_L = 100\Omega$, $R_{FB} = 402\Omega$, $G = +2$, unless otherwise noted.

PARAMETER	CONDITIONS	OPA651U, N			OPA651UB, NB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
FREQUENCY RESPONSE Closed-Loop Bandwidth ⁽²⁾	$G = +2$ $G = +5$ $G = +10$		470 70 34			*(1) * *		MHz MHz MHz
Gain Bandwidth Product			340			*		MHz
Slew Rate	$G = +2$, $V_O = 2\text{V}$ step		300			*		V/ μs
Over Specified Temperature			275			*		V/ μs
Rise Time	0.2V Step		0.8			*		ns
Fall Time	0.2V Step		0.8			*		ns
Settling Time 0.01%	$G = +2$, $V_O = 2\text{V}$ step		16.2			*		ns
0.1%	$G = +2$, $V_O = 2\text{V}$ step		11.5			*		ns
1%	$G = +2$, $V_O = 2\text{V}$ step		7.2			*		ns
Spurious Free Dynamic Range	$G = +2$, $f = 5.0\text{MHz}$, $V_O = 2\text{Vp-p}$, $R_L = 100\Omega$ $R_L = 400\Omega$		67 78			* *		dBc dBc
Differential Gain	$G = +2$, NTSC, $V_O = 1.4\text{Vp}$, $R_L = 150\Omega$		0.01			*		%
Differential Phase	$G = +2$, NTSC, $V_O = 1.4\text{Vp}$, $R_L = 150\Omega$		0.025			*		Degrees
Bandwidth For 0.1dB Flatness	$G = +2$		43			*		MHz
INPUT OFFSET VOLTAGE Input Offset Voltage			± 1	± 5.0		*	± 2.0	mV
Average Drift			± 3			*		$\mu\text{V}/^\circ\text{C}$
Power Supply Rejection ($+V_S$)	$V_S = \pm 4.5\text{V}$ to $\pm 5.5\text{V}$	65	85		70	*		dB
($-V_S$)		52	60		55	*		dB
INPUT BIAS CURRENT Input Bias Current	$V_{CM} = 0\text{V}$		4	20		*	10	μA
Over Temperature			6	30		*	20	μA
Input Offset Current	$V_{CM} = 0\text{V}$		0.4	1.5		*	*	μA
Over Temperature			0.9	3.0		*	*	μA
INPUT NOISE Input Voltage Noise								
Noise Density, $f = 100\text{Hz}$			13			*		$\text{nV}/\sqrt{\text{Hz}}$
$f = 10\text{kHz}$			4.6			*		$\text{nV}/\sqrt{\text{Hz}}$
$f = 1\text{MHz}$			4.6			*		$\text{nV}/\sqrt{\text{Hz}}$
Voltage Noise, BW = 10Hz to 100MHz			46			*		μVrms
Input Bias Current Noise								
Current Noise Density, $f = 0.1\text{Hz}$ to 20kHz			1.1			*		$\text{pA}/\sqrt{\text{Hz}}$
Noise Figure (NF)	$R_S = 10\text{k}\Omega$ $R_S = 50\Omega$		3.2 14			* *		dB dB
INPUT VOLTAGE RANGE Common-Mode Input Range			± 3.0	± 3.5		*	*	V
Over Specified Temperature			75	90	80	*		V
Common-Mode Rejection	$V_{CM} = \pm 0.5\text{V}$							dB
INPUT IMPEDANCE Differential			60 1			*		$\text{k}\Omega$ pF
Common-Mode			2.6 1			*		$\text{M}\Omega$ pF
OPEN-LOOP GAIN Open-Loop Voltage Gain	$V_O = \pm 2\text{V}$, $R_L = 100\Omega$	42	50		45	*		dB
Over Specified Temperature	$V_O = \pm 2\text{V}$, $R_L = 100\Omega$	40			42			dB
OUTPUT Voltage Output			± 2.2	± 3.0		± 2.4	*	V
Over Specified Temperature	No Load $R_L = 250\Omega$		± 2.2	± 2.5		± 2.4	*	V
	$R_L = 100\Omega$		± 2.0	± 2.3		± 2.1	*	V
Current Output, Sourcing		75	110		*	*		mA
Over Specified Temperature		65			*	*		mA
Current Output, Sinking		65	85		*	*		mA
Over Specified Temperature		35			*	*		mA
Short Circuit Current			150			*		mA
Output Resistance	0.1MHz, $G = +2$		0.05			*		Ω
POWER SUPPLY Specified Operating Voltage		± 4.5	± 5	± 5.5	*	*	*	V
Operating Voltage Range			± 5.1	± 7.75		*	± 6.5	V
Quiescent Current				± 8.75			± 7.5	mA
Over Specified Temperature								mA
TEMPERATURE RANGE Specification: U, N, UB, NB		-40		+85	*		*	$^\circ\text{C}$
Thermal Resistance, θ_{JA}			125			*		$^\circ\text{C}/\text{W}$
U SO-8			150			*		$^\circ\text{C}/\text{W}$
N SOT23-5						*		$^\circ\text{C}/\text{W}$

NOTES: (1) An asterisk (*) specifies the same value as the grade to the left. (2) Frequency response can be strongly influenced by PC board parasitics. The OPA651 is nominally compensated assuming 2pF parasitic load. The demonstration boards show low parasitic layouts for the different package styles.

ABSOLUTE MAXIMUM RATINGS

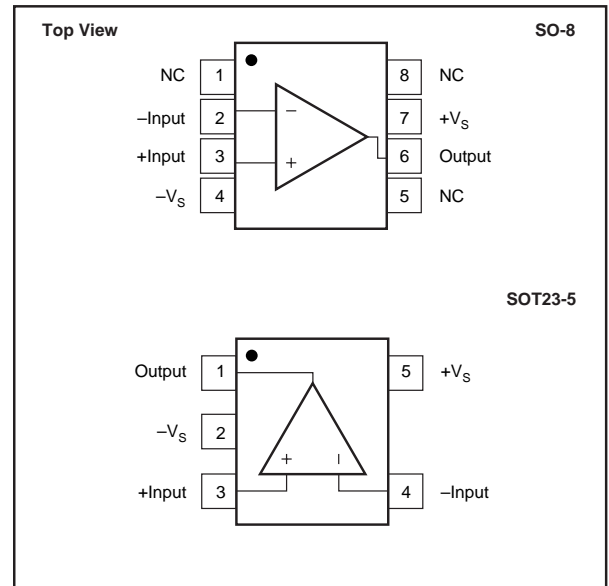
Supply	$\pm 5.5V$
Internal Power Dissipation ⁽¹⁾ :	See Thermal Conditions
Differential Input Voltage	$\pm 1.2V$
Input Voltage Range	$\pm V_S$
Storage Temperature Range: U, UB, N, NB	$-40^{\circ}C$ to $+125^{\circ}C$
Lead Temperature (soldering, 10s)	$+300^{\circ}C$
(soldering, SO-8 3s)	$+260^{\circ}C$
Junction Temperature (T_J)	$+175^{\circ}C$

ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

PIN CONFIGURATION



PACKAGE/ORDERING INFORMATION

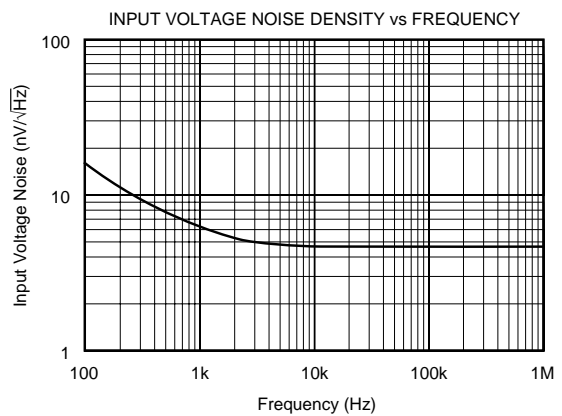
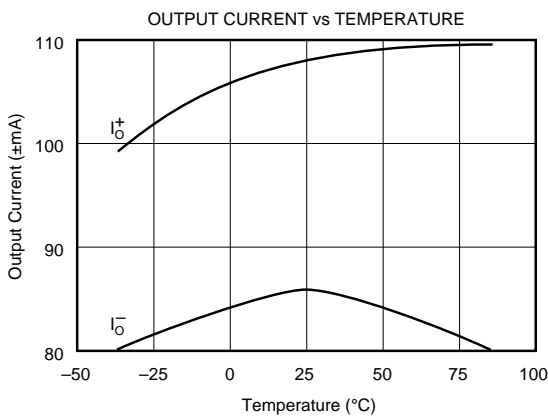
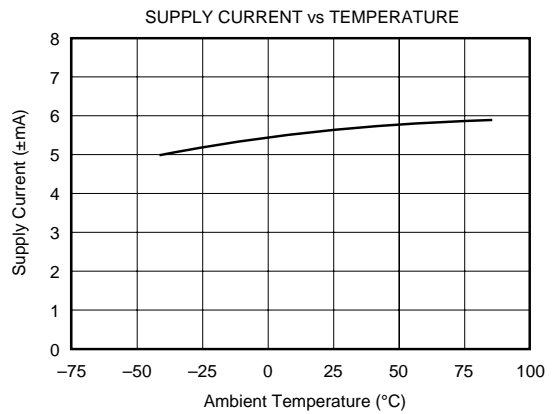
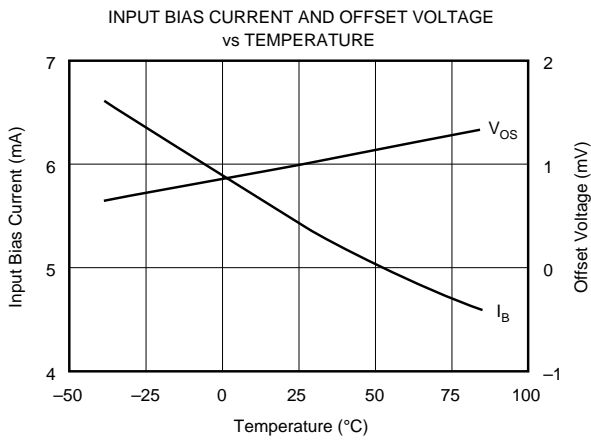
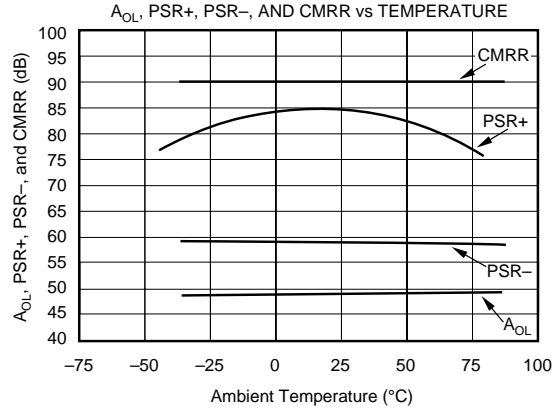
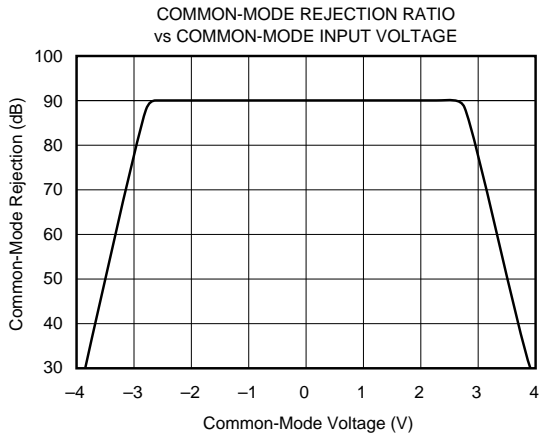
PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER ⁽¹⁾	TEMPERATURE RANGE	PACKAGE MARKING ⁽²⁾	ORDERING NUMBER ⁽³⁾
OPA651U	SO-8 Surface Mount	182	$-40^{\circ}C$ to $+85^{\circ}C$	OPA651U	OPA651U
OPA651UB	SO-8 Surface Mount	182	$-40^{\circ}C$ to $+85^{\circ}C$	OPA651UB	OPA651UB
OPA651N	5-pin SOT23-5	331	$-40^{\circ}C$ to $+85^{\circ}C$	A51	OPA651N-250 OPA651N-3k
OPA651NB	5-pin SOT23-5	331	$-40^{\circ}C$ to $+85^{\circ}C$	A51B	OPA651NB-250 OPA651NB-3k

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book. (2) The "B" grade of the SO-8 package will be marked with a "B" by pin 8. The "B" grade of the SOT23-5 will be marked with a "B" near pins 3 and 4. (3) The SOT23-5 is only available on a 7" tape and reel (e.g. ordering 250 pieces of "OPA651N-250" will get a single 250 piece tape and reel. Ordering 3000 pieces of "OPA651N-3k" will get a single 3000 piece tape and reel). Please refer to Appendix B of Burr-Brown IC Data Book for detailed Tape and Reel Mechanical information.

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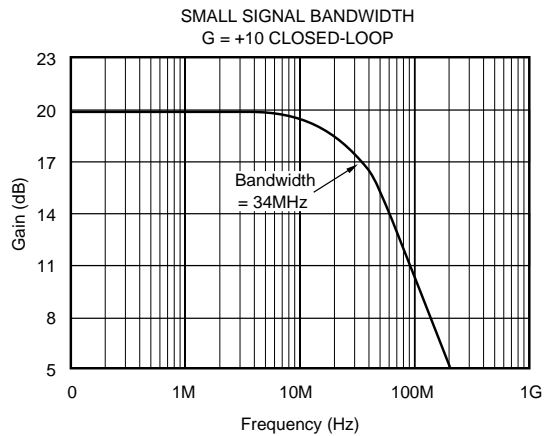
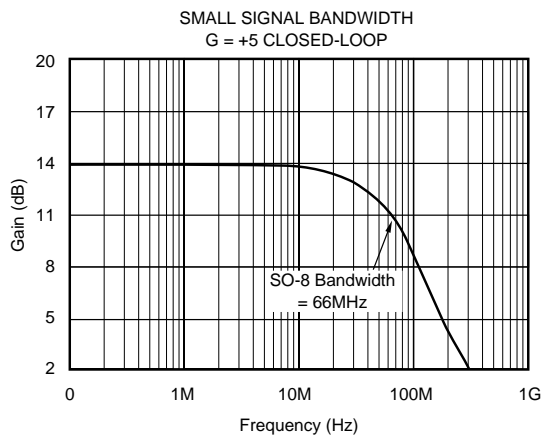
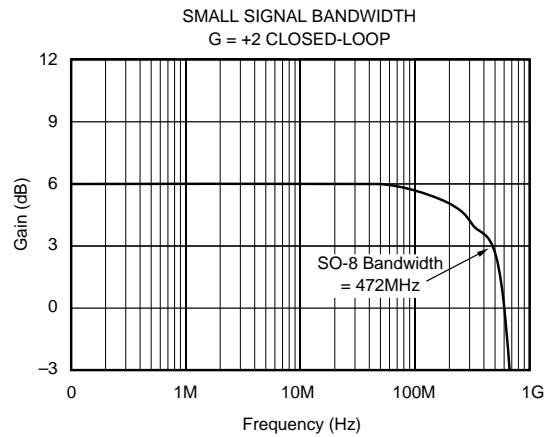
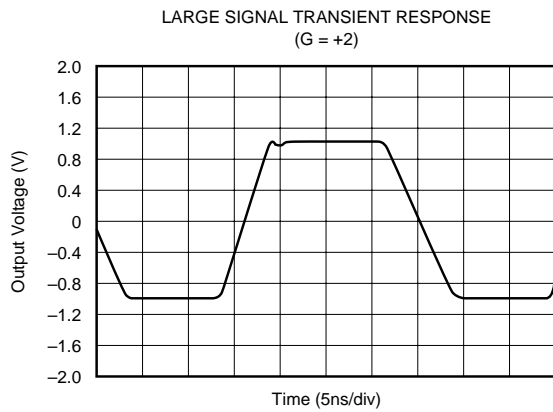
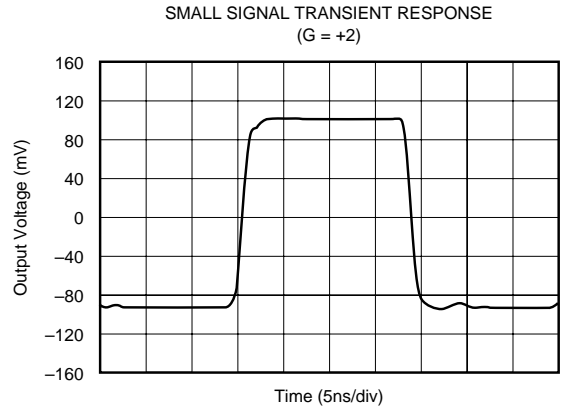
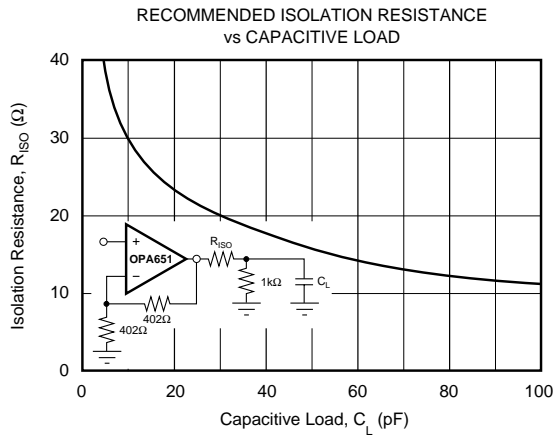
TYPICAL PERFORMANCE CURVES

At $T_A = +25^\circ\text{C}$, $V_S = \pm 5\text{V}$, $R_L = 100\Omega$, $R_{FB} = 402\Omega$, and $G = +2$, unless otherwise noted.



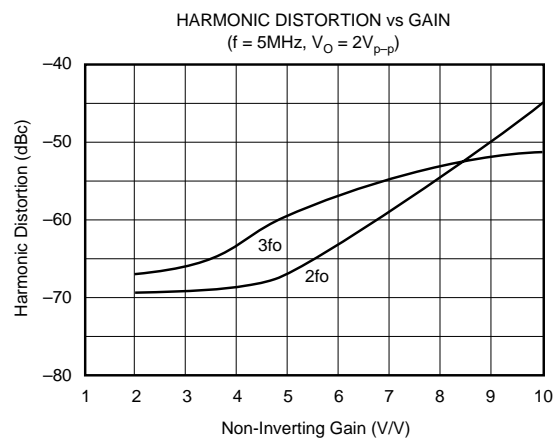
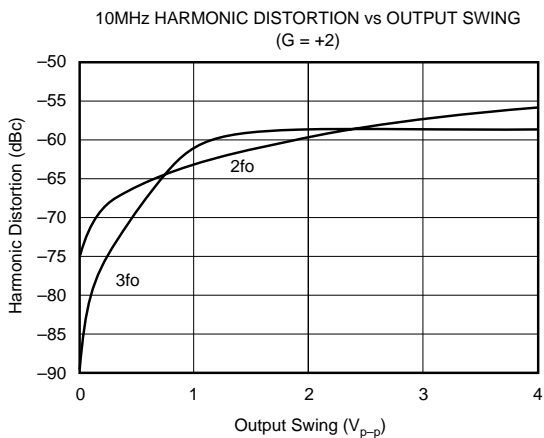
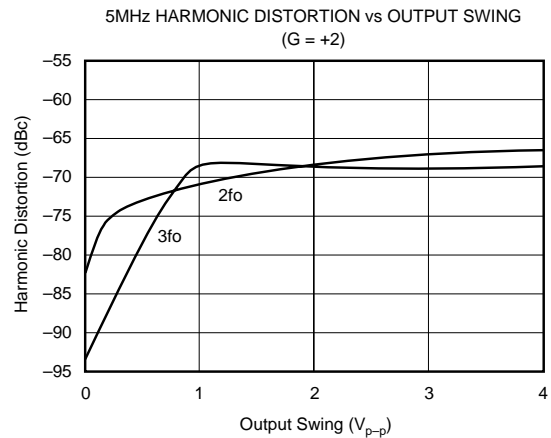
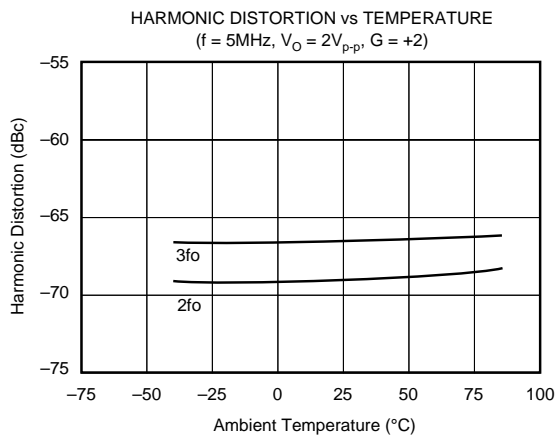
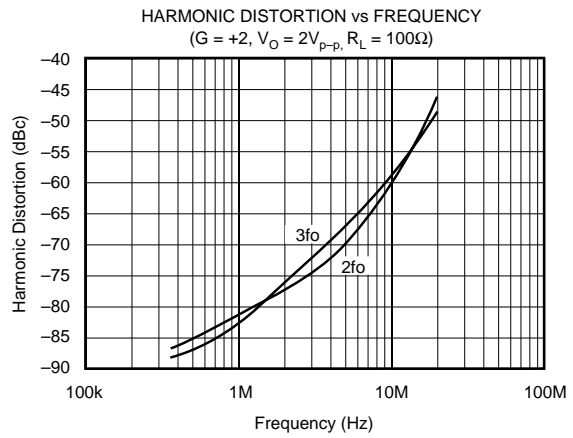
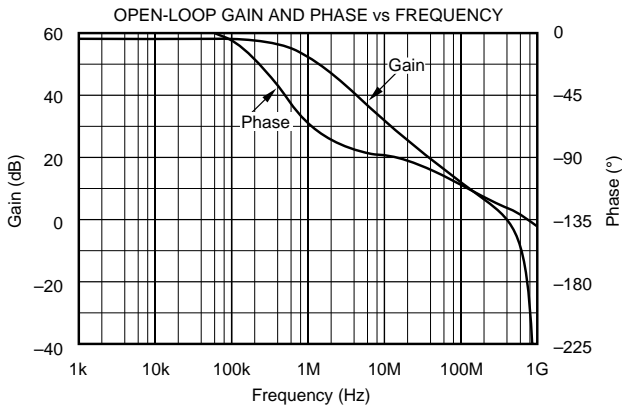
TYPICAL PERFORMANCE CURVES (CONT)

At $T_A = +25^\circ\text{C}$, $V_S = \pm 5\text{V}$, $R_L = 100\Omega$, $R_{FB} = 402\Omega$, and $G = +2$, unless otherwise noted.



TYPICAL PERFORMANCE CURVES (CONT)

At $T_A = +25^\circ\text{C}$, $V_S = \pm 5\text{V}$, $R_L = 100\Omega$, $R_{FB} = 402\Omega$, and $G = +2$, unless otherwise noted.



DISCUSSION OF PERFORMANCE

The OPA651 is a low power, wideband voltage feedback operational amplifier, internally compensated to provide gain of +2 stability. The OPA651's voltage feedback architecture features true differential and fully symmetrical inputs. This minimizes offset errors, making the OPA651 well suited for implementing filter and instrumentation designs. The OPA651's AC performance is optimized to provide a gain bandwidth product of 340MHz and a fast 0.1% settling time of 11.5ns, which is an important consideration in high speed data conversion applications. Along with its excellent settling characteristics, the low DC input offset of $\pm 1\text{mV}$ and drift of $\pm 3\mu\text{V}/^\circ\text{C}$ support high accuracy requirements. In applications requiring a higher slew rate and wider bandwidth, such as video and high bit rate digital communications, consider the current feedback OPA658.

CIRCUIT LAYOUT AND BASIC OPERATION

Achieving optimum performance with a high frequency amplifier like the OPA651 requires careful attention to layout parasitics and selection of external components. Recommendations for PC board layout and component selection include:

a) Minimize parasitic capacitance to any ac ground for all of the signal I/O pins. Parasitic capacitance on the output and inverting input pins can cause instability; on the non-inverting input it can react with the source impedance to cause unintentional bandlimiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes. Otherwise, ground and power planes should be unbroken elsewhere on the board.

b) Minimize the distance ($< 0.25''$) from the two power pins to high frequency $0.1\mu\text{F}$ decoupling capacitors. At the pins, the ground and power plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. Larger ($2.2\mu\text{F}$ to $6.8\mu\text{F}$) decoupling capacitors, effective at lower frequencies, should also be used. These may be placed somewhat farther from the device and may be shared among several devices in the same area of the PC board.

c) Careful selection and placement of external components will preserve the high frequency performance of the OPA651. Resistors should be a very low reactance type. Surface mount resistors work best and allow a tighter overall layout. Metal film or carbon composition axially-leaded resistors can also provide good high frequency performance. Again, keep their leads as short as possible. Never use wirewound type resistors in a high frequency application.

Since the output pin and the inverting input pin are most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close as possible to the package pins. Other network components, such as non-inverting input termination resistors, should also be placed close to the package.

Even with a low parasitic capacitance shunting external resistors, excessively high resistor values can create significant time constants and degrade performance. This is particularly true for the OPA651 with its internal 1.5pF feedback capacitance. Good metal film or surface mount resistors have approximately 0.2pF in shunt with the resistor. For resistor values $> 1.5\text{k}\Omega$, this adds a pole and/or zero below 500MHz that can affect circuit operation. Keep resistor values as low as possible consistent with output loading considerations. The 402Ω feedback used for the Typical Performance Plots is a good starting point for design.

d) Connections to other wideband devices on the board may be made with short direct traces or through on-board transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50 to 100 mils) should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set R_{ISO} from the plot of recommended R_{ISO} vs capacitive load. Low parasitic loads may not need an R_{ISO} since the OPA651 is nominally compensated to operate with a 2pF parasitic load.

If a long trace is required and the 6dB signal loss intrinsic to doubly terminated transmission lines is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50Ω environment is not necessary on board, and in fact a higher impedance environment will improve distortion as shown in the distortion vs load plot. With a characteristic impedance defined based on board material and desired trace dimensions, a matching series resistor into the trace from the output of the amplifier is used as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance will be the parallel combination of the shunt resistor and the input impedance of the destination device; the total effective impedance should match the trace impedance. Multiple destination devices are best handled as separate transmission lines, each with their own series and shunt terminations.

If the 6dB attenuation loss of a doubly terminated line is unacceptable, a long trace can be series-terminated at the source end only. This will help isolate the line capacitance from the op amp output, but will not preserve signal integrity as well as a doubly terminated line. If the shunt impedance at the destination end is finite, there will be some signal attenuation due to the voltage divider formed by the series and shunt impedances.

The OPA651 is nominally specified for operation using $\pm 5\text{V}$ power supplies. A 10% tolerance on the supplies, or an ECL -5.2V for the negative supply, is within the maximum specified total supply voltage of 11V . Higher supply voltages can break down internal junctions possibly leading to catastrophic failure. Single supply operation is possible as long as common mode voltage constraints are observed. The common

mode input and output voltage specifications can be interpreted as a required headroom to the supply voltage. Observing this input and output headroom requirement will allow non-standard or single supply operation. Figure 1 shows one approach to single-supply operation.

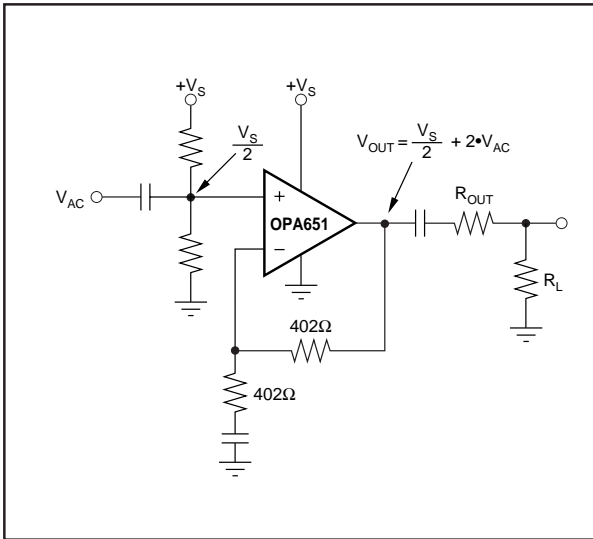


FIGURE 1. Single Supply Operation.

OFFSET VOLTAGE ADJUSTMENT

If additional offset adjustment is needed, the circuit in Figure 2 can be used without degrading offset drift with temperature. Avoid external adjustment whenever possible since extraneous noise, such as power supply noise, can be inadvertently coupled into the amplifier's inverting input terminal. Remember that additional offset errors can be created by the amplifier's input bias currents. Whenever possible, match the impedance seen by both inputs as is shown with R_3 . This will reduce input bias current errors to the amplifier's offset current.

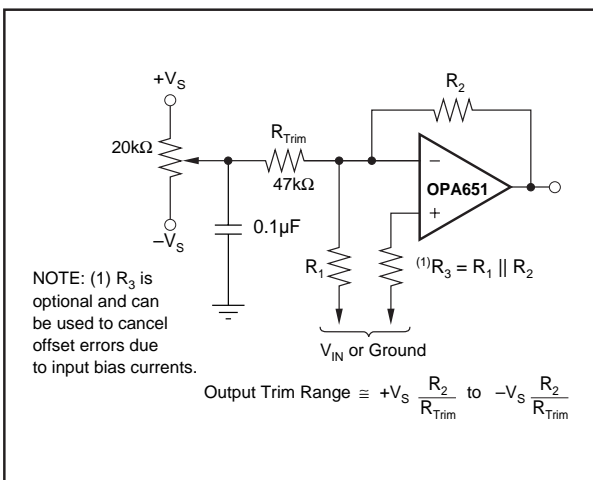


FIGURE 2. Offset Voltage Trim.

ESD PROTECTION

ESD damage has been well recognized for MOSFET devices, but any semiconductor device is vulnerable to this potentially damaging source. This is particularly true for very high speed, fine geometry processes.

ESD damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers, this may cause a noticeable degradation of offset voltage and drift. Therefore, ESD handling precautions are strongly recommended when handling the OPA651.

OUTPUT DRIVE CAPABILITY

The OPA651 has been optimized to drive 75Ω and 100Ω resistive loads. The device can drive a 2V_{p-p} into a 75Ω load. This high-output drive capability makes the OPA651 an ideal choice for a wide range of RF, IF, and video applications. In many cases, additional buffer amplifiers are unneeded.

Many demanding high-speed applications such as driving A/D converters require op amps with low wideband output impedance. For example, low output impedance is essential when driving the signal-dependent capacitances at the inputs of flash A/D converters. As shown in Figure 3, the OPA651 maintains very low-closed loop output impedance over frequency. Closed-loop output impedance increases with frequency since loop gain is decreasing.

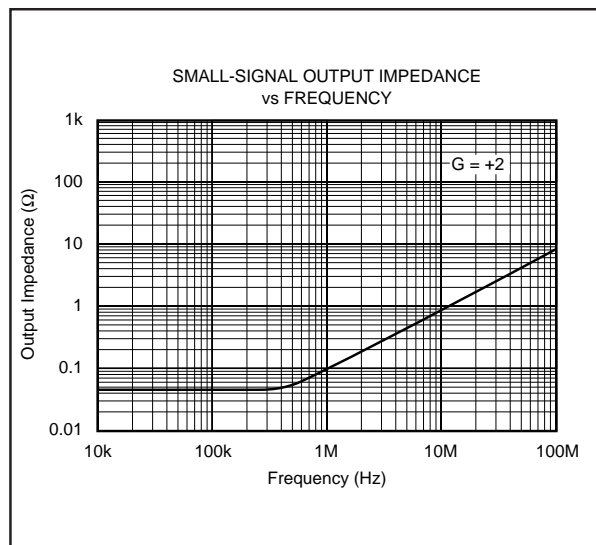


FIGURE 3. Small-Signal Output Impedance vs Frequency.

THERMAL CONSIDERATIONS

The OPA651 will not require heatsinking under most operating conditions. Maximum desired junction temperature will limit the maximum allowed internal power dissipation as described below. In no case should the maximum junction temperature be allowed to exceed +175°C.

Operating junction temperature (T_J) is given by $T_A + P_D \theta_{JA}$. The total internal power dissipation (P_D) is a combination of the total quiescent power (P_{DQ}) and the power dissipated in of the output stage (P_{DL}) to deliver load power. Quiescent power is simply the specified no-load supply current times the total supply voltage across the part. P_{DL} will depend on the required output signal and load but would, for a grounded resistive load, be at a maximum when the output is a fixed DC voltage equal to 1/2 of either supply voltage (assuming equal bipolar supplies). Under this condition, $P_{DL} = V_S^2 / (4 \cdot R_L)$ where R_L includes feedback network loading. Note that it is the power dissipated in the output stage and not in the load that determines internal power dissipation. As an example, compute the maximum T_J for an OPA651N at $A_V = +2$, $R_L = 100\Omega$, $R_{FB} = 402\Omega$, $\pm V_S = \pm 5V$, with the output at $|V_S/2|$, and the specified maximum $T_A = +85^\circ C$. $P_D = 10V \cdot 8.75mA + (5^2) / (4 \cdot (100\Omega || 804\Omega)) = 158mW$. Maximum $T_J = +85^\circ C + 0.158W \cdot 150^\circ C/W = 109^\circ C$.

DRIVING CAPACITIVE LOADS

The OPA651's output stage has been optimized to drive low resistive loads. Capacitive loads, however, will decrease the amplifier's phase margin which may cause high frequency peaking or oscillations. Capacitive loads greater than 10pF should be isolated by connecting a small resistance, usually 15Ω to 30Ω, in series with the output as shown in Figure 4. This is particularly important when driving high capacitance loads such as flash A/D converters. Increasing the gain from +2 will improve the capacitive load drive due to increased phase margin.

In general, capacitive loads should be minimized for optimum high frequency performance. Coax lines can be driven if the cable is properly terminated. The capacitance of coax cable (29pF/foot for RG-58) will not load the amplifier when the coaxial cable or transmission line is terminated in its characteristic impedance.

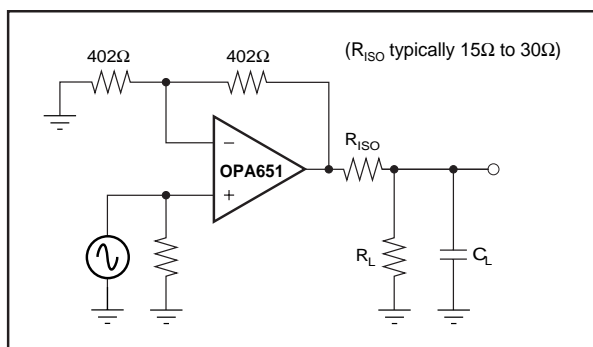


FIGURE 4. Driving Capacitive Loads.

FREQUENCY RESPONSE COMPENSATION

The OPA651 is internally compensated and is stable at a gain of 2 with a phase margin of approximately 60°. (Note

that, from a stability standpoint, an inverting gain of -1V/V is equivalent to a noise gain of 2.) Frequency response for other gains are shown in the Typical Performance Curves.

The high frequency response of the OPA651 in a good layout is very flat with frequency. However, some circuit configurations such as those where large feedback resistances are used, can produce high-frequency gain peaking. This peaking can be minimized by connecting a small capacitor in parallel with the feedback resistor. This capacitor compensates for the closed-loop, high-frequency, transfer function zero that results from the time constant formed by the input capacitance of the amplifier (typically 2pF after PC board mounting), and the input and feedback resistors. The selected compensation capacitor may be a trimmer, a fixed capacitor, or a planned PC board capacitance. The capacitance value is strongly dependent on circuit layout and closed-loop gain. Using small resistor values will preserve the phase margin and avoid peaking by keeping the break frequency of this zero sufficiently high. When high closed-loop gains are required, a three-resistor attenuator (tee-network) is recommended to avoid using large value resistors with large time constants. The OPA651 includes an internal 1.5pF feedback capacitor to achieve best gain of +2 flatness ($R_F = 402\Omega$).

PULSE SETTling TIME

High speed amplifiers like the OPA651 are capable of extremely fast settling time with a pulse input. Excellent frequency response flatness and phase linearity are required to get the best settling times. As shown in the specifications table, settling time for a ±1V step at a gain of +2 for the OPA651 is extremely fast. The specification is defined as the time required, after the input transition, for the output to settle within a specified error band around its final value. For a 2V step, 1% settling corresponds to an error band of ±20mV, 0.1% to an error band of ±2mV, and 0.01% to an error band of ±0.2mV. For the best settling times, particularly into an ADC capacitive load, little or no peaking in the frequency response can be allowed. Using the recommended R_{ISO} for capacitive loads will limit this peaking and reduce the settling times. Fast, extremely fine scale settling (0.01%) requires close attention to ground return currents in the supply decoupling capacitors. For highest performance, consider the OPA642 which isolates the output stage decoupling from the rest of the amplifier.

DIFFERENTIAL GAIN AND PHASE

Differential Gain (DG) and Differential Phase (DP) are among the more important specifications for video applications. The percentage change in closed-loop gain over a specified change in output voltage level is defined as DG. DP is defined as the change in degrees of the closed-loop phase over the same output voltage change. DG and DP are both specified at the NTSC sub-carrier frequency of 3.58MHz. All measurements were performed using an HP 9480.

DISTORTION

The OPA651's harmonic distortion characteristics into a 100Ω load are shown versus frequency and power output in the typical performance curves. Distortion can be significantly improved by increasing the load resistance as illustrated in Figure 5. Remember to include the contribution of the feedback network when calculating the effective load resistance seen by the amplifier.

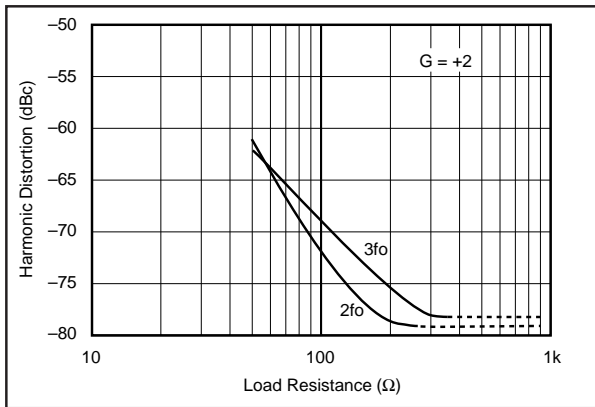


FIGURE 5. 5MHz Harmonic Distortion vs Load Resistance.

NOISE FIGURE

The OPA651 voltage noise spectral density is specified in the Typical Performance Curves. For RF applications, however, Noise Figure (NF) is often the preferred noise specification since it allows system noise performance to be more easily calculated. The OPA651's Noise Figure vs Source Resistance is shown in Figure 6.

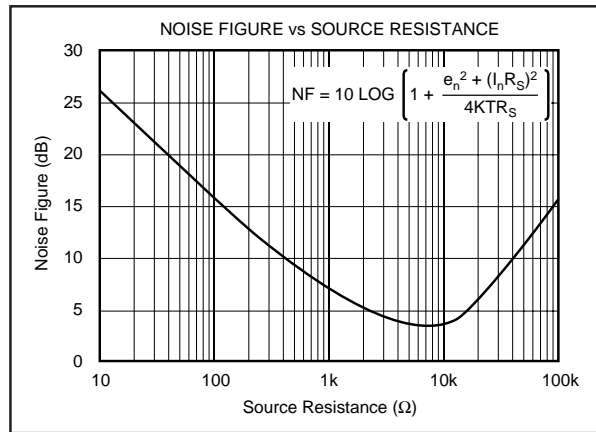


FIGURE 6. Noise Figure vs Source Resistance.

SPICE MODELS AND EVALUATION BOARD

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for Video and RF amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. SPICE models are available on a disk from the Burr-Brown Applications Department.

Demonstration boards are available for each OPA651 package style. These boards implement a very low parasitic layout that will produce the excellent frequency and pulse responses shown in the Typical Performance Curves. For each package style, the recommended demonstration board is:

PRODUCT	PACKAGE	BOARD PART NUMBER	LITERATURE REQUEST NUMBER
OPA651P	8-Pin DIP	DEM-OPA65xP	—
OPA651U	8-Pin SO-8	DEM-OPA65xU	—
OPA651N	6-Pin SOT23-6	DEM-OPA6xxN	MKT-348

Contact your local Burr-Brown sales office or distributor to order demonstration boards.

TYPICAL APPLICATION

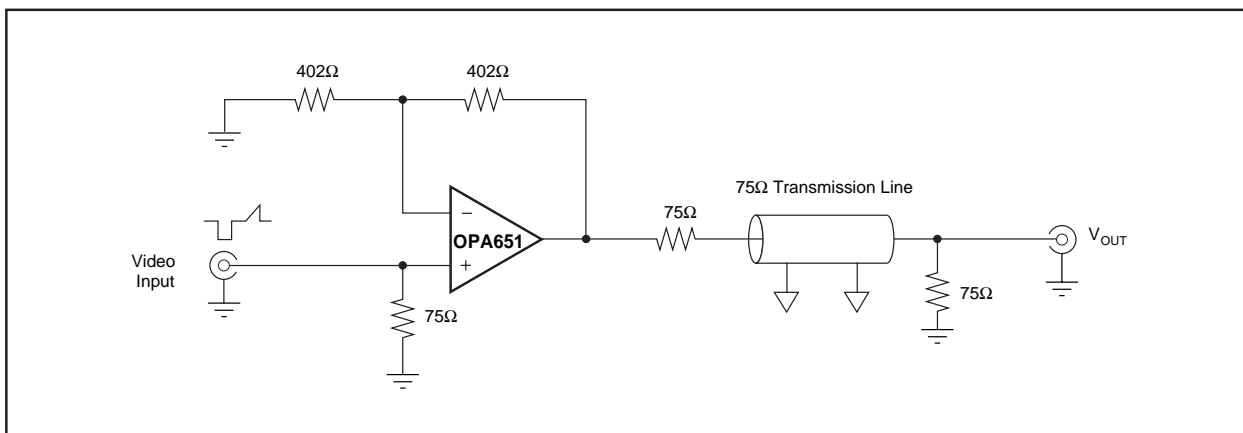


FIGURE 7. Low Distortion Video Amplifier.

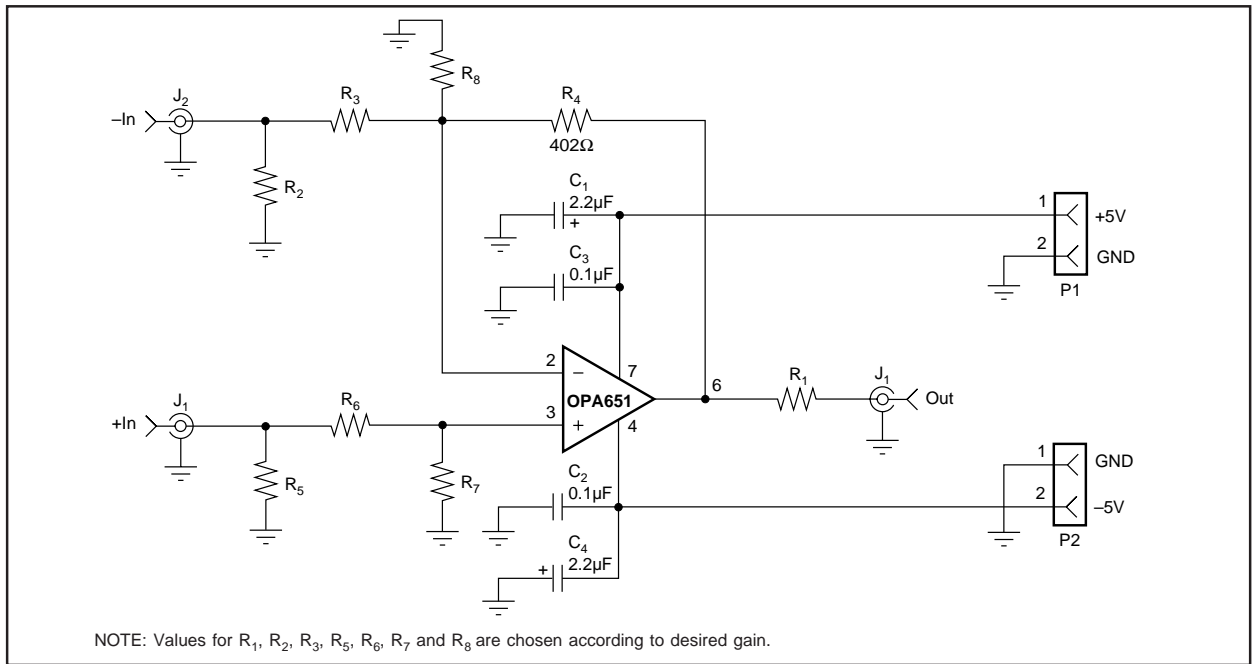


FIGURE 8. Layout Detail For DEM-OPA65xU Demonstration Board.