BURR - BROWN®

PCM1739

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SoundPLUS™ 24-Bit, 192kHz Sampling, Enhanced Multi-Level, Delta-Sigma, Audio DIGITAL-TO-ANALOG CONVERTER

FEATURES

- 24-BIT RESOLUTION
- ANALOG PERFORMANCE (V_{CC} = +5V):
  Dynamic Range: 106dB typ
  SNR: 105dB typ
  THD+N: 0.0015% typ
  Full-Scale Output: 3.1Vp-p typ
- 4x/8x OVERSAMPLING DIGITAL FILTER:
  Passband: 0.454f_S
  Stopband: 0.546f_S
  Stopband Attenuation: –82dB
  Passband Ripple: ±0.002dB
- SAMPLING FREQUENCY: 10kHz to 192kHz
- SYSTEM CLOCK: 128f_S, 192f_S, 256f_S, 384f_S, 512f_S, or 768f_S with Auto Detect
- ACCEPTS 24- or 16-BIT AUDIO DATA
- DATA FORMATS: Standard, I²S
- MODE CONTROLS
  Digital De-Emphasis
  Soft Mute
  Zero Flags for Each Output
- DUAL SUPPLY OPERATION:
  +5V Analog, +3.3V Digital
- 5V TOLERANT DIGITAL INPUTS
- SMALL SSOP-28 PACKAGE

APPLICATIONS

- A/V RECEIVERS
- DVD AUDIO AND MOVIE PLAYERS
- DVD ADD-ON CARDS FOR ENTERTAINMENT PCs
- HDTV RECEIVERS
- CAR AUDIO SYSTEMS
- OTHER APPLICATIONS REQUIRING 24-BIT AUDIO

DESCRIPTION

The PCM1739 is a CMOS, monolithic, integrated circuit which includes stereo 24-bit audio digital-to-analog converters and support circuitry in a small SSOP-28 package. The data converters utilize Burr-Brown's enhanced multi-level delta-sigma architecture, which employs 4th-order noise shaping and 8-level amplitude quantization to achieve excellent dynamic performance and improved tolerance to clock jitter. The PCM1739 accepts industry-standard audio data formats with 16- or 24-bit data, providing easy interfacing to audio DSP and decoder chips. Sampling rates up to 192kHz are supported.

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Twx: 910-952-1111 • Internet: http://www.burr-brown.com/ • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

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SPECIFICATIONS

All specifications at T_A = +25°C, $+V_{CC}$ = +5V, $+V_{DD}$ = +3.3V, system clock = 384f_S (f_S = 44.1kHz) and 24-bit data, unless otherwise noted.

PARAMETER	CONDITIONS	PCM1739E MIN	PCM1739E TYP	PCM1739E MAX	UNITS
RESOLUTION			24		Bits
DATA FORMAT					
Audio Data Interface Formats	User Selectable		Standard/I²S		
Audio Data Bit Length	User Selectable		16 or 24 Bits		
Audio Data Format			MSB-First, Binary Two's Complement		
System Clock Frequency			128, 192, 256, 384, 512, 768f_S		
Sampling Frequency (f_S)		10		200	kHz
DIGITAL INPUT/OUTPUT					
Logic Family			TTL-Compatible		
Input Logic Level					
V_{IH}		2.0			VDC
V_{IL}				0.8	VDC
Input Logic Current					
I_{IH}	$V_{IN} = V_{DD}$			0.1	µA
I_{IL}	V_{IN} = 0V			–0.1	µA
I_{IH}(1)	$V_{IN} = V_{DD}$		65	100	µA
I_{IL}(1)	V_{IN} = 0V			–0.1	µA
Output Logic Level					
V_{OH}(2)	I_{OH} = –2mA	2.4			VDC
V_{OL}(2)	I_{OL} = +2mA			1.0	VDC
V_{OH}(3)	I_{OH} = –4mA	2.4			VDC
V_{OL}(3)	I_{OL} = +4mA			1.0	VDC
DYNAMIC PERFORMANCE(4)					
THD+N, V_{OUT} = 0dB	f_S = 44.1kHz, 384f_S		0.0015	0.0035	%
	f_S = 96kHz, 256f_S		0.0020	0.0050	%
	f_S = 192kHz, 128f_S		0.25	0.0060	%
V_{OUT} = –60dB	f_S = 44.1kHz		0.6	0.8	%
	f_S = 96kHz		0.7	1.0	%
	f_S = 192kHz		0.8	1.2	%
Dynamic Range	EIAJ, A-Weighted, f_S = 44.1kHz	102	106		dB
	A-Weighted, f_S = 96kHz	100	105		dB
	A-Weighted, f_S = 192kHz	98	104		dB
Signal-to-Noise Ratio(5)	EIAJ, A-Weighted, f_S = 44.1kHz	100	105		dB
	A-Weighted, f_S = 96kHz	100	104		dB
	A-Weighted, f_S = 192kHz	100	104		dB
Channel Separation	f_S = 44.1kHz	100	104		dB
	f_S = 96kHz	98	103		dB
	f_S = 192kHz	96	102		dB
DC ACCURACY					
Gain Error			±1.0	±3.0	% of FSR
Gain Mismatch, Channel-to-Channel			±1.0	±3.0	% of FSR
Bipolar Zero Error	$V_{OUT} = 0.5V_{CC}$ at BPZ		±30	±60	mV
ANALOG OUTPUT					
Output Voltage	Full Scale (–0dB)		62% of V_{CC}		Vp-p
Center Voltage			50% of V_{CC}		VDC
Load Impedance	AC Load	5			kΩ
DIGITAL FILTER PERFORMANCE					
Filter Characteristics					
Passband	±0.002dB			0.454f_S	Hz
	–3dB			0.490f_S	Hz
Stopband		0.546fs			Hz
Passband Ripple				±0.002	dB
Stopband Attenuation	Stopband = 0.546f_S	–75			dB
	Stopband = 0.567f_S	–82			dB
Delay Time			34/f_S		sec
De-Emphasis Error			±0.1		dB
ANALOG FILTER PERFORMANCE					
Frequency Response	At 20kHz		–0.03		dB
	At 44kHz		–0.20		dB
Cut-Off Frequency	–3dB		190		kHz

SPECIFICATIONS (cont.)

All specifications at +25°C, $+V_{CC}$ = +5V, $+V_{DD}$ = +3.3V, system clock = $384f_S$ (f_S = 44.1kHz) and 24-bit data, unless otherwise noted.

PARAMETER	CONDITONS	PCM1739E MIN	PCM1739E TYP	PCM1739E MAX	UNITS
POWER SUPPLY REQUIREMENTS					
Voltage Range					
V_{DD}		+3.0	+3.3	+3.6	VDC
V_{CC}		+4.5	+5.0	+5.5	VDC
Supply Current					
I_{DD}(6)	V_{DD} = 3.3V				
	f_S = 44.1 kHz		8.5	12.0	mA
	f_S = 96kHz, $256f_S$		16.5		mA
	f_S = 192kHz, $128f_S$		19.5		mA
I_{CC}	V_{CC} = 5.0V				
	f_S = 44.1kHz		13.0	18.0	mA
	f_S = 96kHz, $256f_S$		14.0		mA
	f_S = 192kHz, $128f_S$		14.5		mA
Power Dissipation	V_{DD} = 3.3V, V_{CC} = 5.0V				
	f_S = 44.1kHz		93	130	mW
	f_S = 96kHz, $256f_S$		124		mW
	f_S = 192kHz, $128f_S$		137		mW
TEMPERATURE RANGE					
Operation		0		70	°C
Storage		–55		+125	°C
Thermal Resistance θ_{JA}			100		°C/W

NOTES: (1) Pins 8, 9, 26, 27, 28 (TEST1, IBIT, DEM0 DEM1, FORM). (2) Pins 23, 24 (ZEROL, ZEROR). (3) Pin 4 (CLKO). (4) Analog performance specs are tested with Shibasoku #725 THD Meter 400Hz HPF, 30kHz LPF on, average mode with 20kHz bandwidth limiting. The load connected to the analog output is 5kΩ or larger, AC-coupled. (5) SNR is tested with Infinite Zero Detection off. (6) CLKO is disabled.

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage, V_{DD}	+4.0V
V_{CC}	+6.5V
Input Current (except power supply pins)	±10mA
Supply Voltage Difference	±0.1V
GND Voltage Difference	±0.1V
Digital Input Voltage	–0.2V to +5.5V
Digital Output Voltage	–0.2V to (V_{DD} + 0.2V)
Power Dissipation	650mW
Operating Temperature Range	0°C to +70°C
Storage Temperature	–55°C to +125°C
Lead Temperature (soldering, 5s)	+260°C
Package Temperature (IR reflow, 10s)	+235°C

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

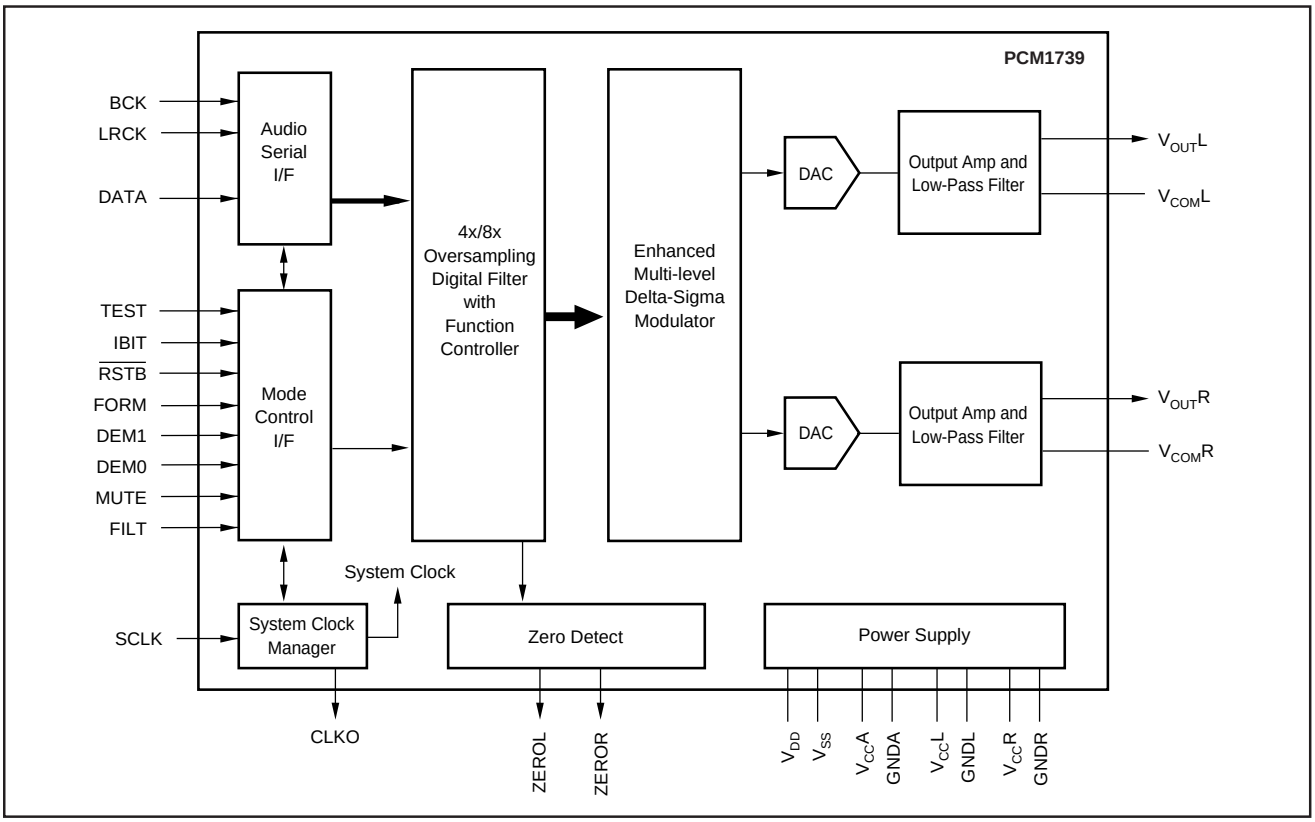
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

PACKAGE	PACKAGE	PACKAGE DRAWING NUMBER	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER(1)	TRANSPORT MEDIA
PCM1739E	28-Lead SSOP	324	0°C to +70°C	PCM1739E	PCM1739E	Rails
"	"	"	"	"	PCM1739E/2K	Tape and Reel

NOTES: (1) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /2K indicates 2000 devices per reel). Ordering 2000 pieces of “PCM1739E/2K” will get a single 2000-piece Tape and Reel.

BLOCK DIAGRAM



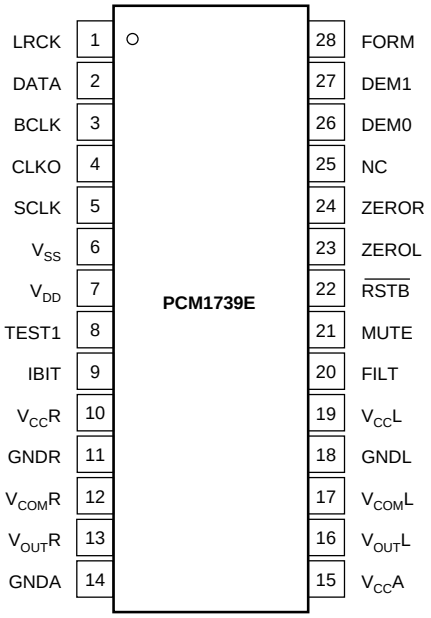
PIN ASSIGNMENTS

PIN	NAME	TYPE	DESCRIPTION
1	LRCK	IN	Left/Right Word Clock(1)
2	DATA	IN	Data In for Left and Right Channels(1)
3	BCLK	IN	Bit Clock(1)
4	CLKO	OUT	System Clock Output
5	SCLK	IN	System Clock Input(1)
6	V_{SS}	—	Digital Ground
7	V_{DD}	—	Digital Supply, +3.3V.
8	TEST1	IN	Test Pin. Must be connected to V_{DD}(2).
9	IBIT	IN	Audio Data Word Length Select(2)
10	$V_{CC}R$	—	Analog Supply for Right Channel, +5V.
11	GNDR	—	Analog Ground for Right Channel
12	$V_{COM}R$	—	Common for Right Channel
13	$V_{OUT}R$	OUT	Analog Output for Right Channel
14	GNDA	—	Analog Ground
15	$V_{CC}A$	—	Analog Supply, +5V.
16	$V_{OUT}L$	OUT	Analog Ouput for Left Channel
17	$V_{COM}L$	—	Common for Left Channel
18	GNDL	—	Analog Ground for Left Channel
19	$V_{CC}L$	—	Analog Supply for Left Channel, +5V.
20	FILT	IN	4x/8x Interpolation Filter Select(2)
21	MUTE	IN	Digital Mute for Left and Right Channels(2)
22	RSTB	IN	Reset, Active Low(1).
23	ZEROL	OUT	Zero Flag for Left Channel
24	ZEROR	OUT	Zero Flag for Right Channel
25	NC	—	No Connect
26	DEM0	IN	De-Emphasis Filter Select 0(2)
27	DEM1	IN	De-Emphasis Filter Select 1(2)
28	FORM	IN	Audio Data Format Select(2)

NOTES: (1) Schmitt-Trigger input with internal pull-down, 5V tolerant.
(2) Schmitt-Trigger input, 5V tolerant.

PIN CONFIGURATION

Top View **SSOP**

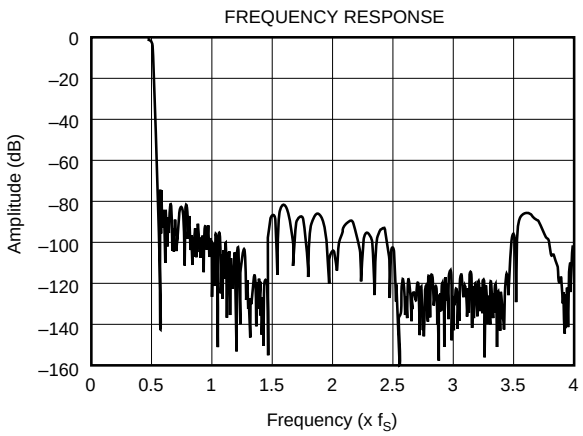


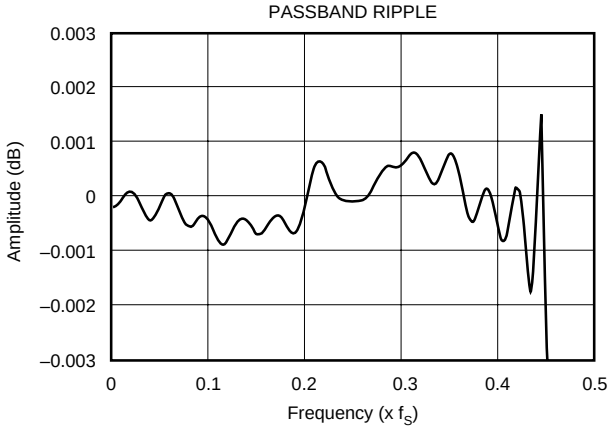
TYPICAL PERFORMANCE CURVES

All specifications at T_A = +25°C, V_{DD} = V_{CC} = 5V, SYSCLK = 384f_S (f_S = 44.1kHz), and 20-bit input data, unless otherwise noted.

DIGITAL FILTER

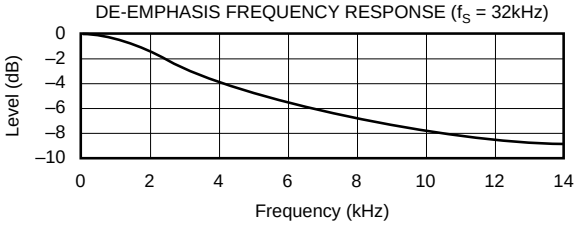
Digital Filter (De-Emphasis Off, f_S = 44.1kHz)

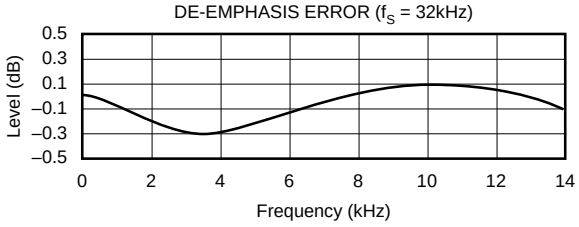


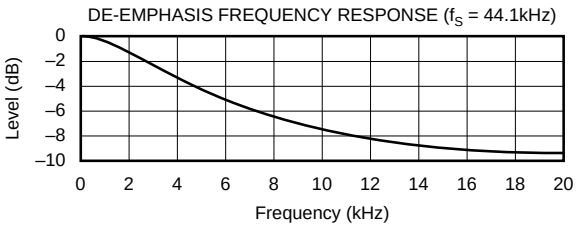


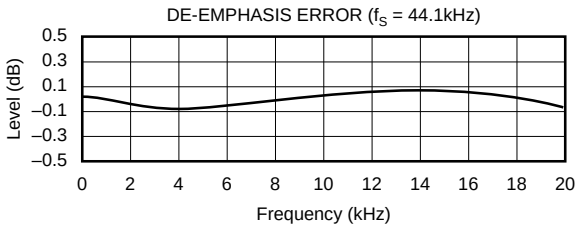
DIGITAL FILTER

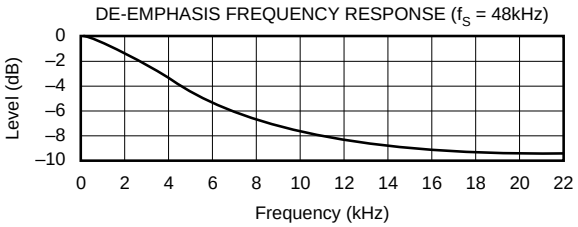
De-Emphasis Error

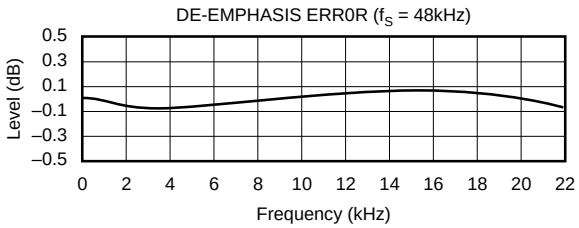












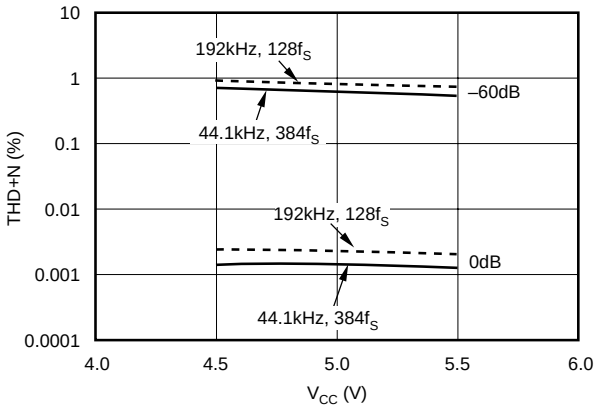
TYPICAL PERFORMANCE CURVES (cont.)

All specifications at T_A = +25°C, V_{DD} = V_{CC} = 5V, SYSCLK = 384f_S (f_S = 44.1kHz), and 20-bit input data, unless otherwise noted.

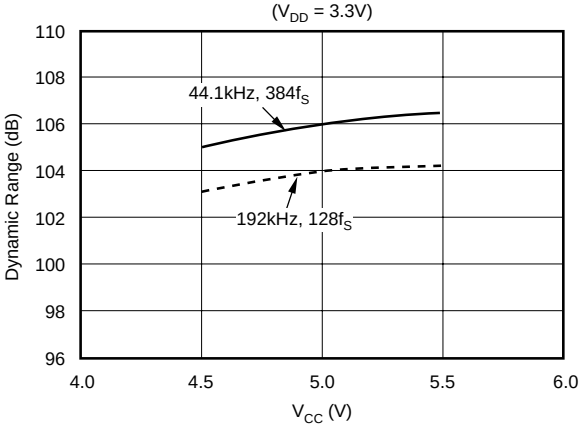
ANALOG DYNAMIC PERFORMANCE

Supply Voltage Characteristics

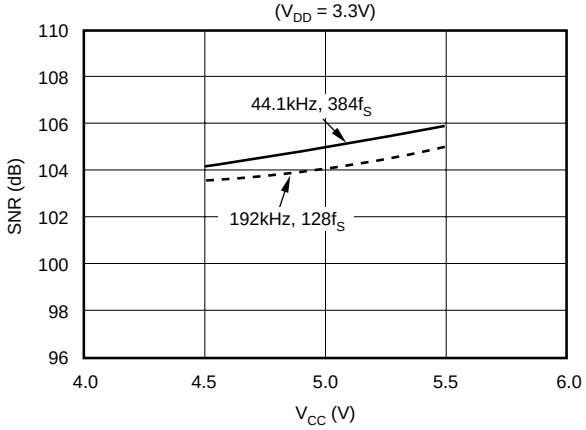
TOTAL HARMONIC DISTORTION + NOISE vs V_{CC}
(V_{DD} = 3.3V)



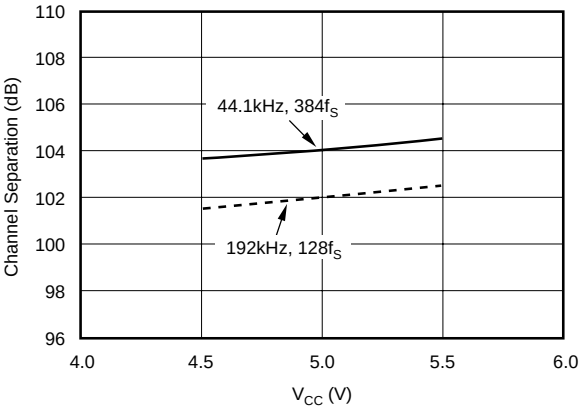
DYNAMIC RANGE vs V_{CC}
(V_{DD} = 3.3V)



SIGNAL-TO-NOISE RATIO vs V_{CC}
(V_{DD} = 3.3V)

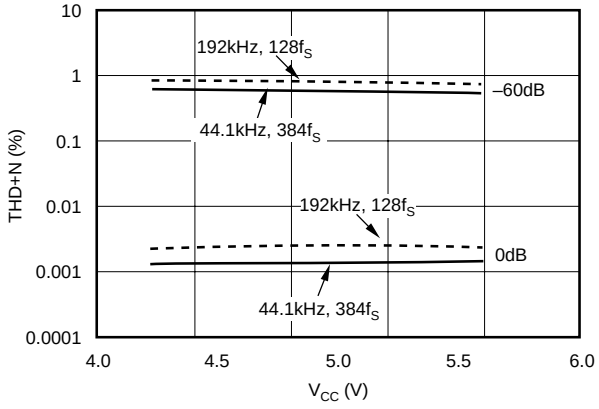


CHANNEL SEPARATION vs V_{CC}

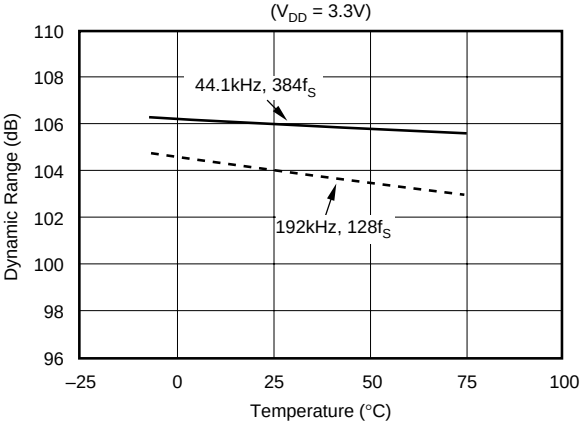


Temperature Characteristics

TOTAL HARMONIC DISTORTION + NOISE
vs TEMPERATURE



DYNAMIC RANGE vs TEMPERATURE
(V_{DD} = 3.3V)

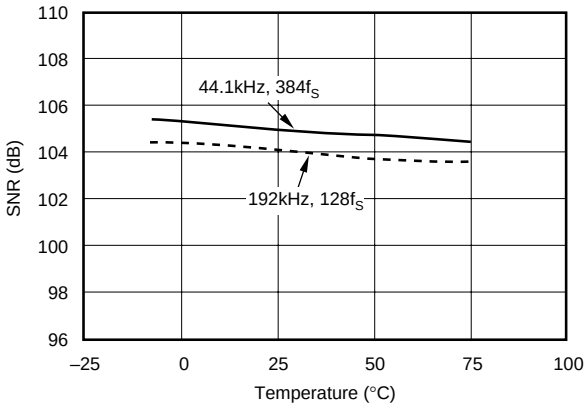


TYPICAL PERFORMANCE CURVES (cont.)

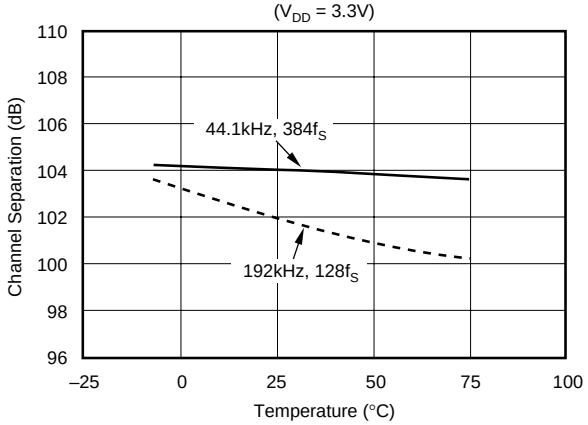
All specifications at T_A = +25°C, V_{DD} = V_{CC} = 5V, SYSCLK = 384f_S (f_S = 44.1kHz), and 20-bit input data, unless otherwise noted.

Temperature Characteristics (cont.)

SIGNAL-TO-NOISE RATIO vs TEMPERATURE
(V_{DD} = 3.3V)



CHANNEL SEPARATION vs TEMPERATURE
(V_{DD} = 3.3V)



SYSTEM CLOCK AND RESET FUNCTIONS

SYSTEM CLOCK INPUT

The PCM1739 requires a system clock for operating the digital interpolation filters and multi-level delta-sigma modulators. The system clock is applied at the SCLK input (pin 5). Table I shows examples of system clock frequencies for common audio sampling rates.

Figure 1 shows the timing requirements for the system clock input. For optimal performance, it is important to use a clock source with low phase jitter and noise. Burr-Brown's PLL1700 multi-clock generator is an excellent choice for providing the PCM1739 system clock.

SYSTEM CLOCK OUTPUT

A buffered version of the system clock input is available at the CLKO output (pin 4). CLKO operates at the same frequency as the system clock, SCLK.

POWER-ON AND EXTERNAL RESET FUNCTIONS

The PCM1739 includes a power-on reset function. Figure 2 shows the operation of this function. The system clock input at SCLK should be active for at least one clock period prior to V_{DD} = 2.0V. With the system clock active and V_{DD} > 2.0V, the power-on reset function will be enabled. The initialization sequence requires 1024 system clocks from the time V_{DD} > 2.0V. The PCM1739 also includes an external reset capability using the $\overline{RSTB}$ input (pin 22). This allows an external controller or master reset circuit to force the PCM1739 to initialize to its reset default state. For normal operation, $\overline{RSTB}$ should be set to a logic '1'.

Figure 3 shows the external reset operation and timing. The $\overline{RSTB}$ pin is set to logic '0' for a minimum of 20ns. The $\overline{RSTB}$ pin is then set to a logic '1' state, which starts the initialization sequence, which lasts for 1024 system clock periods.

The external reset is especially useful in applications where there is a delay between PCM1739 power up and system clock activation. In this case, the $\overline{RSTB}$ pin should be held at a logic '0' level until the system clock has been activated.

SAMPLING FREQUENCY (f_S)	SYSTEM CLOCK FREQUENCY, f_{SCLK}, (MHZ)					
	$128f_S$	$192f_S$	$256f_S$	$384f_S$	$512f_S$	$768f_S$
16kHz	—	—	4.0960	6.1440	8.1920	12.2880
32kHz	—	—	8.1920	12.2880	16.3840	24.5760
44.1kHz	—	—	11.2896	16.9344	22.5792	33.8688
48kHz	—	—	12.2880	18.4320	24.5760	36.8640
88.2kHz	—	—	22.5792	33.8688	45.1584	See Note 1
96kHz	12.2880	18.4320	24.5760	36.8640	49.1520	See Note 1
176.4kHz	24.5792	33.8688	See Note 2	See Note 2	See Note 2	See Note 2
192kHz	24.5760	36.8640	See Note 2	See Note 2	See Note 2	See Note 2

NOTES: (1) The $768f_S$ system clock rate is not supported for f_S > 64kHz. (2) This system clock rate is not supported for the given sampling frequencies.

TABLE I. System Clock Rates for Common Audio Sampling Frequencies.

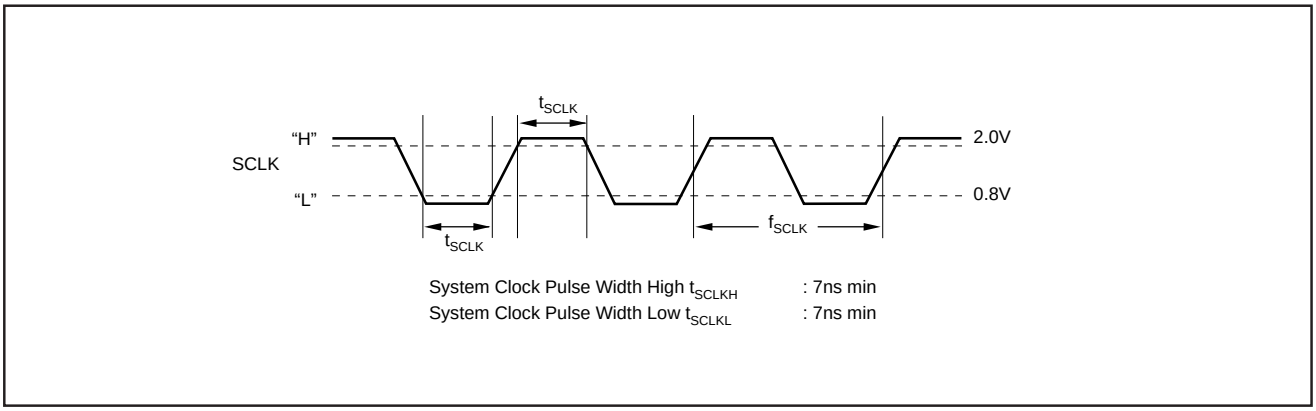


FIGURE 1. System Clock Input Timing.

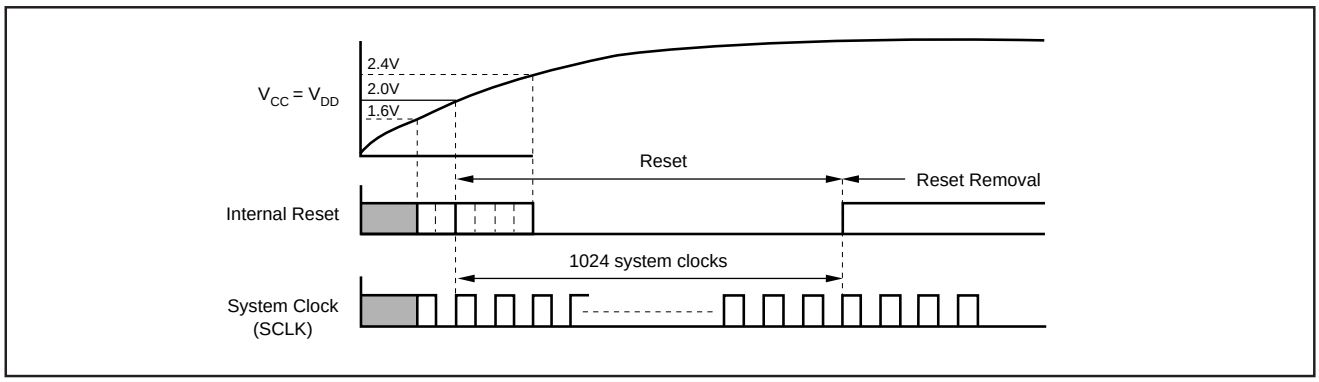


FIGURE 2. Power-On Reset Timing.

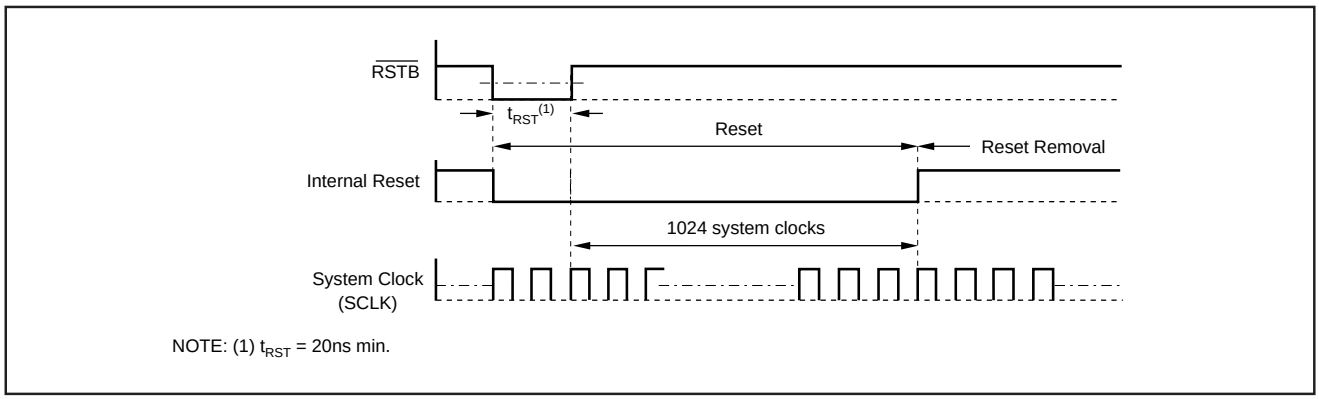


FIGURE 3. External Reset Timing.

AUDIO SERIAL INTERFACE

The audio serial interface for the PCM1739 is comprised of a 3-wire synchronous serial port. It includes LRCK (pin 1), BCLK (pin 3), and DATA (pin 2). BCLK is the serial audio bit clock, and is used to clock the serial data present on DATA into the audio interface's serial shift registers. Serial data is clocked into the PCM1739 on the rising edge of BCLK. LRCK is the serial audio left/right word clock. It is used to latch serial data into the serial audio interface's internal registers.

Both LRCK and BCLK must be synchronous to the system clock. Ideally, it is recommended that LRCK and BCLK be derived from the system clock input or output, SCLK or CLKO. The left/right clock, LRCK, is operated at the sampling frequency (f_S). The bit clock, BCK, may be operated at 48 or 64 times the sampling frequency.

AUDIO DATA FORMATS AND TIMING

The PCM1739 supports industry-standard audio data formats, including Standard and I^2S. The audio data word length may be either 24 or 16 bits. Data format and word length are selected using the FORM and IBIT pins, as described in the Mode Controls section of this data sheet. All formats require Binary Two's Complement, MSB-first audio data. The data formats are shown in Figure 4, while Figure 5 shows a detailed timing diagram for the serial audio interface.

MODE CONTROLS

This section describes the mode control pins used to configure the operating mode of the PCM1739.

AUDIO DATA FORMAT

The data format used by the audio serial interface is selected using the FORM input (pin 28). The formats available include Standard and I^2S. Table II shows the FORM pin configuration.

FORM	DATA FORMAT
L	Standard
H	I^2S

TABLE II. Audio Data Format Selection.

AUDIO DATA WORD LENGTH

The data word length used by the audio serial interface is selected using the IBIT input (pin 9). The word length may be either 24 or 16 bits. Table III shows the IBIT pin configuration.

IBIT	DATA WORD LENGTH
L	24 Bits
H	16 Bits

TABLE III. Audio Data Word Length Selection.

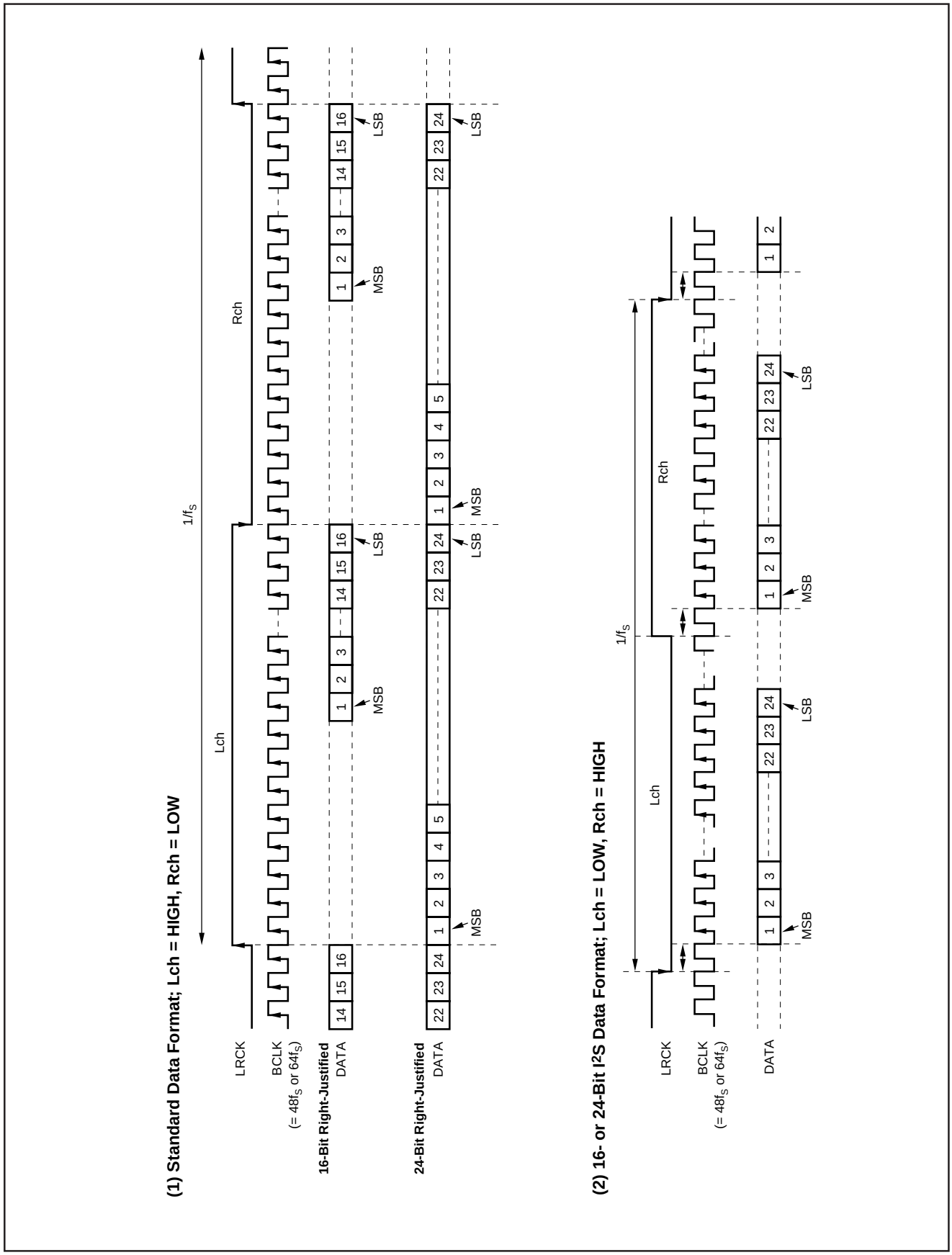
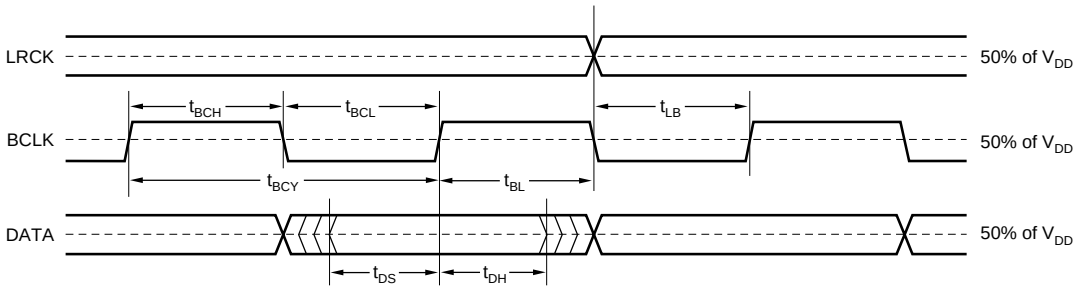


FIGURE 4. Audio Data Input Formats.



SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{BCY}	BCK Pulse Cycle Time		48 or 64f_S(1)	
t_{BCH}	BCK High Level Time	35		ns
t_{BCL}	BCK Low Level Time	35		ns
t_{BL}	BCK Rising Edge to LRCK Edge	10		ns
t_{LB}	LRCK Falling Edge to BCK Rising Edge	10		ns
t_{DS}	DIN Set Up Time	10		ns
t_{DH}	DIN Hold Time	10		ns

NOTE: (1) f_S is the sampling frequency.

FIGURE 5. Audio Interface Timing.

4x/8x DIGITAL INTERPOLATION

The PCM1739's digital filter may be configured for either 4x or 8x oversampling. The 8x oversampling setting is utilized for sampling frequencies up to 96kHz, while 4x oversampling is utilized for 192kHz operation. The FILT input (pin 20) is used to select the oversampling rate of the digital filter. Table IV shows the FILT pin configuration.

FILT	OVERSAMPLING RATE
L	8x
H	4x (Required for 192kHz operation)

TABLE IV. Digital Filter Oversampling Rate Selection.

SOFT MUTE

The Soft Mute function provides for quiet muting of the DAC outputs, $V_{OUT}L$ (pin 16) and $V_{OUT}R$ (pin 13). This is done by ramping an internal digital attenuator from unity gain to digital mute (all 0's input to the digital filter). The MUTE input (pin 21) is used to enable and disable the Soft Mute function. Table V shows the MUTE pin configuration.

MUTE	SOFT MUTE STATUS
L	Disabled
H	Enabled

TABLE V. Soft Mute Selection.

DIGITAL DE-EMPHASIS

The PCM1739 provides a De-emphasis function for sampling rates equal to 32kHz, 44.1kHz or 48kHz. It is incorporated into the digital filter of the PCM1739. The De-emphasis function is required for proper playback of early audio compact disks (CDs), which were mastered with signal emphasis for higher frequencies in the audio band. This was done to improve the poor high frequency performance of early CD players. Plots of the de-emphasis filter and error functions for 32kHz, 44.1kHz, and 48kHz are shown in the Typical Performance Curves section of this data sheet.

The DEM0 (pin 26) and DEM1 (pin 27) inputs of the PCM1739 are used to enable and disable the digital de-emphasis function. Table VI shows the DEM0 and DEM1 pin configurations.

DEM1	DEM0	DE-EMPHASIS FUNCTION
L	L	OFF
L	H	32kHz De-Emphasis Filter
H	L	44.1kHz De-Emphasis Filter
H	H	48kHz De-Emphasis Filter

TABLE VI. Digital De-Emphasis.

ANALOG OUTPUTS

The PCM1739 includes two independent output channels; $V_{OUT}L$ (pin 16) and $V_{OUT}R$ (pin 13). These are unbalanced outputs, each capable of driving 3.1Vp-p typical into a 5kΩ, AC-coupled load (V_{CC} = +5V). The internal output amplifiers for $V_{OUT}L$ and $V_{OUT}R$ are DC biased to a DC common-mode (or bipolar zero) voltage, equal to $V_{CC}/2$.

The output amplifiers include an RC continuous time filter, which helps to reduce the out-of-band noise energy present at the DAC outputs due to the noise shaping characteristics of the PCM1739's delta-sigma D/A converters. The fre-

quency response of this filter is shown in Figure 6. By itself, this filter is not enough to attenuate the out-of-band noise to an acceptable level for most applications. An external low-pass filter is required to provide sufficient out-of-band noise rejection. Further discussion of DAC post filter circuits is provided in the Applications Information section of this data sheet.

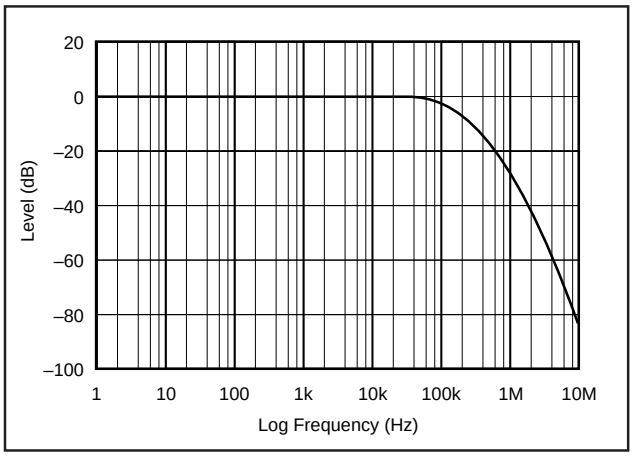


FIGURE 6. Output Filter Frequency Response.

V_{COM}L AND V_{COM}R OUTPUTS

Two unbuffered, DC common-mode voltage output pins, V_{COM}L (pin 17) and V_{COM}R (pin 12), are brought out for decoupling purposes. These pins are normally biased to a DC voltage level equal to $V_{CC}/2$. These pins may be used to bias external circuits, but they must be connected to high impedance nodes. Figure 7 shows examples of the proper use of the V_{COM}L and V_{COM}R pins for external biasing applications.

ZERO FLAG OUTPUTS

The PCM1739 includes circuitry for detecting an all zero data condition for the data input pin, DATA. Zero detection for each output channel is independent from the other. If the data for a given channel remains at a '0' level for 1024 sample periods (or LRCK clock periods), a Zero Detect condition exists for the that channel. Given that a Zero Detect condition exists, the Zero Flag pin(s) for the corresponding channel(s) will be set to a logic '1' state. The zero flag outputs include ZEROL (pin 23) and ZEROR (pin 24). These pins can be used to operate external mute circuits, or used as status indicators for audio signal processor, microcontroller, or other digitally-controlled functions.

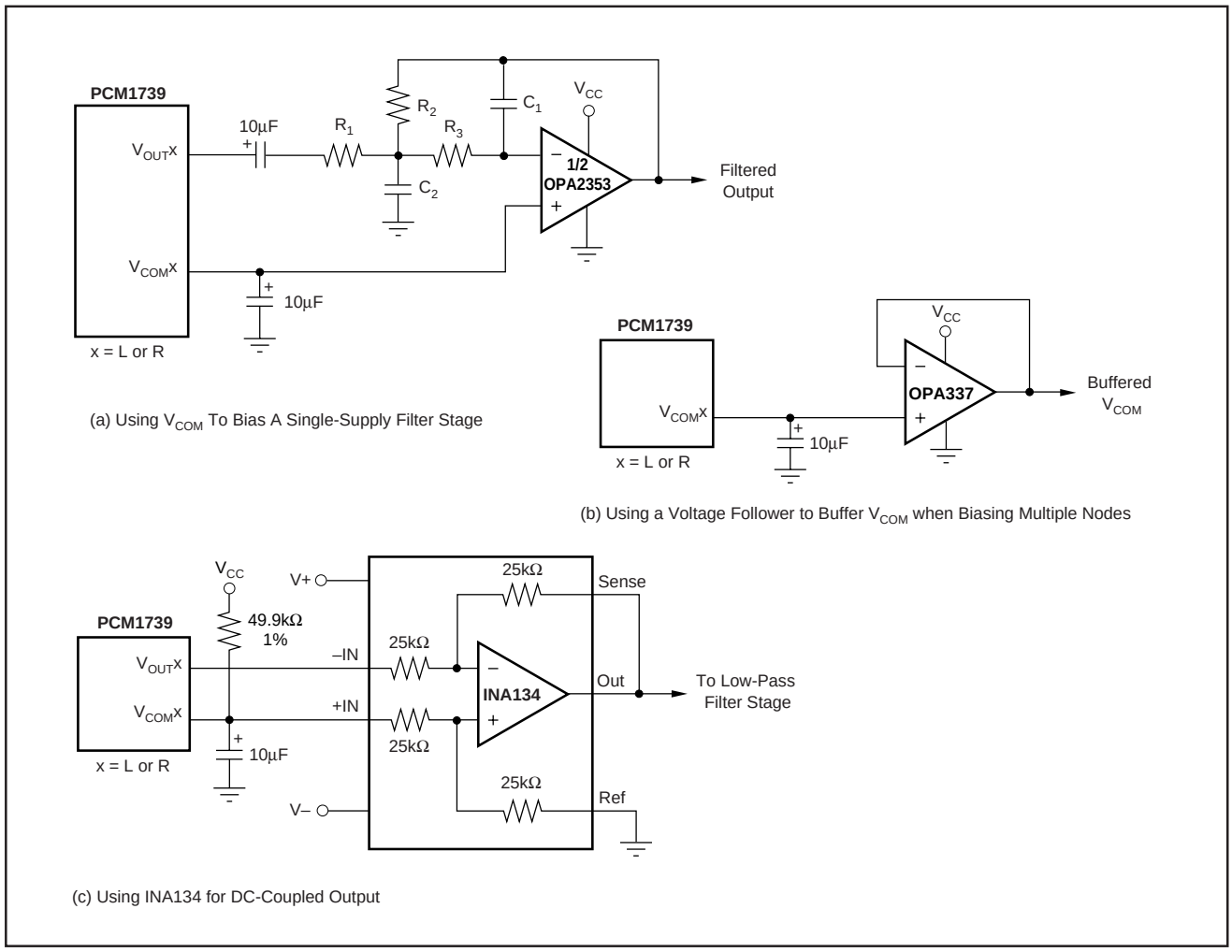


FIGURE 7. Biasing External Circuits Using the V_{COM}L and V_{COM}R Pins.

APPLICATIONS INFORMATION

CONNECTION DIAGRAM

A basic connection diagram with the necessary power supply bypassing and decoupling components is shown in Figure 8. Burr-Brown recommends using the component values shown in Figure 8 for all designs.

The use of series resistors (22Ω to 100Ω) is recommended for the SCLK, LRCK, BCLK, and DATA inputs. The series resistor combines with the stray PCB and device input capacitance to form a low-pass filter, which reduces high frequency noise emissions and helps to dampen glitches and ringing present on clock and data lines.

POWER SUPPLIES AND GROUNDING

The PCM1739 requires a +5V analog supply and a +3.3V digital supply. The +5V supply is used to power the DAC analog and output filter circuitry, while the +3.3V supply is used to power the digital filter and logic circuitry. For best performance, the +3.3V supply should be derived from the +5V supply using a linear regulator, shown in Figure 8. Burr-Brown's REG1117-3.3 is an ideal choice for this application.

Proper power supply bypassing is shown in Figure 8. The bypass capacitors should be located as close as possible to the PCM1739 package. The 1µF and 10µF capacitors should be tantalum or aluminum electrolytic, while the 0.1µF capacitors are ceramic (X7R type is recommended for surface mount applications).

D/A OUTPUT CIRCUITS

Delta-sigma D/A converters utilize noise-shaping techniques to improve in-band Signal-to-Noise (SNR) performance at the expense of generating increased out-of-band noise above the Nyquist Frequency, or $f_S/2$. The out-of-band noise must be low-pass filtered in order to provide optimal converter performance. This is accomplished by a combination of on-chip and external low pass filtering.

Figures 7a and 9 show the recommended external low pass active filter circuits for dual and single-supply applications. These circuits are 2nd-order filters using the Multiple Feedback (MFB) circuit arrangement, which reduces sensitivity to passive component variations over frequency and temperature. For more information regarding MFB active filter design, please refer to Burr-Brown Applications Bulletin AB-034.

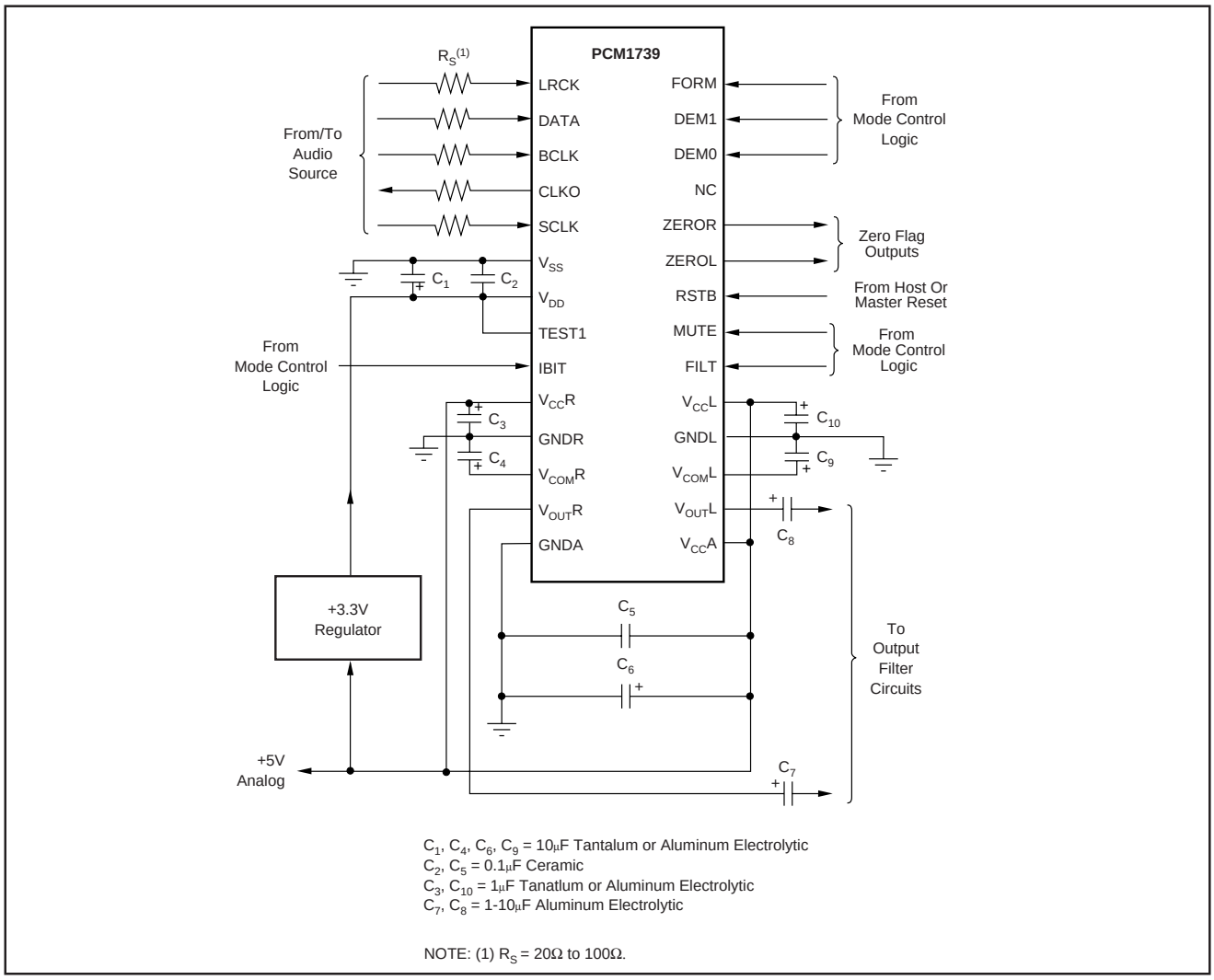


FIGURE 8. Basic Connection Diagram.

Since the overall system performance is defined by the quality of the D/A converters and their associated analog output circuitry, high quality audio op amps are recommended for the active filters. Burr-Brown's OPA2134 and OPA2353 dual op amps are shown in Figures 7a and 9, and are recommended for use with the PCM1739.

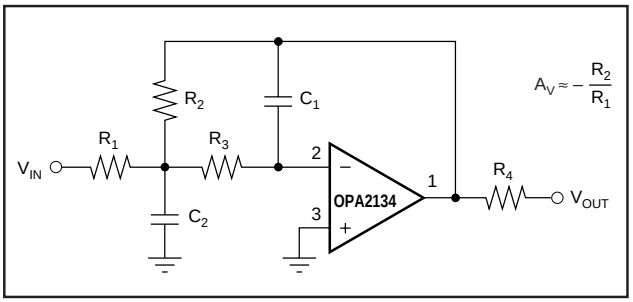


FIGURE 9. Dual Supply Filter Circuit.

PCB LAYOUT GUIDELINES

A typical PCB floor plan for the PCM1739 is shown in Figure 10. A ground plane is recommended, with the analog and digital sections being isolated from one another using a split or cut in the circuit board. The PCM1739 should be oriented with the digital I/O pins facing the ground plane split/cut, allowing for direct connection of the digital audio interface and control signals originating from the digital section of the board.

Separate power supplies are recommended for the digital and analog sections of the board. This prevents the switching noise present on the digital supply from contaminating the analog power supply and degrading the dynamic performance of the PCM1739. In cases where a common +5V supply must be used for the analog and digital sections, an

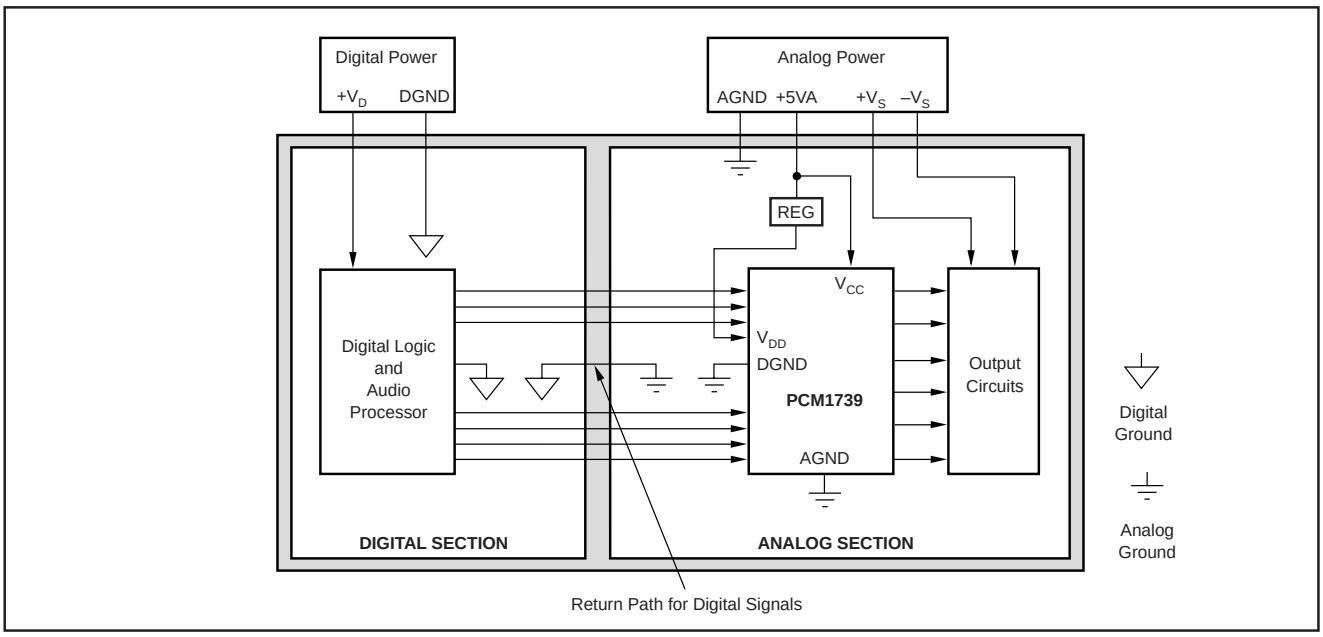


FIGURE 10. Recommended PCB Layout.

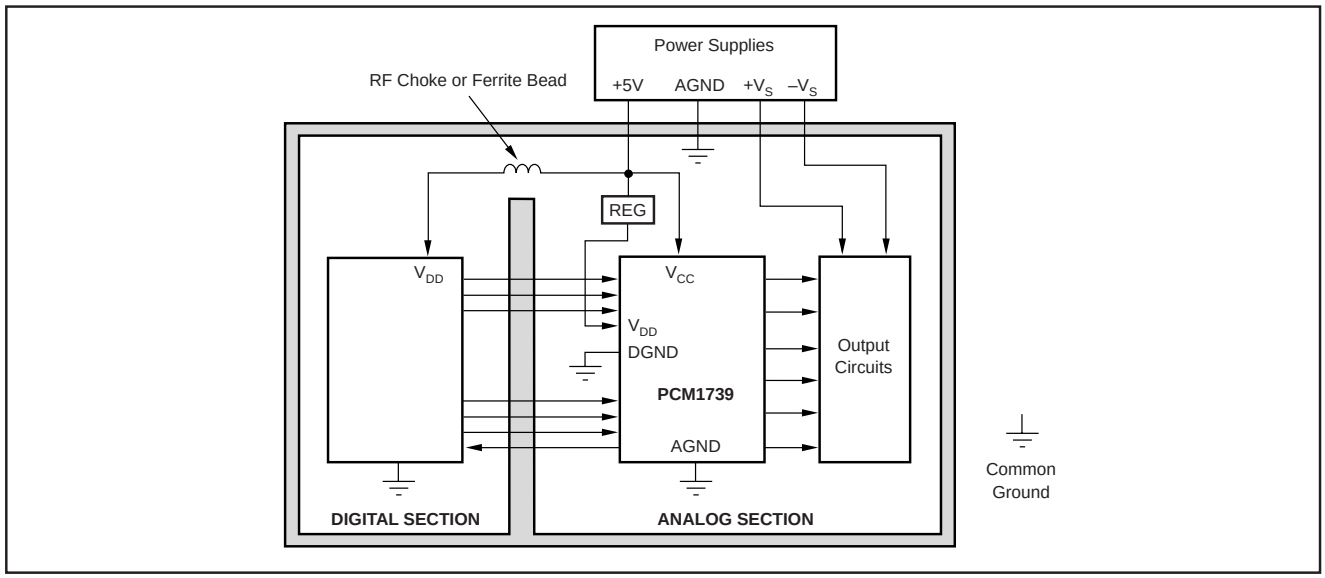


FIGURE 11. Single-Supply PCB Layout.

inductance (RF choke, ferrite bead) should be placed between the analog and digital +5V supply connections to avoid coupling of the digital switching noise into the analog circuitry. Figure 11 shows the recommended approach for single-supply applications

THEORY OF OPERATION

The delta-sigma section of PCM1739 is based on a 8-level amplitude quantizer and a 4th-order noise shaper. This section converts the oversampled input data to 8-level delta-sigma format.

A block diagram of the 8-level delta-sigma modulator is shown in Figure 12. This 8-level delta-sigma modulator has the advantage of stability and clock jitter sensitivity over the typical one-bit (2-level) delta-sigma modulator.

The combined oversampling rate of the delta-sigma modulator and the interpolation filter is $64f_S$ for all system clock combinations (128, 192, 256, 384, 512, $768f_S$).

The theoretical quantization noise performance of the 8-level delta-sigma modulator is shown in Figure 13. The enhanced multi-level delta-sigma architecture also has advantages for input clock jitter sensitivity due to the multi-level quantizer, with the simulated jitter sensitivity shown in Figure 14.

KEY PERFORMANCE PARAMETERS AND MEASUREMENT

This section provides information on how to measure key dynamic performance parameters for the PCM1739. In all cases, an Audio Precision System Two Cascade or equivalent audio measurement system is utilized to perform the testing.

TOTAL HARMONIC DISTORTION + NOISE

Total Harmonic Distortion + Noise (THD+N) is a significant figure of merit for audio D/A converters since it takes into account both harmonic distortion and all noise sources within a specified measurement bandwidth. The true rms value of the distortion and noise is referred to as THD+N.

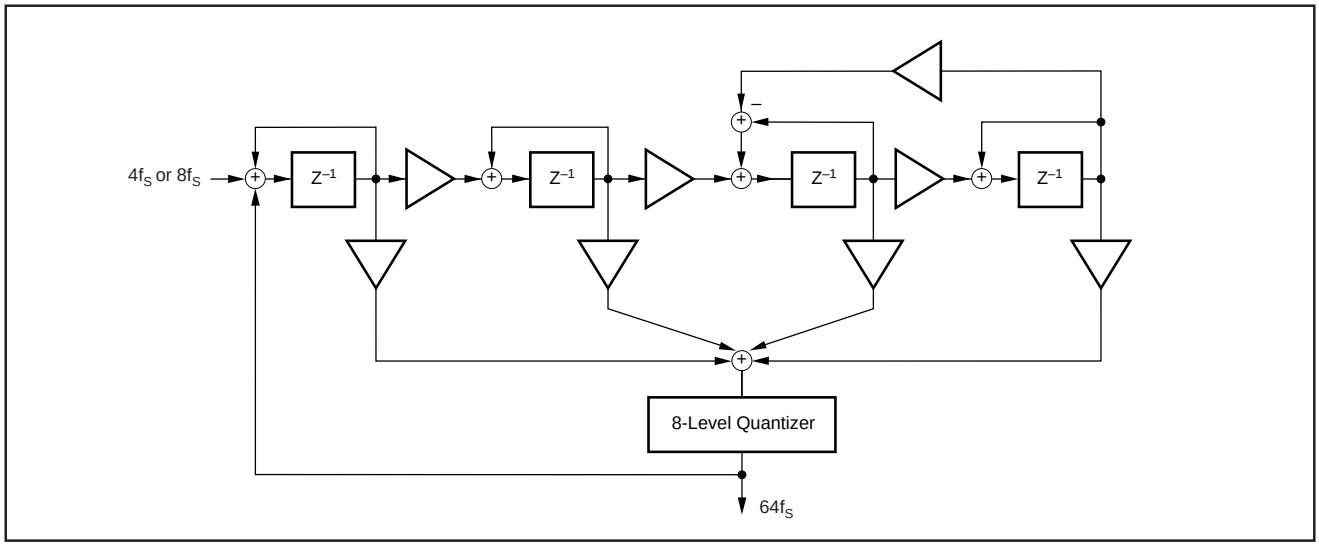


FIGURE 12. Eight-Level Delta-Sigma Modulator.

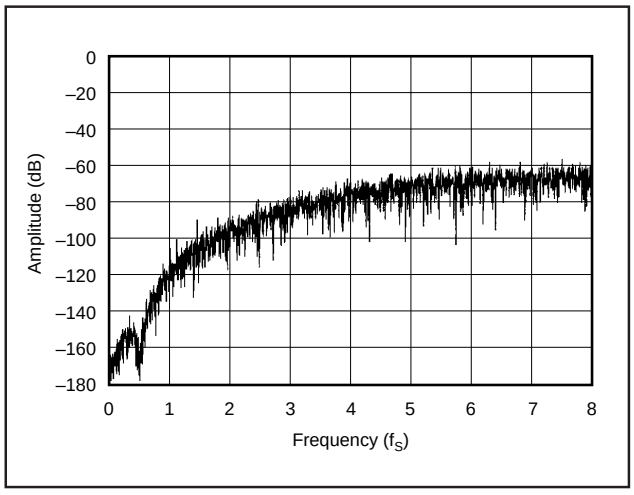


FIGURE 13. Quantization Noise Spectrum.

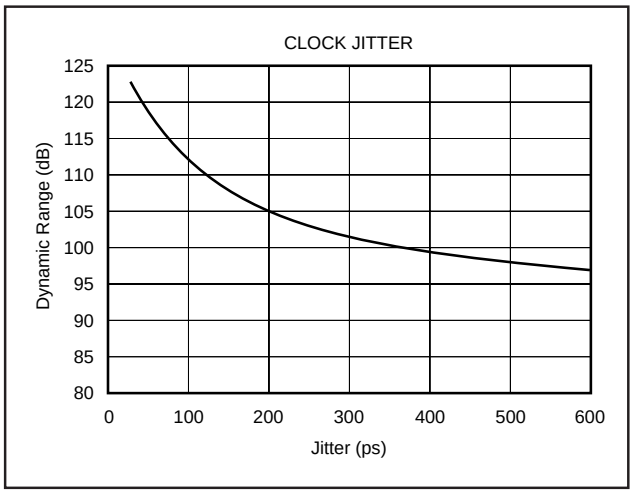


FIGURE 14. Jitter Sensitivity.

For the PCM1739, THD+N is measured with a full scale, 1kHz digital sine wave as the test stimulus at the input of the DAC. The digital generator is set to 24-bit audio word length and a sampling frequency of 44.1kHz, 96kHz, or 192kHz. The digital generator output is taken from the unbalanced S/PDIF connector of the measurement system. The S/PDIF data is transmitted via a coaxial cable to the digital audio receiver on the DEM-DAI1739 demo board. The receiver is then configured to output 24-bit data in either I^2S or left-justified data format. The DAC audio interface format is programmed to match the receiver output format. The analog output is then taken from the DAC post filter and connected to the analog analyzer input of the measurment system. The analog input is band limited using filters resident in the analyzer. The resulting THD+N is measured by the analyzer and displayed by the measurement system.

DYNAMIC RANGE

Dynamic range is specified as A-Weighted, THD+N measured with a –60dBFS, 1kHz digital sine wave stimulus at the input of the D/A converter. This measurement is designed to give a good indicator of how the DAC will perform given a low-level input signal.

The measurement setup for the dynamic range measurement is shown in Figure 15, and is similar to the THD+N test setup discussed previously. The differences include the bandlimit filter selection, the additional A-Weighting filter, and the –60dBFS input level.

IDLE CHANNEL SIGNAL-TO-NOISE RATIO

The SNR test provides a measure of the noise floor of the D/A converter. The input to the D/A is all 0's data, and the D/A converter's Infinite Zero Detect Mute function must be disabled (default condition at power up for the PCM1739). This ensures that the delta-sigma modulator output is connected to the output amplifier circuit so that idle tones (if present) can be observed and effect the SNR measurement. The dither function of the digital generator must also be disabled to ensure an all '0's data stream at the input of the D/A converter.

The measurement setup for SNR is identical to that used for dynamic range, with the exception of the input signal level. (see the notes provided in Figure 16).

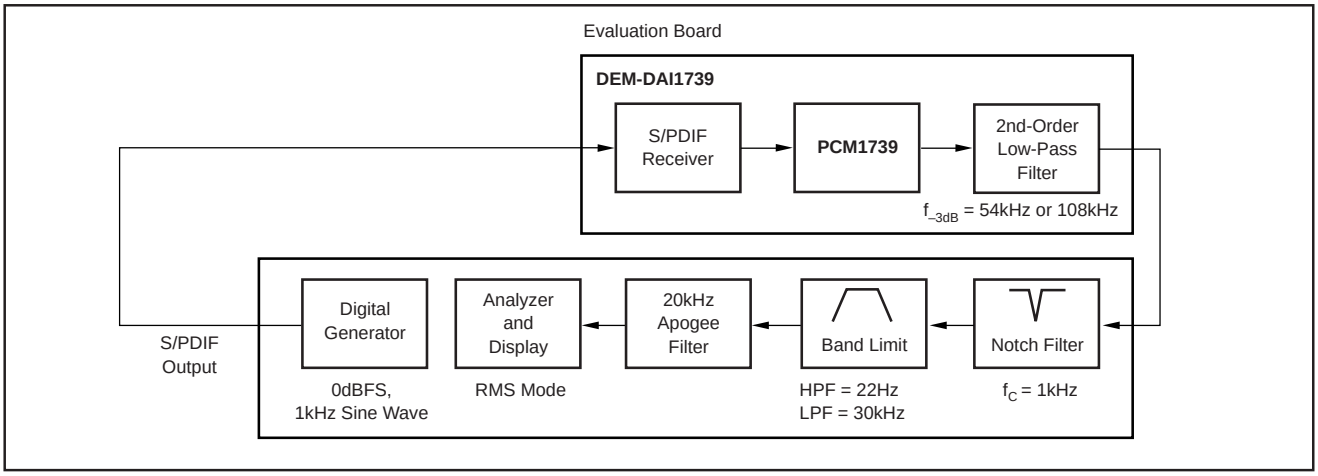


FIGURE 15. Test Setup for THD+N Measurement.

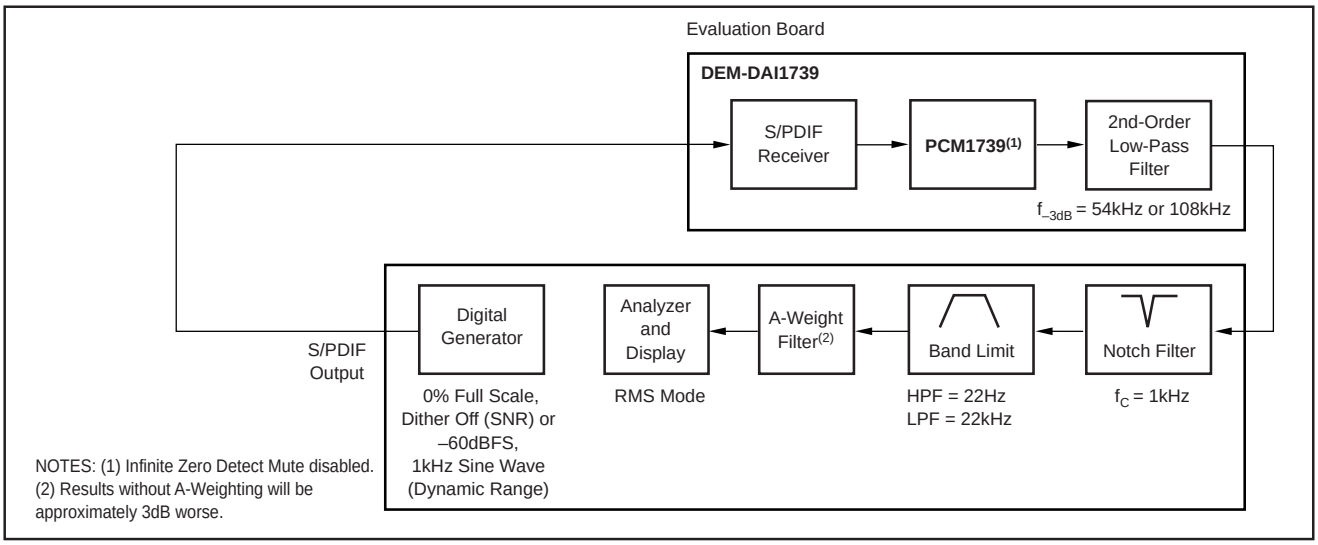


FIGURE 16. Test Set-Up for Dynamic Range and SNR Measurements.