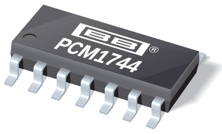
BURR - BROWN®



PCM1744

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SoundPlus™ 24 Bits, 96kHz, Sampling Stereo Audio DIGITAL-TO-ANALOG CONVERTER

FEATURES

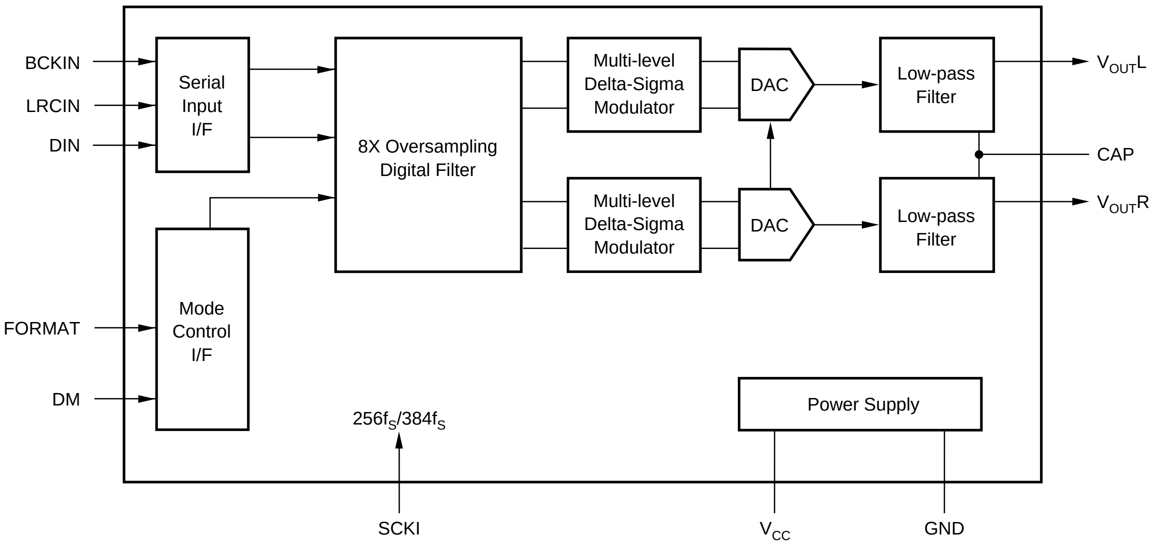
- COMPLETE STEREO DAC: Includes Digital Filter and Output Amp
- DYNAMIC RANGE: 95dB
- MULTIPLE SAMPLING FREQUENCIES: Up to 96kHz
- 8x OVERSAMPLING DIGITAL FILTER
- SYSTEM CLOCK: $256f_S/384f_S$
- 24-BIT I^2S DATA INPUT FORMAT
- SMALL 14-PIN SOIC PACKAGE

DESCRIPTION

The PCM1744 is a complete low cost stereo audio digital-to-analog converter (DAC), operating off of a $256f_S$ or $384f_S$ system clock. The DAC contains a 3rd-order ΔΣ modulator, a digital interpolation filter, and an analog output amplifier. The PCM1744 accepts 24-bit input data in a I^2S format.

The digital filter performs an 8x interpolation function and includes de-emphasis at 44.1kHz. The PCM1744 can accept digital audio sampling frequencies from 16kHz to 96kHz, always at 8X oversampling.

The PCM1744 is ideal for low-cost, CD-quality consumer audio applications.



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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

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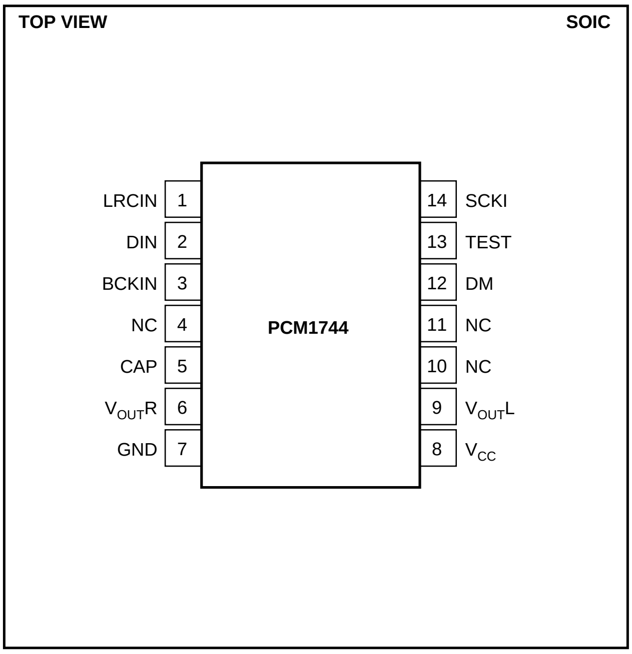
SPECIFICATIONS

All specifications at +25°C, $+V_{CC}$ = +5V, f_S = 44.1kHz, and 18-bit input data, SYSCLK = $384f_S$, unless otherwise noted.

PARAMETER	CONDITIONS	PCM1744 MIN	PCM1744 TYP	PCM1744 MAX	UNITS
RESOLUTION			24		Bits
DATA FORMAT					
Audio Data Interface Format			I^2S		
Audio Data Format			Two's Binary Complement		
Sampling Frequency (f_S)		16		96	kHz
Internal System Clock Frequency			$256f_S/384f_S$		
DIGITAL INPUT/OUTPUT					
Logic Level			TTL		
Input Logic Level					
V_{IH} (1)		2.0			VDC
V_{IL} (1)				0.8	VDC
Input Logic Current: I_{IN} (1)				±0.8	µA
DYNAMIC PERFORMANCE(2)	f = 991kHz				
THD+N at FS (0dB)			–83	–79	dB
THD+N at –60dB			–32		dB
Dynamic Range	EIAJ, A-weighted	90	95		dB
Signal-to-Noise Ratio	EIAJ, A-weighted	90	97		dB
Channel Separation		88	95		dB
DC ACCURACY					
Gain Error			±1.0	±10.0	% of FSR
Gain Mismatch, Channel-to-Channel			±1.0	±5.0	% of FSR
Bipolar Zero Error	$V_{OUT} = V_{CC}/2$ at BPZ		±20	±50	mV
ANALOG OUTPUT					
Output Voltage	Full Scale (0dB)		0.62 x V_{CC}		Vp-p
Center Voltage			$V_{CC}/2$		VDC
Load Impedance	AC Load	10			kΩ
DIGITAL FILTER PERFORMANCE					
Passband				0.445	f_S
Stopband		0.555			f_S
Passband Ripple				±0.17	dB
Stopband Attenuation		–35			dB
Delay Time			$11.125/f_S$		sec
INTERNAL ANALOG FILTER					
–3dB Bandwidth			100		kHz
Passband Response	f = 20kHz		–0.16		dB
POWER SUPPLY REQUIREMENTS					
Voltage Range		4.5	5	5.5	VDC
Supply Current			13	18	mA
Power Dissipation			65	90	mW
TEMPERATURE RANGE					
Operation		–25		+85	°C
Storage		–55		+125	°C

NOTES: (1) Pins 1, 2, 3, 12, 13, 14: LRCIN, DIN, BCKIN, DM, FORMAT, SCKI. (2) Dynamic performance specs are tested with 20kHz low pass filter and THD+N specs are tested with 30kHz LPF, 400Hz HPF, Average-Mode.

PIN CONFIGURATION



PIN ASSIGNMENTS

PIN	NAME	I/O	FUNCTION
1(1)	LRCIN	IN	Sample Rate Clock Input
2(1)	DIN	IN	Audio Data Input
3(1)	BCKIN	IN	Bit Clock Input for Audio Data.
4	NC	—	No Connection
5	CAP	—	Common Pin of Analog Output Amp
6	$V_{OUT}R$	OUT	Right-Channel Analog Output
7	GND	—	Ground
8	V_{CC}	—	Power Supply
9	$V_{OUT}L$	OUT	Left-Channel Analog Output
10	NC	—	No Connection
11	NC	—	No Connection
12(2)	DM	IN	De-Emphasis Control HIGH: De-emphasis ON LOW: De-emphasis OFF
13(2)	TEST	—	Test Pin. Must be left open.
14(1)	SCKI	IN	System Clock Input ($256f_S$ or $384f_S$)

NOTE: (1) Schmitt-Trigger input. (2) Schmitt-Trigger input with internal pull-up.

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage ..... +6.5V
$+V_{CC}$ to $+V_{DD}$ Difference ..... ±0.1V
Input Logic Voltage ..... –0.3V to (V_{DD} + 0.3V)
Power Dissipation 290mW
Operating Temperature Range ..... –25°C to +85°C
Storage Temperature ..... –55°C to +125°C
Lead Temperature (soldering, 5s) ..... +260°C
Thermal Resistance, θ_{JA} ..... +90°C/W

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

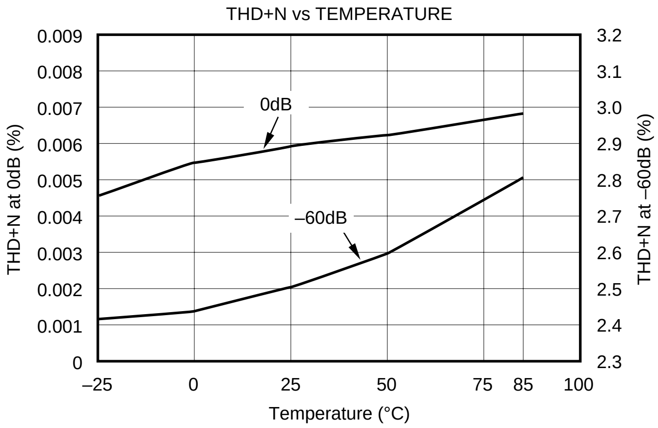
PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER(1)	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER(2)	TRANSPORT MEDIA
PCM1744	SO-14	235	–25°C to +85°C	PCM1744U	PCM1744U	Rails
"	"	"	"	PCM1744U	PCM1744U/2K	Tape and Reel

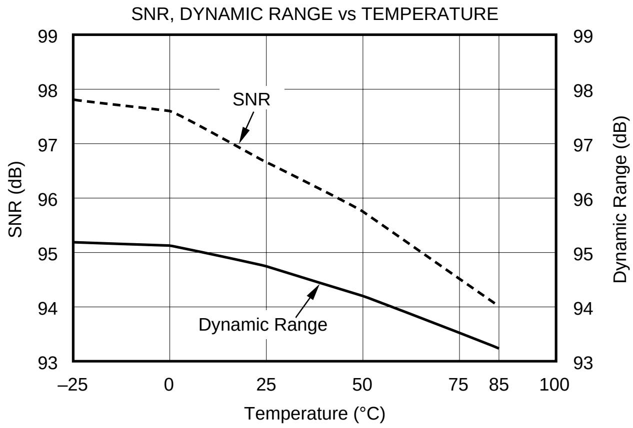
NOTES: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book, or visit the Burr-Brown web site at www.burr-brown.com. (2) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /2K indicates 2000 devices per reel). Ordering 2000 pieces of “PCM1744U/2K” will get a single 2500-piece Tape and Reel. For detailed Tape and Reel mechanical information, refer to Appendix B of Burr-Brown IC Data Book.

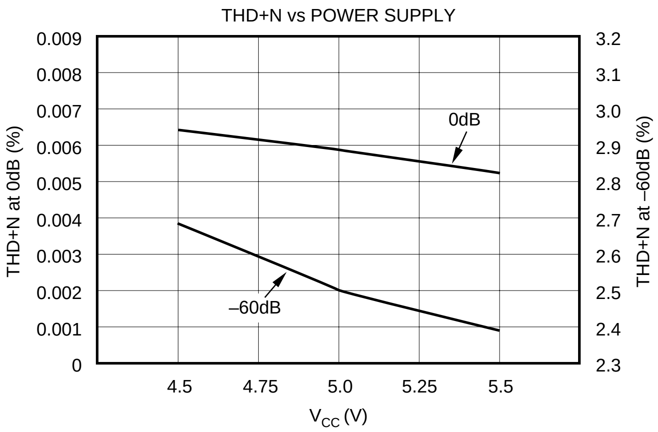
TYPICAL PERFORMANCE CURVES

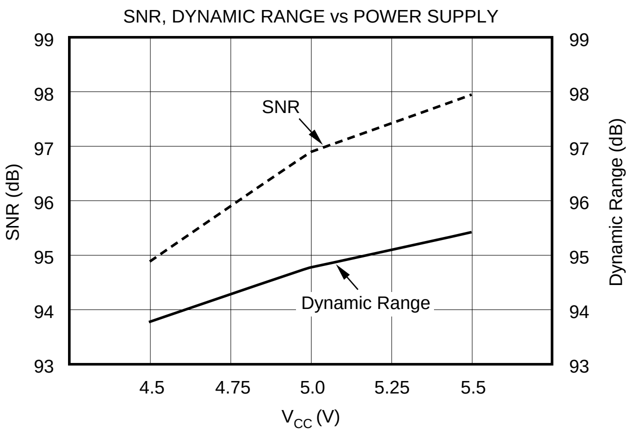
At T_A = +25°C, $+V_{CC}$ = +5V, f_S = 44.1kHz, SYSCLK = $256f_S$, unless otherwise noted.

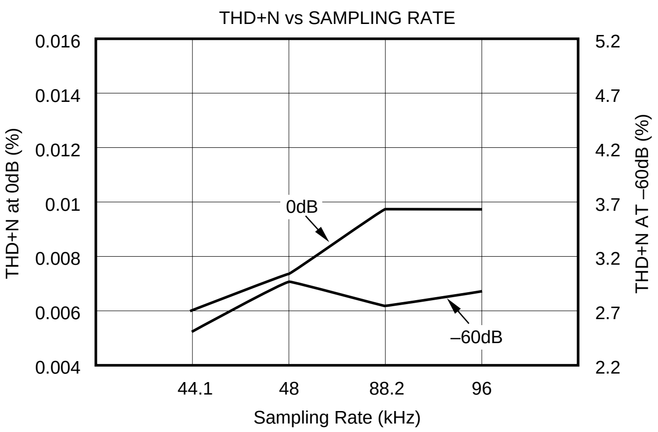
DYNAMIC PERFORMANCE

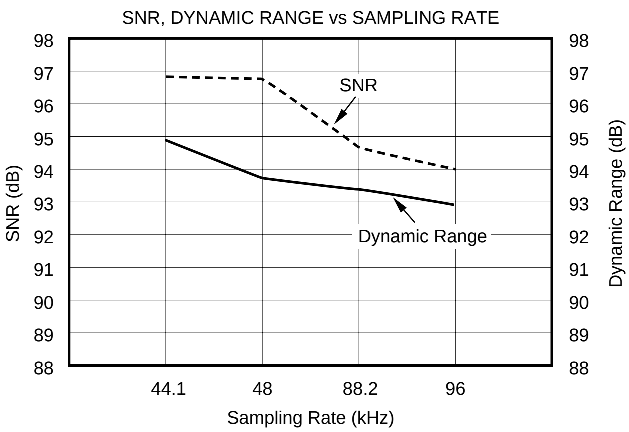








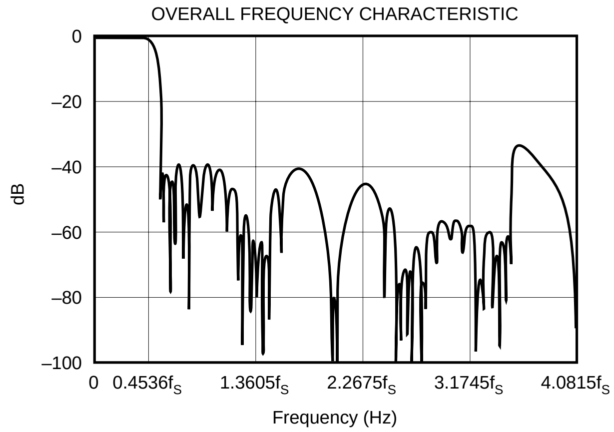


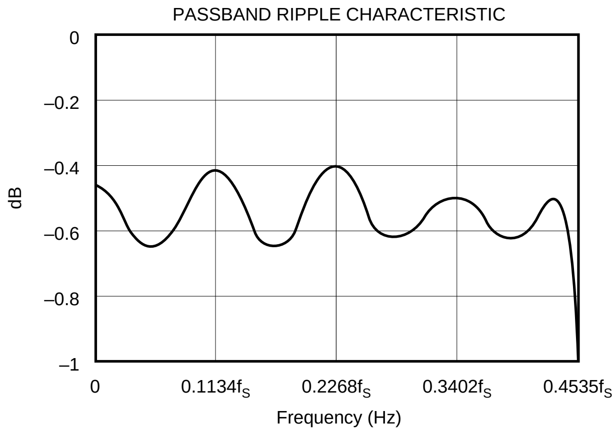


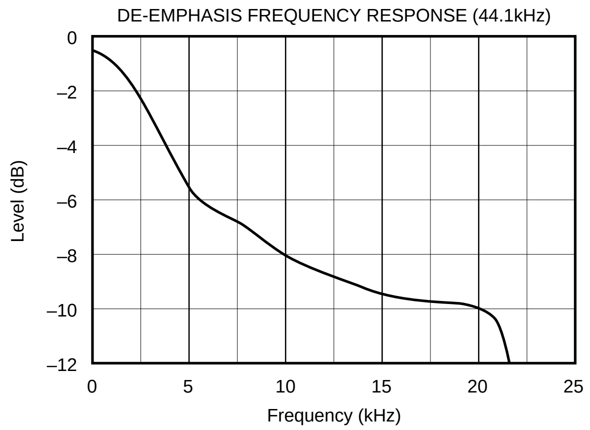
TYPICAL PERFORMANCE CURVES

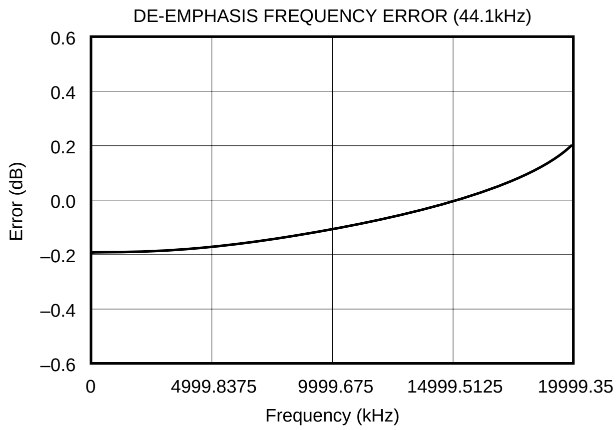
At T_A = +25°C, $+V_{CC}$ = $+V_{DD}$ = +5V, f_S = 44.1kHz, and 18-bit input data, SYSCLK = $384f_S$, unless otherwise noted.

DIGITAL FILTER









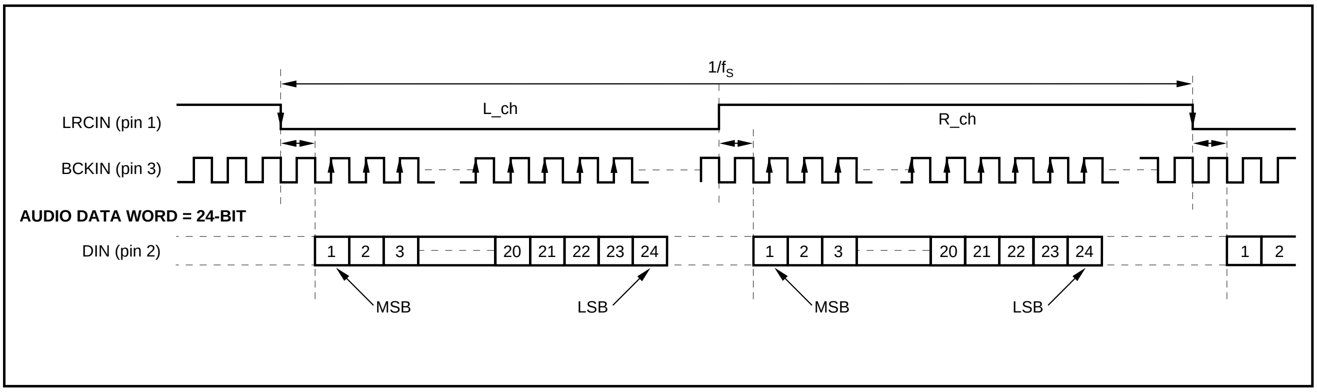
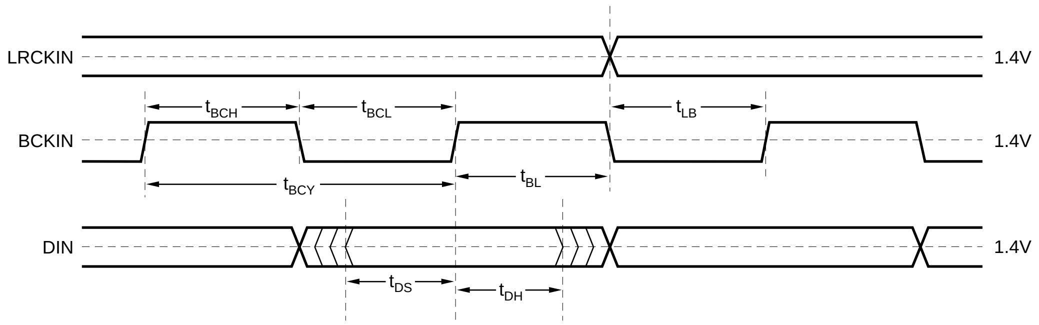
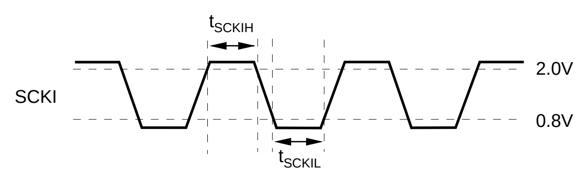


FIGURE 1. I^2S Data Input Timing.



BCKIN Pulse Cycle Time	: t_{BCY}	: 100ns (min)
BCKIN Pulse Width High	: t_{BCH}	: 50ns (min)
BCKIN Pulse Width Low	: t_{BCL}	: 50ns (min)
BCKIN Rising Edge to LRCIN Edge	: t_{BL}	: 30ns (min)
LRCIN Edge to BCKIN Rising Edge	: t_{LB}	: 30ns (min)
DIN Set-up Time	: t_{DS}	: 30ns (min)
DIN Hold Time	: t_{DH}	: 30ns (min)

FIGURE 2. Audio Data Input Timing.



System Clock Pulse Width High	t_{SCKIH}	13ns (min)
System Clock Pulse Width Low	t_{SCKIL}	13ns (min)

FIGURE 3. System Clock Timing Requirements.

SYSTEM CLOCK

The system clock for PCM1744 must be either $256f_S$ or $384f_S$, where f_S is the audio sampling frequency (LRCIN), typically 32kHz, 44.1kHz, 48kHz, 88.2kHz or 96kHz. The system clock is used to operate the digital filter and the noise shaper. The system clock input (SCKI) is at pin 14. Timing conditions for SCKI are shown in Figure 3.

PCM1744 has a system clock detection circuit which automatically detects the frequency, either $256f_S$ or $384f_S$. The system clock should be synchronized with LRCIN (pin 1), but PCM1744 can compensate for phase differences. If the phase difference between LRCIN and system clock is greater than ±6 bit clocks (BCKIN), the synchronization is performed automatically. The analog outputs are forced to a bipolar zero state ($V_{CC}/2$) during the synchronization function. Table I shows the typical system clock frequency inputs for the PCM1744.

SAMPLING RATE (LRCIN)	SYSTEM CLOCK FREQUENCY (MHz)	
	$256f_S$	$384f_S$
32kHz	8.192	12.288
44.1kHz	11.2896	16.9340
48kHz	12.288	18.432
88.2kHz	22.5792	33.868
96kHz	24.576	36.864

TABLE I. System Clock Frequencies vs Sampling Rate.

TYPICAL CONNECTION DIAGRAM

Figure 4 illustrates the typical connection diagram for PCM1744 used in a stand-alone application.

INPUT DATA FORMAT

PCM1744 can accept input data a 24-bit I^2S format, as shown in Figure 1.

RESET

PCM1744 has an internal power-on reset circuit. The internal power-on reset initializes (resets) when the supply voltage V_{CC} > 2.2V (typ). The power-on reset has an initialization period equal to 1024 system clock periods after V_{CC} > 2.2V. During the initialization period, the outputs of the DAC are invalid, and the analog outputs are forced to $V_{CC}/2$. Figure 5 illustrates the power-on reset and reset-pin reset timing.

DE-EMPHASIS CONTROL

Pin 12 (DM) enables PCM1744's de-emphasis function. De-emphasis operates only at 44.1kHz.

DM	
0	De-emphasis OFF
1	De-emphasis ON (44.1kHz)

TABLE II. De-emphasis Control Selection.

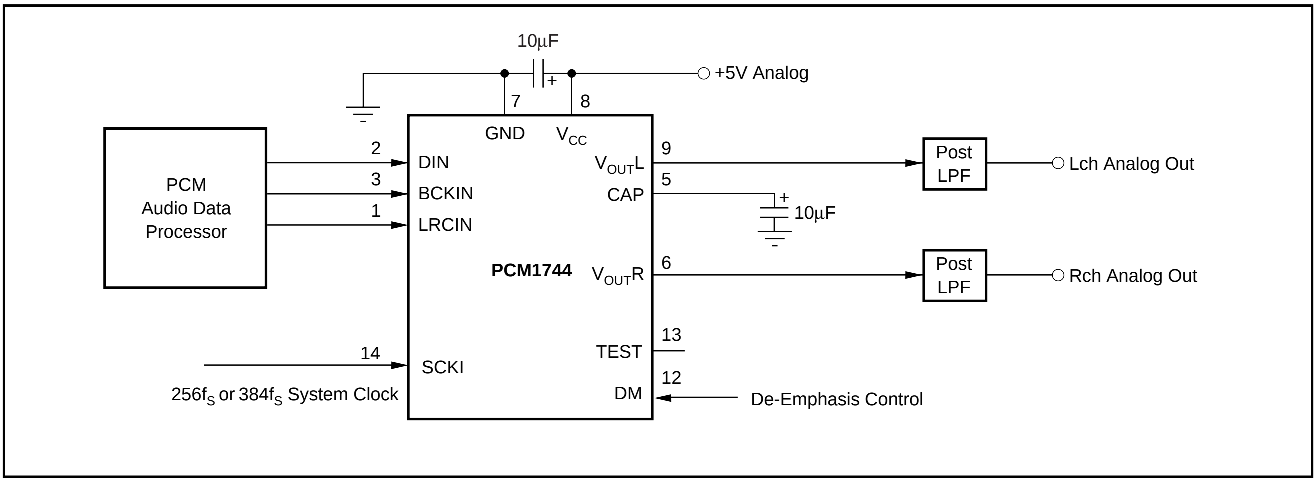


FIGURE 4. Typical Connection Diagram.

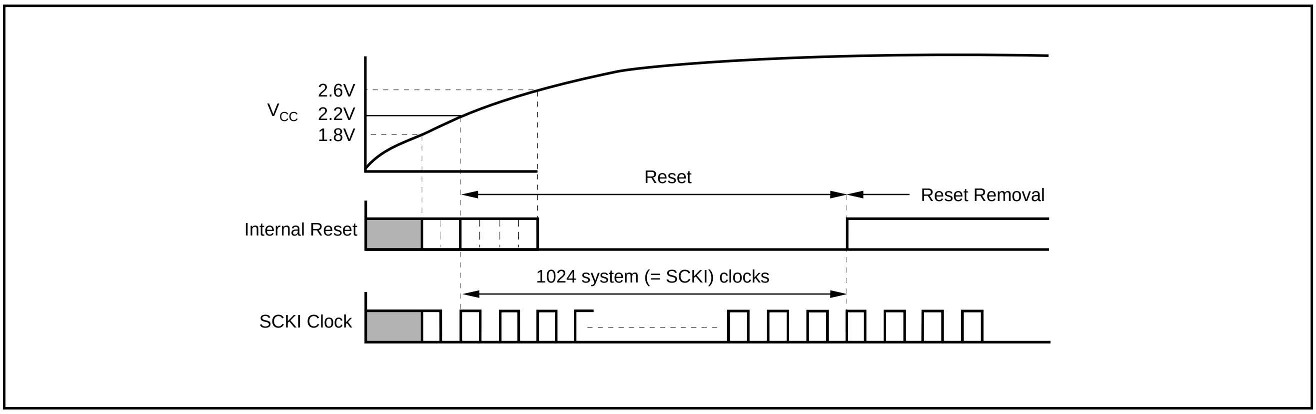


FIGURE 5. Internal Power-On Reset Timing.

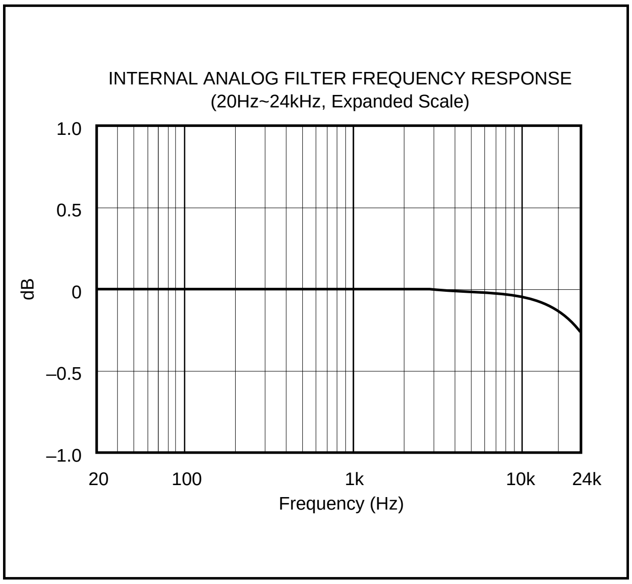


FIGURE 6. Low-Pass Filter Frequency Response.

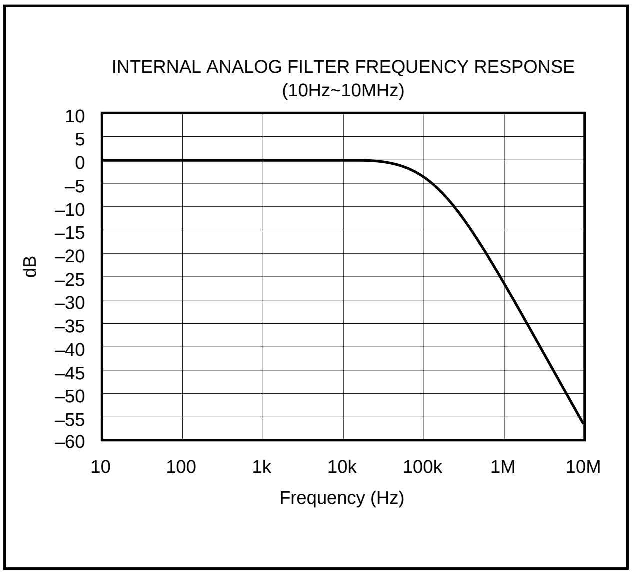


FIGURE 7. Low-Pass Filter Wideband Frequency Response.

APPLICATION CONSIDERATIONS

DELAY TIME

There is a finite delay time in delta-sigma converters. In A/D converters, this is commonly referred to as latency. For a delta-sigma D/A converter, delay time is determined by the order number of the FIR filter stage, and the chosen sampling rate. The following equation expresses the delay time of PCM1744:

$$T_D = 11.125 \text{ x } 1/f_S$$

$$\text{For } f_S = 44.1\text{kHz}, T_D = 11.125/44.1\text{kHz} = 251.4\mu\text{s}$$

Applications using data from a disc or tape source, such as CD audio, CD-Interactive, Video CD, DAT, Minidisc, etc., generally are not affected by delay time. For some professional applications such as broadcast audio for studios, it is important for total delay time to be less than 2ms.

OUTPUT FILTERING

For testing purposes all dynamic tests are done on the PCM1744 using a 20kHz low-pass filter. This filter limits the measured bandwidth for THD+N, etc. to 20kHz. Failure to use such a filter will result in higher THD+N and lower SNR and dynamic range readings than are found in the specifications. The low-pass filter removes out-of-band noise. Although it is not audible, it may affect dynamic specification numbers.

The performance of the internal low pass filter from DC to 24kHz is shown in Figure 6. The higher frequency roll-off of the filter is shown in Figure 7. If the user's application has the PCM1744 driving a wideband amplifier, it is recommended to use an external low-pass filter. A simple 3rd-order filter is shown in Figure 8. For some applications, a passive RC filter or 2nd-order filter may be adequate.

BYPASSING POWER SUPPLIES

The power supplies should be bypassed as close as possible to the unit. It is also recommended to include a 0.1µF ceramic capacitor in parallel with the 10µF tantalum bypass capacitor.

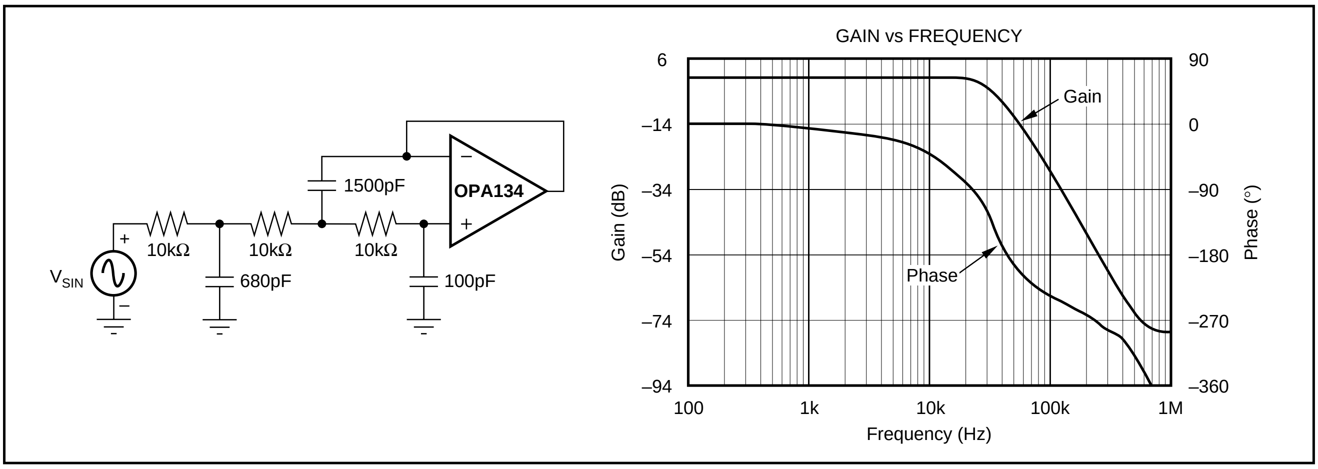


FIGURE 8. 3rd-Order LPF.

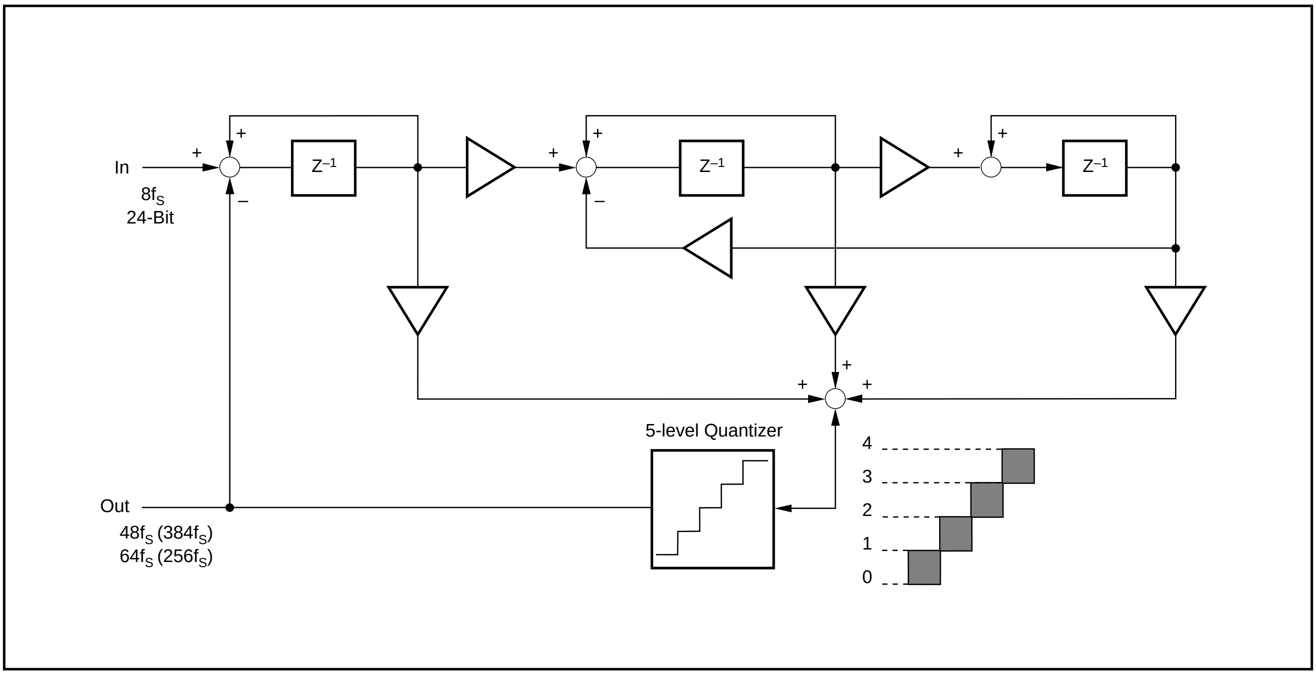


FIGURE 9. 5-Level ΔΣ Modulator Block Diagram.

THEORY OF OPERATION

The delta-sigma section of PCM1744 is based on a 5-level amplitude quantizer and a 3rd-order noise shaper. This section converts the oversampled input data to 5-level delta-sigma format. A block diagram of the 5-level delta-sigma modulator is shown in Figure 9. This 5-level delta-sigma modulator has the advantage of stability and clock jitter over the typical one-bit (2-level) delta-sigma modulator.

The combined oversampling rate of the delta-sigma modulator and the internal 8x interpolation filter is $96f_S$ for a $384f_S$ system clock, and $64f_S$ for a $256f_S$ system clock. The theoretical quantization noise performance of the 5-level delta-sigma modulator is shown in Figure 10.

Multi Level Delta Sigma

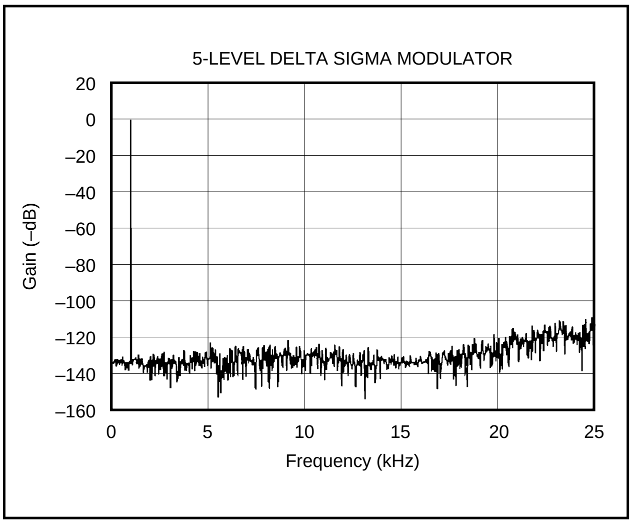


FIGURE 10. Quantization Noise Spectrum.