BURR - BROWN®

PCM2702

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16-Bit Stereo DIGITAL-TO-ANALOG CONVERTER with USB Interface

FEATURES

- **INTEGRATED USB INTERFACE:**
  - **Full-Speed Transceiver Supports 12Mbps Data Transfer.**
  - **Fully Compliant with the USB 1.0 Specification.**
  - **Adaptive Mode for Isochronous Transfer.**
  - **Self-Powered Device.**
- **ACCEPTS 16-BIT STEREO AND MONO USB AUDIO DATA STREAMS.**
- **ANALOG PERFORMANCE (V_{CC} = 5V):**
  - **Dynamic Range: 100dB (typ at 16-bit)**
  - **SNR: 105dB (typ)**
  - **THD+N: 0.002% (typ at 16-bit)**
  - **Full-Scale Output: 3.1Vp-p**
- **8X OVERSAMPLING DIGITAL FILTER:**
  - **Passband: 0.454f_S**
  - **Stopband: 0.546f_S**
  - **Passband Ripple: ±0.002dB**
  - **Stopband Attenuation: –82dB**
- **SAMPLING RATE (F_S): 32kHz, 44.1kHz, 48kHz**
- **ON-CHIP CLOCK GENERATOR WITH SINGLE 12MHz CLOCK SOURCE**
- **MULTI-FUNCTIONS:**
  - **Digital Attenuator: 0dB to –64dB, 1dB/step**
  - **Soft Mute**
  - **Zero Flag**
  - **Suspend Flag**
  - **Playback Flag**
- **DUAL POWER SUPPLIES:**
  - **+5V for Analog portion**
  - **+3.3V for Digital portion**
- **PACKAGE: SSOP-28**

APPLICATIONS

- **STAND-ALONE USB AUDIO SPEAKERS**
- **CRT/LCD INTEGRATED USB AUDIO SPEAKERS**
- **USB AUDIO AMPLIFIERS**
- **OTHER USB AUDIO APPLICATIONS**

DESCRIPTION

The PCM2702 is a single chip digital-to-analog converter offering two D/A output channels and an integrated USB 1.0 compliant interface controller. The newly developed SpAct™ (Sampling Period Adaptive Controlled Tracking) system recovers a stable, low-jitter clock for internal PLL and DAC operation from the USB interface audio data.

The PCM2702 is based upon Burr-Brown's Enhanced Multi-level Delta-Sigma Modulator, an 8x oversampling digital interpolation filter, and an analog output low-pass filter.

The PCM2702 can accept a 48kHz, 44.1kHz and 32kHz sampling rates, using either 16-bit stereo or monaural audio data. Digital attenuation and soft-mute features are included, and are controlled via USB audio class request.

Patents Pending.

SpAct™ is a trademark of Burr-Brown Corporation.

USB
UNIVERSAL SERIAL BUS

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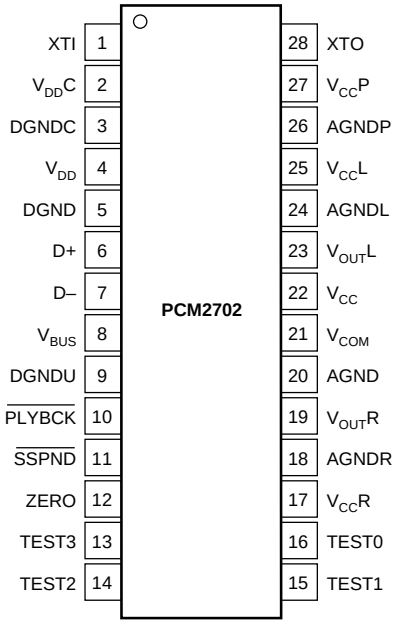
SPECIFICATIONS

At T_A = +25°C, V_{CC} = $V_{CC}L$ = $V_{CC}R$ = $V_{CC}P$ = 5.0V, V_{DD} = $V_{DD}C$ = 3.3V, f_S = 44.1MHz, signal frequency = 1kHz and 16-bit data, unless otherwise specified.

PARAMETER	CONDITIONS	PCM2702E MIN	PCM2702E TYP	PCM2702E MAX	UNITS
RESOLUTION			16		Bits
HOST INTERFACE			Supports USB revision 1.0, Full Speed		
DIGITAL FORMAT					
Audio Data Format			USB ISOCHRONOUS OUT		
Audio Data Bit Length			16		
Audio Data Channel			1, 2		
Sampling Frequency (f_S)			32, 44.1, 48		
DIGITAL INPUT/OUTPUT					
Input Logic Level V_{IH}(1)		2.0			VDC
V_{IL}(1)				0.8	VDC
V_{IH}(2)		0.7 V_{DD}			VDC
V_{IL}(2)				0.7 V_{DD}	VDC
Input Logic Current I_{IH}(1)	V_{IN} = V_{DD}		+65	+100	µA
I_{IL}(1)	V_{IN} = 0V			±10	µA
I_{IH}(2)	V_{IN} = V_{DD}			±10	µA
I_{IL}(2)	V_{IN} = 0V			±10	µA
Output Logic Level V_{OH}(3)	I_{OH} = –1mA	2.8			VDC
V_{OL}(3)	I_{OL} = +1mA			0.5	VDC
DYNAMIC PERFORMANCE(4)					
THD+N at V_{OUT} = 0dB			0.002	0.005	%
THD+N at V_{OUT} = –60dB			1.2		%
Dynamic Range	EIAJ, A-Weighted	96	100		dB
SIgnal-to-Noise Ratio	EIAJ, A-Weighted	100	105		dB
Channel Seperation		98	103		dB
DC ACCURACY					
Gain Error			±1.0	±3.0	% of FSR
Gain Mismatch, Channel-to-Channel			±1.0	±3.0	% of FSR
Bipolar Zero Error	V_{OUT} = 0.5 V_{CC} at BPZ		±30	±60	mV
ANALOG OUTPUT					
Output Voltage	Full-Scale(–0dB)		62% of V_{CC}		Vp-p
Center Voltage			50% of V_{CC}		VDC
Load Impedance	AC-Load	5			kΩ
DIGITAL FILTER PERFORMANCE					
Passband	±0.002dB			0.454f_S	
Passband	–3dB			0.490f_S	
Stopband		0.546f_S			
Passband Ripple				±0.002	dB
Stopband Attenuation	Stopband = 0.546f_S	–75			dB
Stopband Attenuation	Stopband = 0.567f_S	–82			dB
Delay Time			34/f_S	11	s
ANALOG FILTER PERFORMANCE					
Frequency Response	at 20kHz		≠0.02		dB
POWER SUPPLY REQUIREMENTS					
Voltage Range V_{DD}, $V_{DD}C$		+3.0	+3.3	+3.6	VDC
V_{CC}, $V_{CC}L$, $V_{CC}R$, $V_{CC}P$		+4.5	+5.0	+5.5	VDC
Supply Current I_{DD}	V_{DD} = $V_{DD}C$ = 3.3V		22	30	mA
I_{CC}	V_{CC} = $V_{CC}L$ = $V_{CC}R$ = $V_{CC}P$ = 5.0V		18	25	mA
Power Dissipation	V_{DD} = $V_{DD}C$ = 3.3V, and V_{CC} = $V_{CC}L$ = $V_{CC}R$ = $V_{CC}P$ = 5.0V		165	225	mW
TEMPERATURE RANGE					
Operation Temperature		0		70	°C
Storage Temperature		–55		+125	°C
Thermal Resistance, θ_{JA}	SSOP-28		100		°C/W

NOTES: (1) Pins 8, 13, 14, 15, 16: V_{BUS}, TEST3 TEST2 TEST1, TEST0. (2) Pin1: XTI. (3) Pins 10, 11, 12, 28: PLYBCK, SSPND, ZERO, XTO. (4) The dynamic performance is based upon ideal host signal quality, and may vary according to the system. Dynamic performance specifications are tested using a Shibasoku #725 THD Meter with 400Hz HPF, 30kHz LPF, Average Mode, and 20kHz Bandwidth limiting. The load connected to the analog output is 5kΩ, or larger, via AC coupling.

Top View **SSOP**



PIN	NAME	TYPE	DESCRIPTIONS
1	XTI	IN	Crystal Oscillator Input.(1)
2	$V_{DD}C$	—	Digital Power Supply for Clock Generator, +3.3V.
3	DGNDC	—	Digital Ground for Clock Generator.
4	V_{DD}	—	Digital Power Supply, +3.3V.
5	DGND	—	Digital Ground.
6	D+	IN/OUT	USB Differential Input/Output Plus.
7	D–	IN/OUT	USB Differential Input/Output Minus.
8	V_{BUS}	IN	USB Bus Power (this pin NEVER consumes USB bus power).(2)
9	DGNDU	—	Digital Ground for USB Transceiver.
10	$\overline{PLYBCK}$	OUT	Playback flag, active LOW (LOW: playback, HIGH: idle).
11	$\overline{SSPND}$	OUT	Suspend flag, active LOW (LOW: suspend, HIGH: operational).
12	ZERO	OUT	Zero flag (LOW: Normal, HIGH: ZERO.)
13	TEST3	IN	Test pin 3. Connect to digital ground.(2)
14	TEST2	IN	Test pin 2. Connect to digital ground.(2)
15	TEST1	IN	Test pin 1. Connect to digital ground.(2)
16	TEST0	IN	Test pin 0. Connect to digital ground.(2)
17	$V_{CC}R$	—	Analog Supply for R-channel, +5V.
18	AGNDR	—	Analog Ground for R-channel.
19	$V_{OUT}R$	OUT	Analog Output for R-channel.
20	AGND	—	Analog Ground.
21	V_{COM}	—	DC Common-Mode Voltage for DAC.
22	V_{CC}	—	Analog Supply, +5V.
23	$V_{OUT}L$	OUT	Analog Output for L-channel.
24	AGNDL	—	Analog Ground for L-channel.
25	$V_{CC}L$	—	Analog Supply for L-channel, +5V.
26	AGNDP	—	Analog Ground for PLL.
27	$V_{CC}P$	—	Analog Supply for PLL, +5V.
28	XTO	OUT	Crystal Oscillator Output.

NOTES: (1) 3.3 V tolerant. (2) Schmitt trigger input with internal pull-down, 5V tolerant.

ABSOLUTE MAXIMUM RATINGS(1)

Supply Voltage(2)	+6.5V
Supply Voltage(3)	+4.0V
Supply Voltage Differences(4)	±0.1V
Supply Voltage Differences(5)	±0.1V
Ground Voltage Differences(6)	±0.1V
Digital Input Voltage(7)	–0.3V to V_{DD} + 0.3V
Digital Input Voltage(8)	–0.3V to 6.5V
Analog Input Voltage	–0.3V to V_{CC} + 0.3V
Input Current (any pins except supplies)	±10mA
Operating Temperature	–25°C to +85°C
Storage Temperature	–55°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering, 5s)	+260°C
Package Temperature (IR reflow, peak, 10s)	+235°C

NOTES: (1) Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability. (2) V_{CC}, $V_{CC}L$, $V_{CC}R$, $V_{DD}P$. (3) V_{DD}, $V_{DD}C$. (4) Among V_{CC}, $V_{CC}L$, $V_{CC}R$, $V_{CC}P$. (5) Among V_{DD}, $V_{DD}C$. (6) Among AGND, AGNDL, AGNDR, AGNDP, DGND, DGNDC, and DGNDU. (7) XTI, D+, D–, $\overline{PLYBCK}$, $\overline{SSPND}$, ZERO, XTO. (8) V_{BUS}, TEST#, TEST2, TEST1, TEST0.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

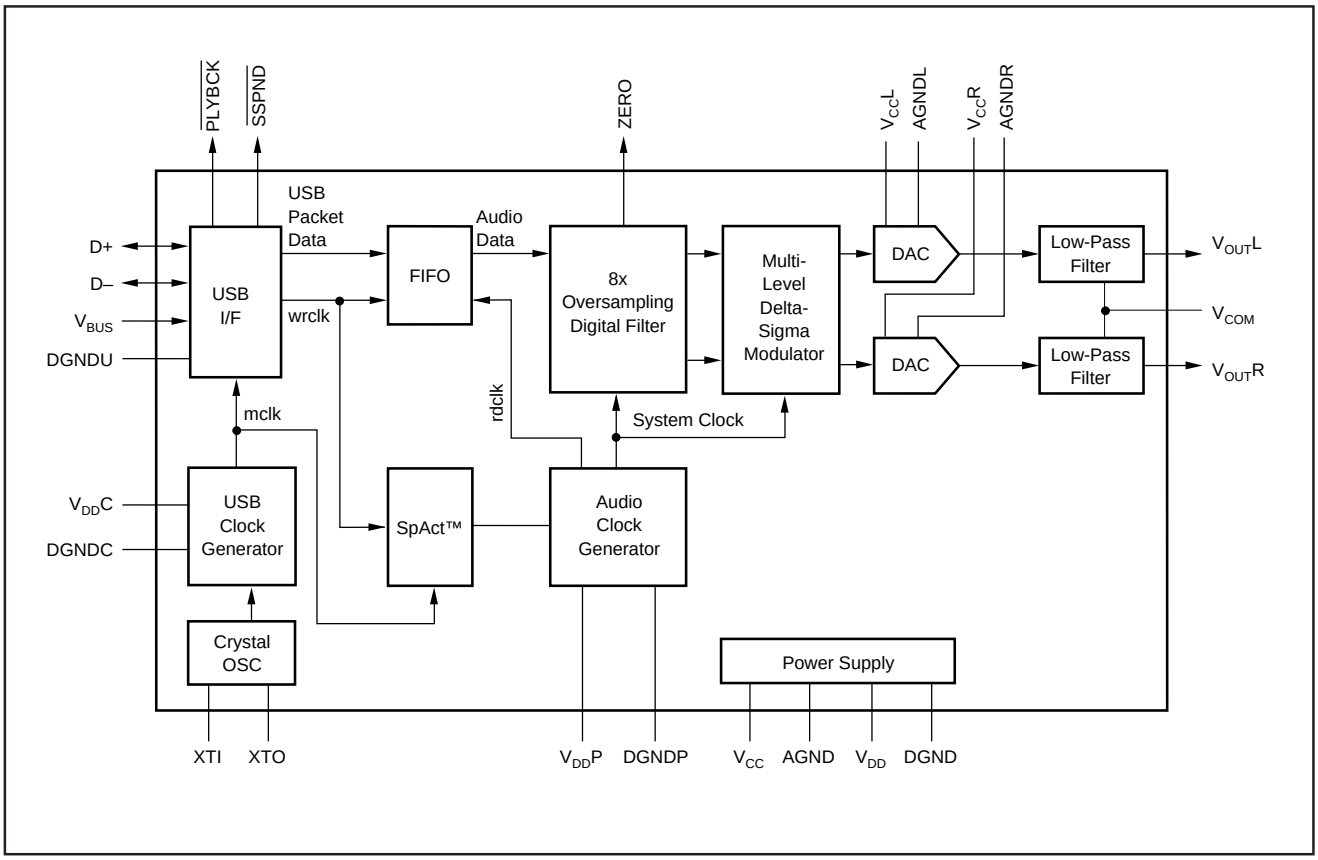
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER(1)	TRANSPORT MEDIA
PCM2702E	SSOP-28	324	0°C to +70°C	PCM2702E	PCM2702E	Rails
"	"	"	"	"	PCM2702E/2K	Tape and Reel

NOTE: (1) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /2K indicates 2000 devices per reel). Ordering 2000 pieces of "PCM2702E/2K" will get a single 2000-piece Tape and Reel.

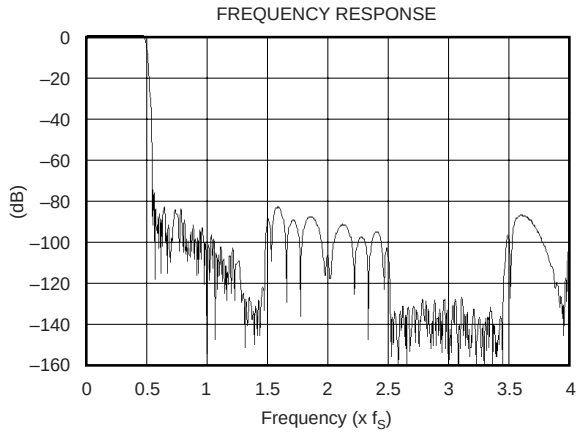
BLOCK DIAGRAM

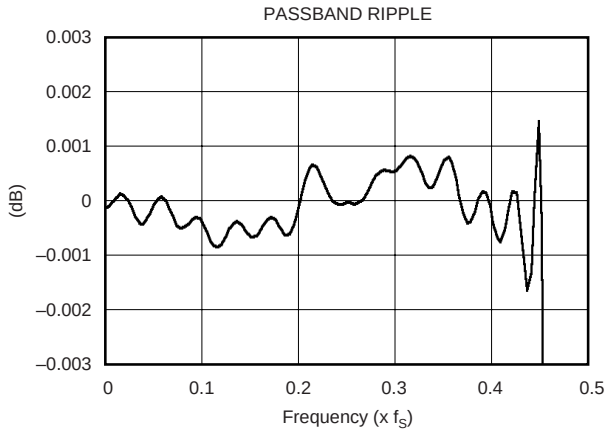


TYPICAL PERFORMANCE CURVES

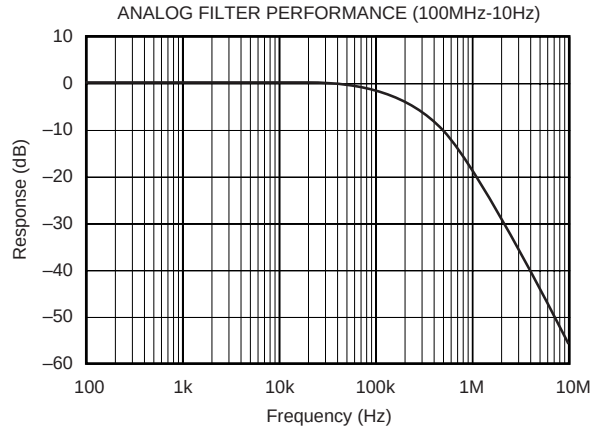
All specifications at T_A = +25°C, V_{CC} = $V_{CC}L$ = $V_{CC}R$ = $V_{CC}P$ = 5.0V, V_{DD} = $V_{DD}C$ = 3.3V, f_S = 44.1MHz, signal frequency = 1kHz and 16-bit data, unless otherwise specified.

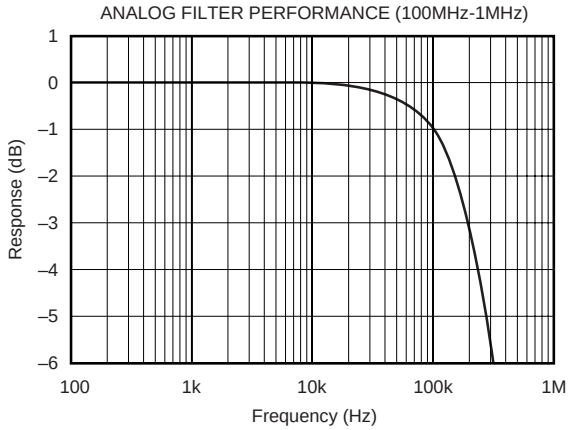
DIGITAL FILTER PERFORMANCE





ANALOG FILTER PERFORMANCE



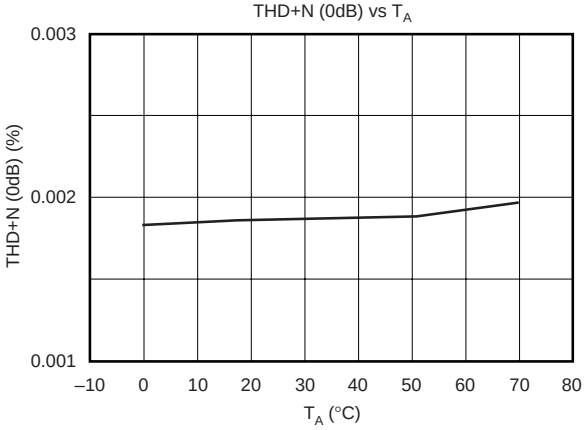


TYPICAL PERFORMANCE CURVES (Cont.)

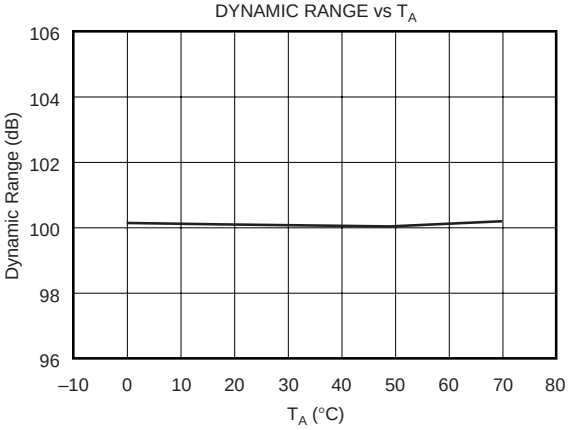
All specifications at T_A = +25°C, V_{CC} = $V_{CC}L$ = $V_{CC}R$ = $V_{CC}P$ = 5.0V, V_{DD} = $V_{DD}C$ = 3.3V, f_S = 44.1MHz, signal frequency = 1kHz and 16-bit data, unless otherwise specified.

ANALOG DYNAMIC PERFORMANCE

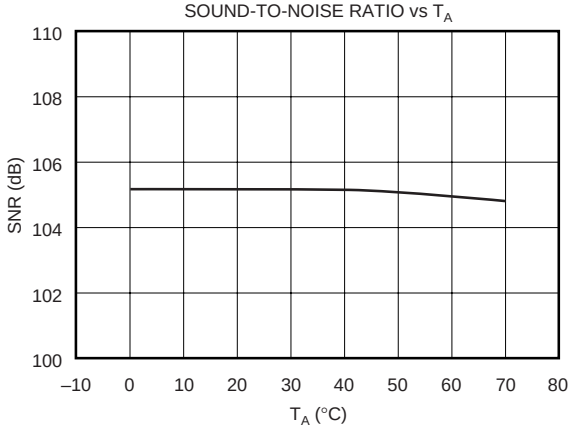
THD+N (0dB) vs T_A



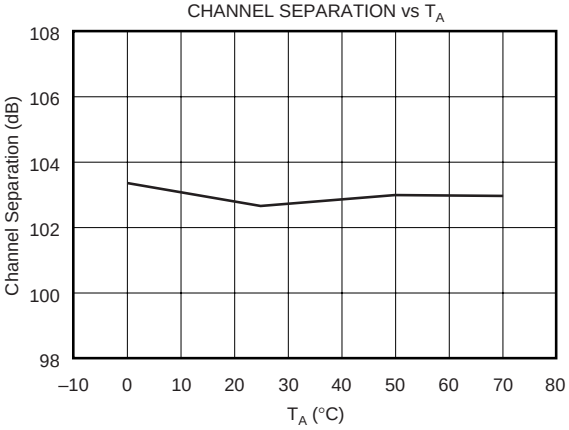
DYNAMIC RANGE vs T_A



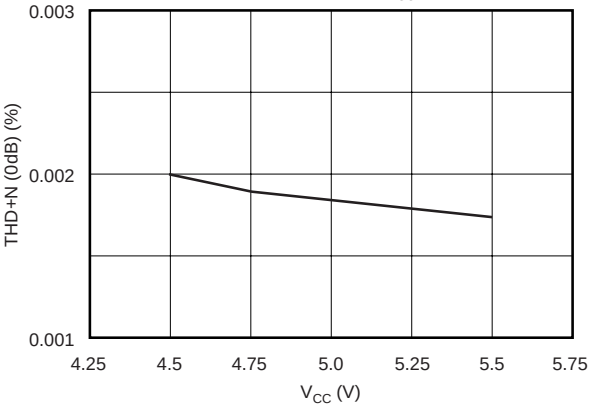
SOUND-TO-NOISE RATIO vs T_A



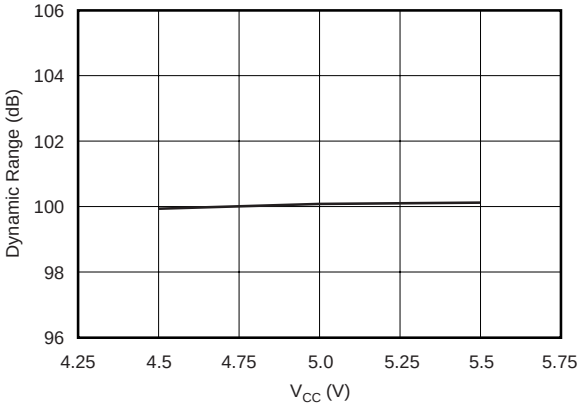
CHANNEL SEPARATION vs T_A



THD+N (0dB) vs V_{CC}



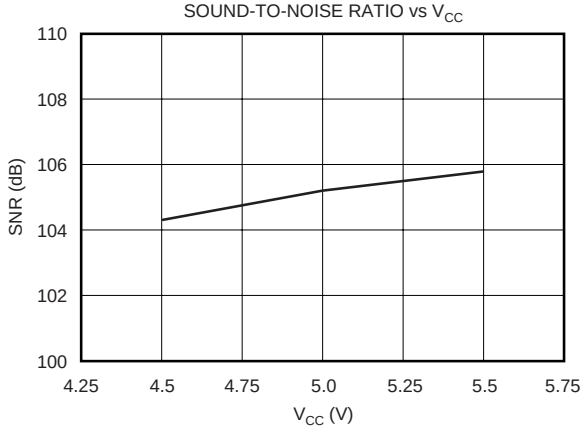
DYNAMIC RANGE vs V_{CC}



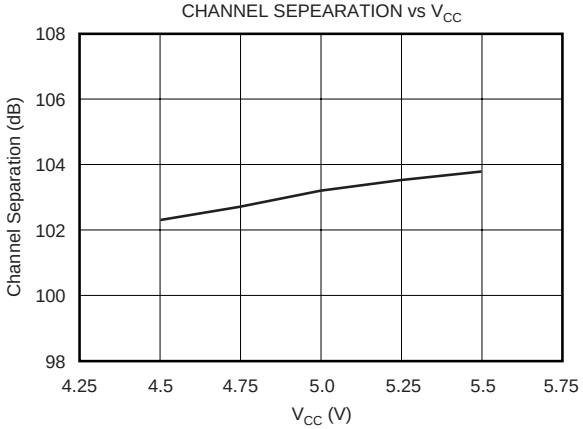
TYPICAL PERFORMANCE CURVES (Cont.)

All specifications at T_A = +25°C, V_{CC} = $V_{CC}L$ = $V_{CC}R$ = $V_{CC}P$ = 5.0V, V_{DD} = $V_{DD}C$ = 3.3V, f_S = 44.1MHz, signal frequency = 1kHz and 16-bit data, unless otherwise specified.

SOUND-TO-NOISE RATIO vs V_{CC}



CHANNEL SEPEARATION vs V_{CC}



THEORY OF OPERATION

USB INTERFACE

The description of the USB interface complies with Universal Serial Bus specification Rev. 1.0.

Control and audio data are both transferred to the PCM2702 via D+ (pin 6) and D– (pin 7). All data to/from the PCM2702 are transferred at full-speed. V_{BUS} (pin 8) and DGNDU (pin 9) are also connected to the USB bus. V_{BUS} (pin 8) never consumes USB bus power, it is used only for detecting the connection of the USB bus. The following information is provided in the device descriptor.

USB Revision	1.0
Device Class	0x00 (device defined interface level)
Device Subclass	0x00 (not specified)
Device Protocol	0x00 (not specified)
Max Packet Size for Endpoint 0	8 byte
Vendor ID	0x08BB
Device ID	0x2702
Release	1.0

TABLE I. Device Definition.

DEVICE CONFIGURATION

Figure 1 illustrates USB audio function topology. The PCM2702 has two interfaces. Each interface is constructed by some alternative setting. Interface #0 has one alternative setting. Alternative setting #0 describes the standard audio control interface. The audio control interface is constructed by a terminal. The PCM2702 has the following three terminals.

- Input Terminal (IT)
- Output Terminal (OT)
- Feature Unit (FU)

The Input Terminal is defined as “USB stream” (terminal type 0x0101). The Input Terminal can accept 2-channel audio streams comprised of left and right channel data. The Output Terminal is defined as a “speaker” (terminal type 0x0301). The Feature Unit supports the following sound control features.

- Volume Control
- Mute Control

The built-in digital volume controller can be manipulated by an audio class specific request from 0.0dB to –64.0dB in steps of 1.0dB. Each channel can be set independently. The master volume control is also supported. The built-in digital mute controller can be manipulated by an audio class specific request. A master mute-control request is acceptable. A request to an individual channel will be stalled and ignored.

Interface #1 has three alternative settings. Alternative setting #0 is the Zero Bandwidth setting. Alternative setting #1 is the 16-Bit Stereo setting, and is an operational setting. Alternative setting #2 is the 16-Bit Monaural setting, and is also an operational setting. The PCM2702 has the following two endpoints.

- Control Endpoint (EP #0)
- Isochronous Audio Data Stream Endpoint (EP #2)

The Control Endpoint is a default endpoint and is used to control all functions of the PCM2702 by the standard USB request and the USB audio class specific request. The Isochronous Audio Data Stream Endpoint is an audio sink endpoint, which receives the PCM audio data, and accepts the adaptive transfer mode.

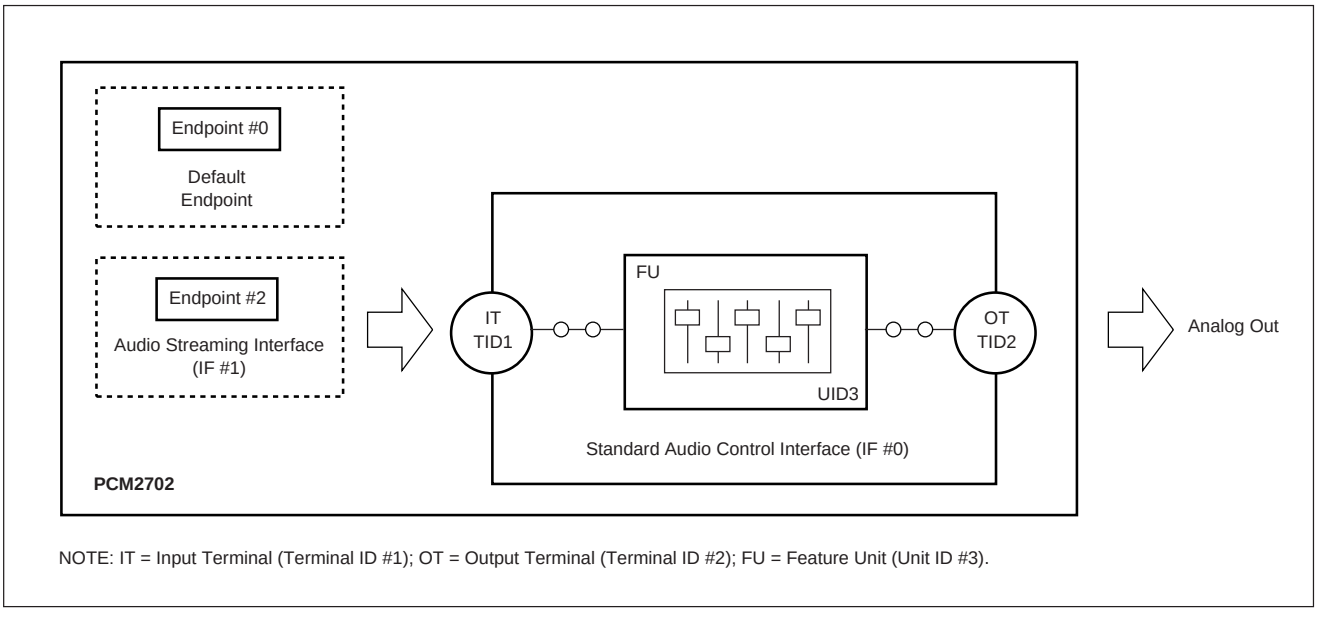


FIGURE 1. USB Audio Function Topology.

CLOCK AND RESET

The PCM2702 requires a 12MHz (±500ppm) clock for USB and audio functions, which may be generated by an on-chip crystal oscillator with external 12MHz crystal resonator, or supplied by an external clock applied at XTI (pin1). The 12MHz crystal resonator must be connected to XTI (pin 1) and XTO (pin 28), along with a 1MΩ resistor and two small capacitors (value is dependent upon the specified load capacitance of the crystal resonator). If an external clock is used, the clock must be supplied at XTI, and XTO must be left open. The clock signal applied at XTI must be +3.3V logic level, as this input is not +5V tolerant. Figures 2 and 3 illustrate the circuit connections required for crystal and external clock options.

The PCM2702 includes an internal power-on reset circuit, which automatically initializes digital logic when V_{DD} exceeds 2.0V typical (range: 1.6V to 2.4V). Initialization requires approximately 350µs for completion. The V_{DD} supply must rise to 2.0V within 10ms for proper power-on sequence operation.

INTERFACE SEQUENCE

Power-on, Attach, and Playback Sequence

The PCM2702 is ready for setup when the reset sequence has finished and the USB bus is connected. After connection is established, the PCM2702 is ready to accept USB audio data. While waiting for audio data (idle state), the analog outputs are set to bipolar zero (BPZ) and the zero flag, ZERO (pin 12), is set to HIGH.

When receiving the audio data, the PCM2702 stores the first audio packet, which contains 1ms of audio data, into an internal storage buffer. The PCM2702 starts playing the audio data upon detection of the Start of Frame (SOF) packet.

See Figures 4 and 5 for the normal operation sequence.

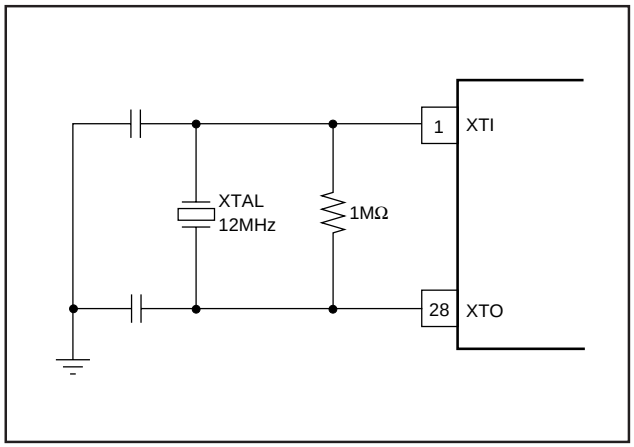


FIGURE 2. 12MHz Crystal Resonator Connection.

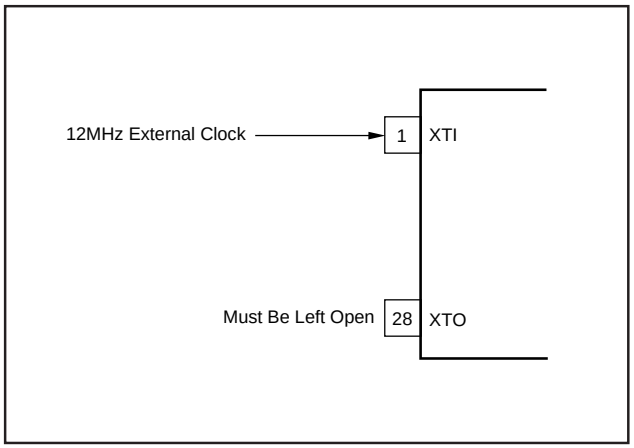


FIGURE 3. External 12MHz Clock Input Connection.

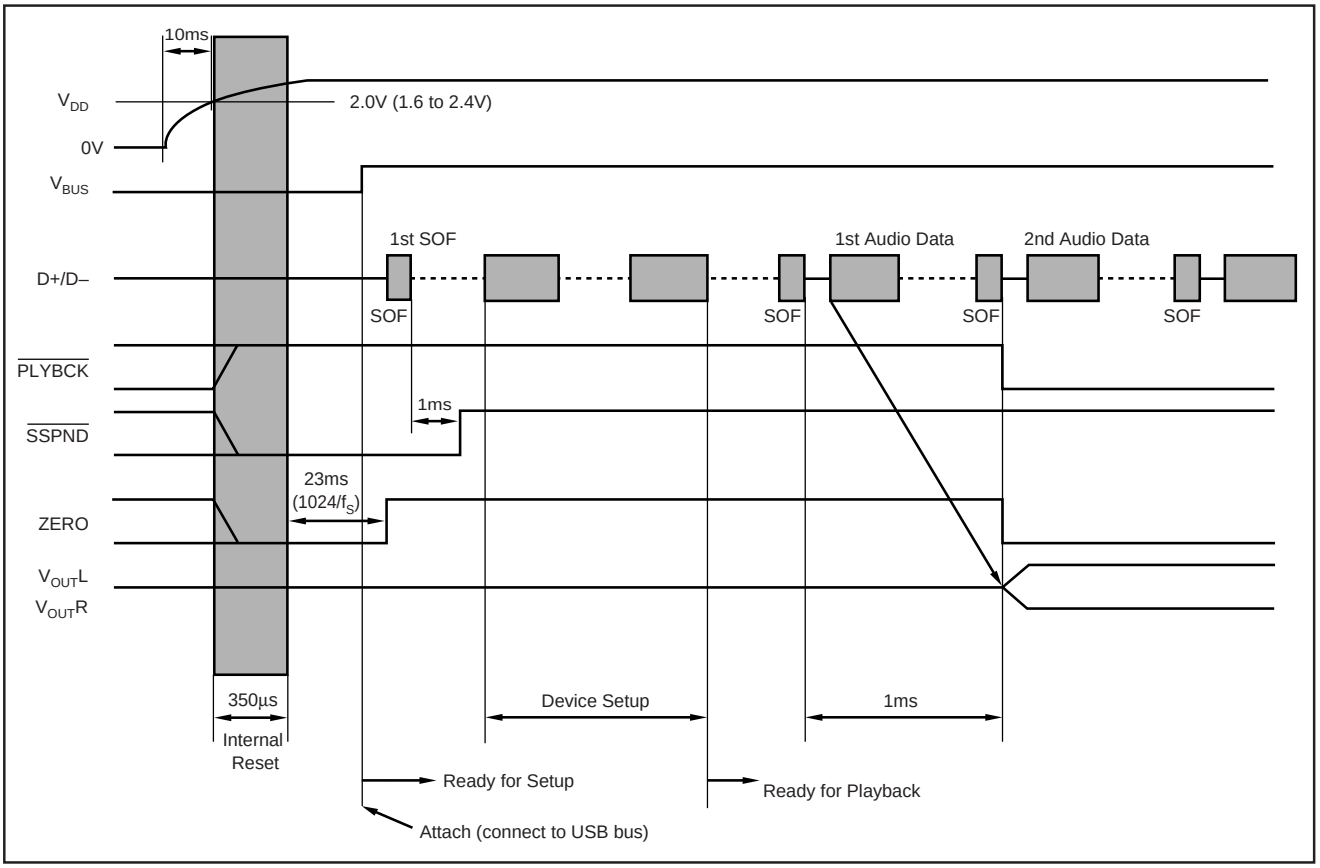


FIGURE 4. Connecting the PCM2702 to the USB Bus After Power-On.

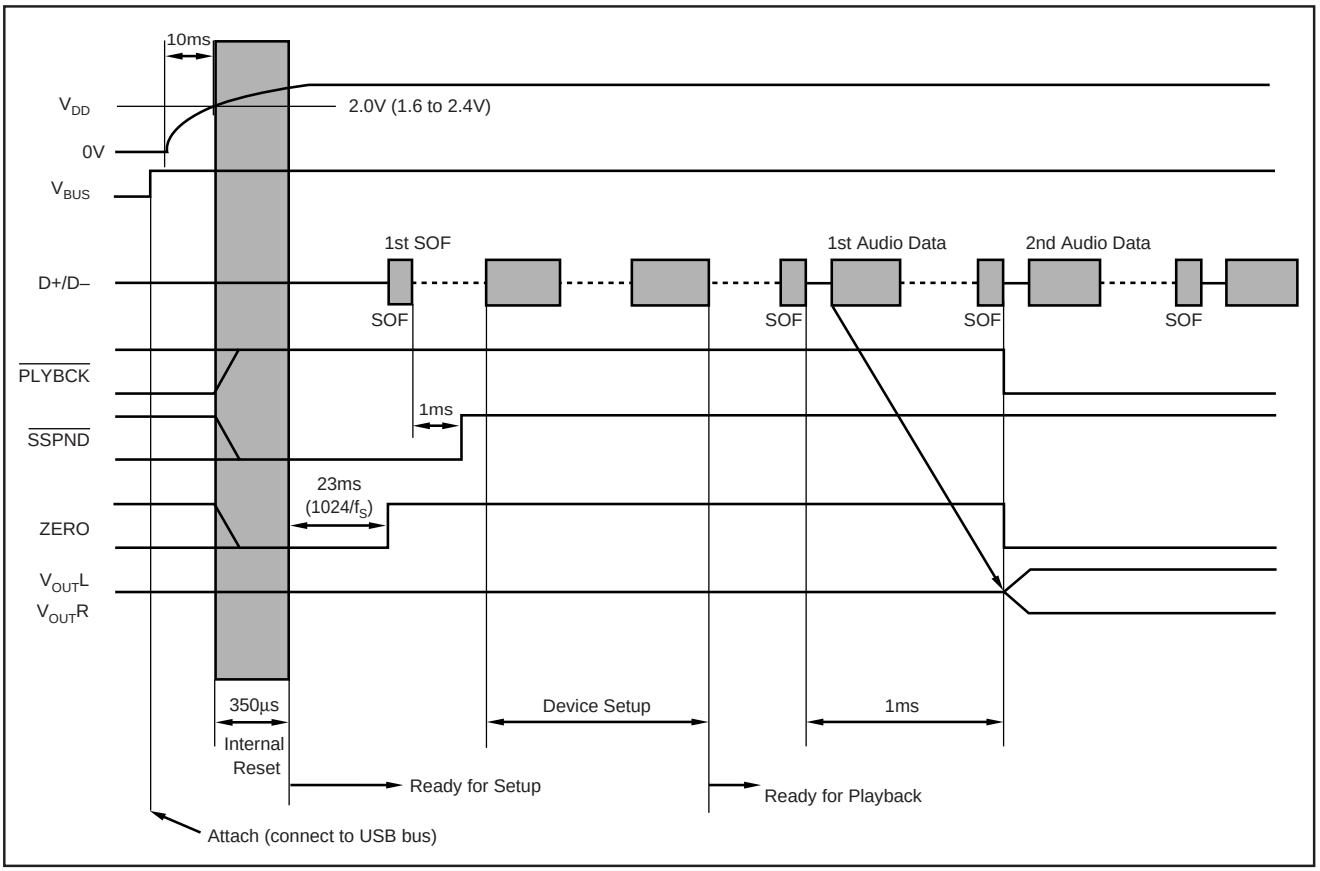


FIGURE 5. Connecting the PCM2702 to the USB Bus Prior to Power-On.

Play, Stop, and Detach sequence

When host finishes or aborts audio playback, the PCM2702 will stop playing after the last transmitted audio data has been received. Figure 6 shows the operation sequence for play, stop, and detach.

$\overline{\text{PLYBCK}}$, $\overline{\text{SSPND}}$, AND ZERO FLAG

$\overline{\text{PLYBCK}}$, $\overline{\text{SSPND}}$, and Zero flag in Figures 4, 5, and 6 are defined as follows.

$\overline{\text{PLYBCK}}$—while PCM audio input data is playing back, $\overline{\text{PLYBCK}}$ (pin 10) is switched LOW.

$\overline{\text{SSPND}}$—upon detection of a suspend state on the USB port, $\overline{\text{SSPND}}$ (pin 11) is switched LOW.

ZERO—if the PCM audio input data is continuously zero for 1024 sampling periods ($1/f_S$), ZERO (pin12) is switched to HIGH.

TEST PINS

The PCM2702 has four test pins—TEST0 (pin 16), TEST1 (pin 15), TEST2 (pin 14), and TEST3 (pin 13)—which are used solely for testing at the factory. These pins must be connected to a digital ground for proper operation.

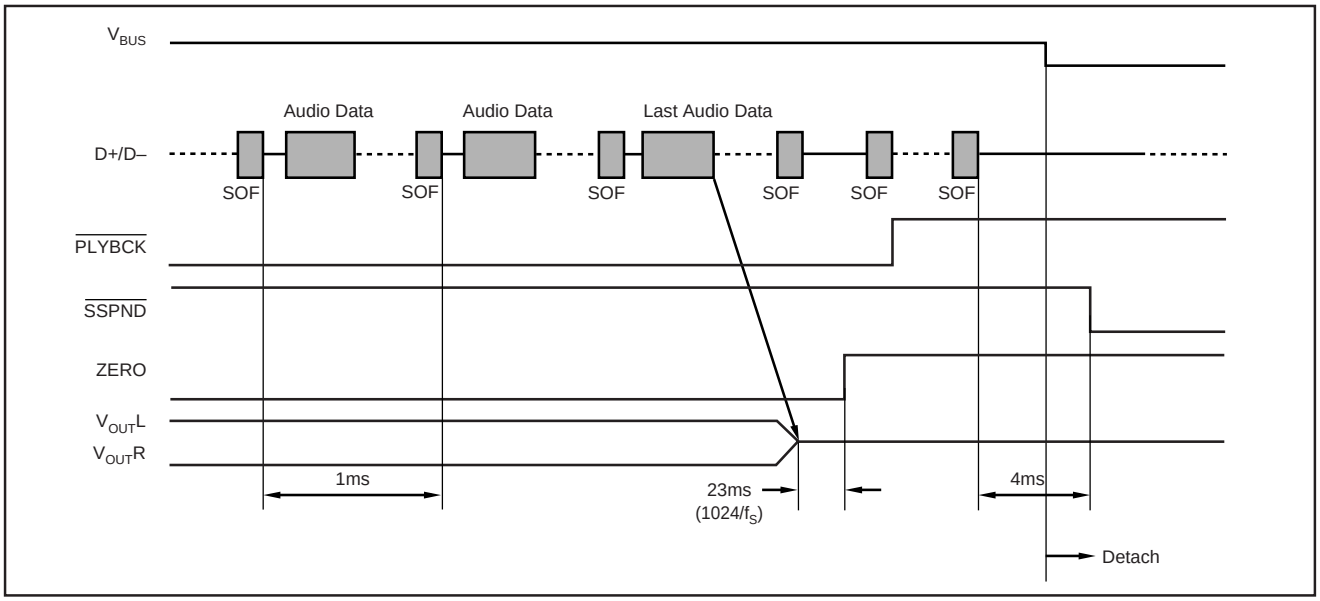
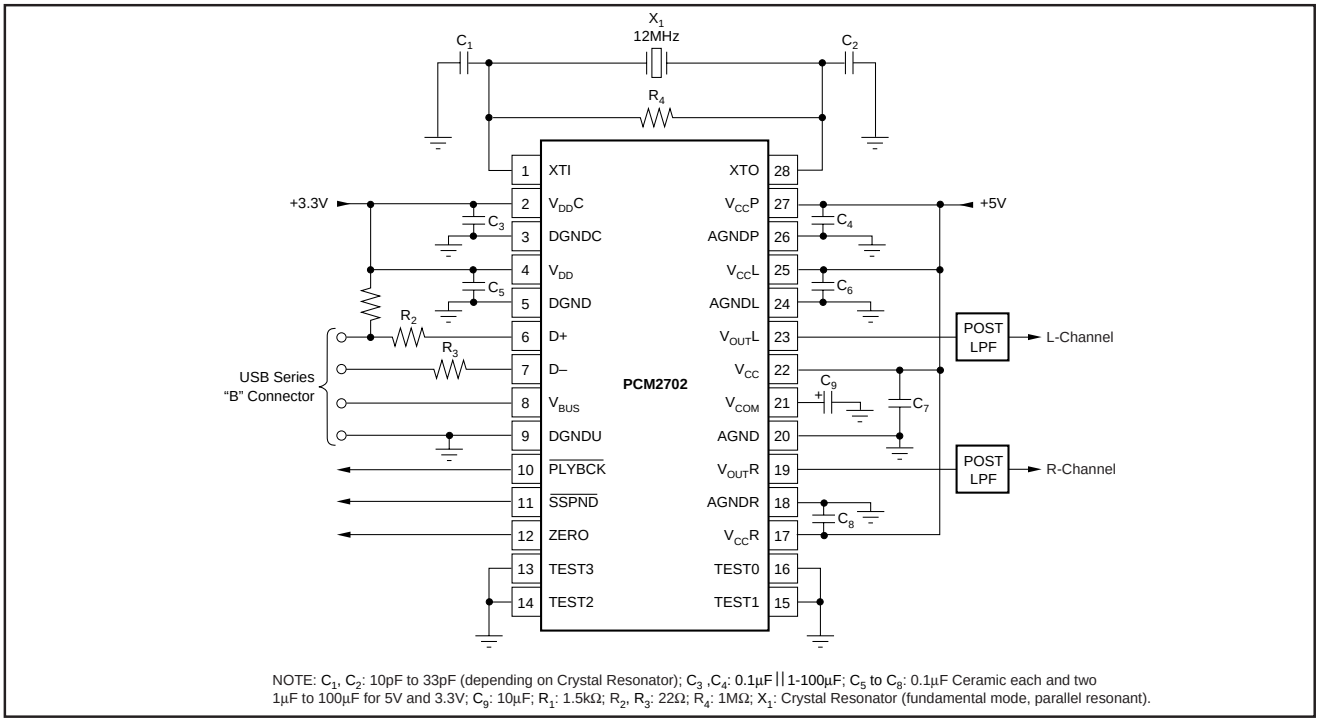


FIGURE 6. Play, Stop, and Detach.



NOTE: C_1, C_2: 10pF to 33pF (depending on Crystal Resonator); C_3 ,C_4: 0.1µF || 1-100µF; C_5 to C_8: 0.1µF Ceramic each and two 1µF to 100µF for 5V and 3.3V; C_9: 10µF; R_1: 1.5kΩ; R_2, R_3: 22Ω; R_4: 1MΩ; X_1: Crystal Resonator (fundamental mode, parallel resonant).

FIGURE 7. Typical Connection Diagram.