BURR - BROWN®

VSP2000

SpeedPLUS™ CCD SIGNAL PROCESSOR FOR DIGITAL CAMERAS

FEATURES

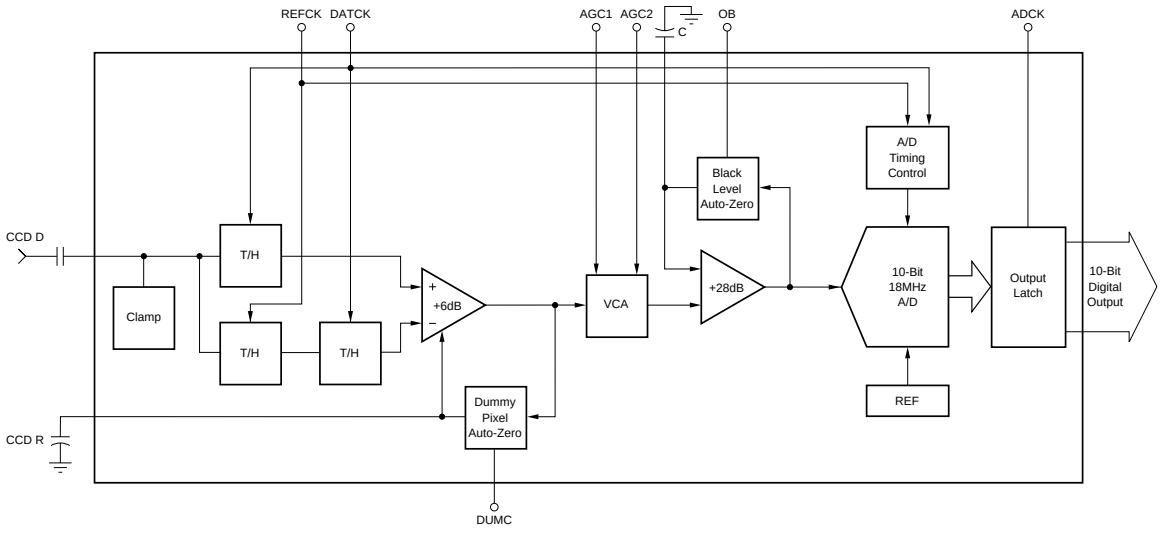
- **CCD SIGNAL PROCESSING**
  Correlated Double Sampling
  Black Level Clamping
  0 to +34dB Gain Ranging
  High SNR: 53dB
- **10-BIT A/D CONVERSION**
  Up to 18MHz Conversion Rate
  No Missing Codes
- **PORTABLE OPERATION**
  Low Voltage: Down to 2.7V
  Low Power: 150mW at 2.7V

APPLICATIONS

- **VIDEO CAMERAS**
- **DIGITAL STILL CAMERAS**
- **PC CAMERAS**
- **SECURITY CAMERAS**

DESCRIPTION

The VSP2000 is a complete digital camera IC, providing signal conditioning and 10-bit analog-to-digital conversion for the output of a CCD array. The primary CCD channel provides correlated double sampling to extract the video information from the pixels, 0dB to +34dB gain range with analog control for varying illumination conditions, and black level clamping for an accurate black reference. The stable gain control is linear in dB. Additionally, the black level is quickly recovered after gain changes. The VSP2000 is available in a 48-lead LQFP package and operates from a single +3V supply.



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SPECIFICATIONS

At T_A = +25°C, AV_{DD} = AV_{DD2} = +3.0V, DV_{DD} = DV_{DD1} = DRV_{DD} = +3.0V, unless otherwise specified.

PARAMETER	CONDITIONS	VSP2000 MIN	VSP2000 TYP	VSP2000 MAX	UNITS
DIGITAL INPUT					
Logic Family			CMOS		
Logic Levels	Logic HI	$+V_{DD}/2$		$+V_{DD}$	V
	Logic LO	0		+0.4	V
Logic Currents	Logic HI, V_{IN} = $+V_{DD}$			10	µA
	Logic LO, V_{IN} = 0V			10	µA
A/D Clock Duty Cycle			50		%
DIGITAL OUTPUT					
Logic Family			CMOS		
Logic Levels	Logic HI, C_l = 10pF	$+V_{DD}$ –0.5		$+V_{DD}$	V
	Logic LO, C_l = 10pF	0		+0.4	V
TRANSFER CHARACTERISTICS					
Resolution			10		Bit
Differential Non-Linearity			±0.4		LSB
Integral Non-Linearity			±2.0		LSB
No Missing Codes			Guaranteed		
Signal Settling Time	Black to Full Scale Change to 1/4 LSB into ADS			110	ns
Conversion Rate		500kHz		18	MHz
Data Latency			5.5		Clocks
Signal-to-Noise Ratio[1]	Grounded Input Cap, VCA Gain Max		53		dB
Black Clamp Level			32		LSB
CDS					
Data Settling Time to +0.1% for FS Change with R_S = 40	From Leading Edge of DATCK		11		ns
Input Capacitance	DATCK Low		20		pF
Input Time Constant			300		ps
Data Full Scale Input	After AC Coupling Cap	600			mV
INPUT CLAMP					
Clamp on Resistance			3.3		kΩ
Clamp Level			1		V
VCA CHARACTERISTICS					
Gain Control Voltage Range		0.3		2.4	V
Gain at Max Control Voltage		32	34		dB
Gain Control Linearity			±1.0		dB
Gain Control Settling Time			10		µs
Transfer Function			18		dB/V
POWER SUPPLY					
Rated Voltage		+2.7	+3.0	+3.3	V
Current, Quiescent	3V Supply		60		mA
Power Dissipation	3V Supply		180		mW
	2.7V Supply		150		mW
Power Down Mode			24		mW
TEMPERATURE RANGE					
Specified Range	Ambient	–25		+85	°C
Thermal Resistance, θ_{JA}					
48-Lead LQFP			100		°C/W

NOTE: (1) SNR = 20log (Full Scale Voltage/rms Noise).

ABSOLUTE MAXIMUM RATINGS

$+V_S$	+6V
Analog Input	(0 –0.3V) to ($+V_S$ +0.3V)
Logic Input	(0 –0.3V) to ($+V_S$ +0.3V)
Case Temperature	+100°C
Junction Temperature	+150°C
Storage Temperature	+150°C

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER(1)	TEMPERATURE RANGE
VSP2000	48-Lead LQFP	340	–40°C to +85°C

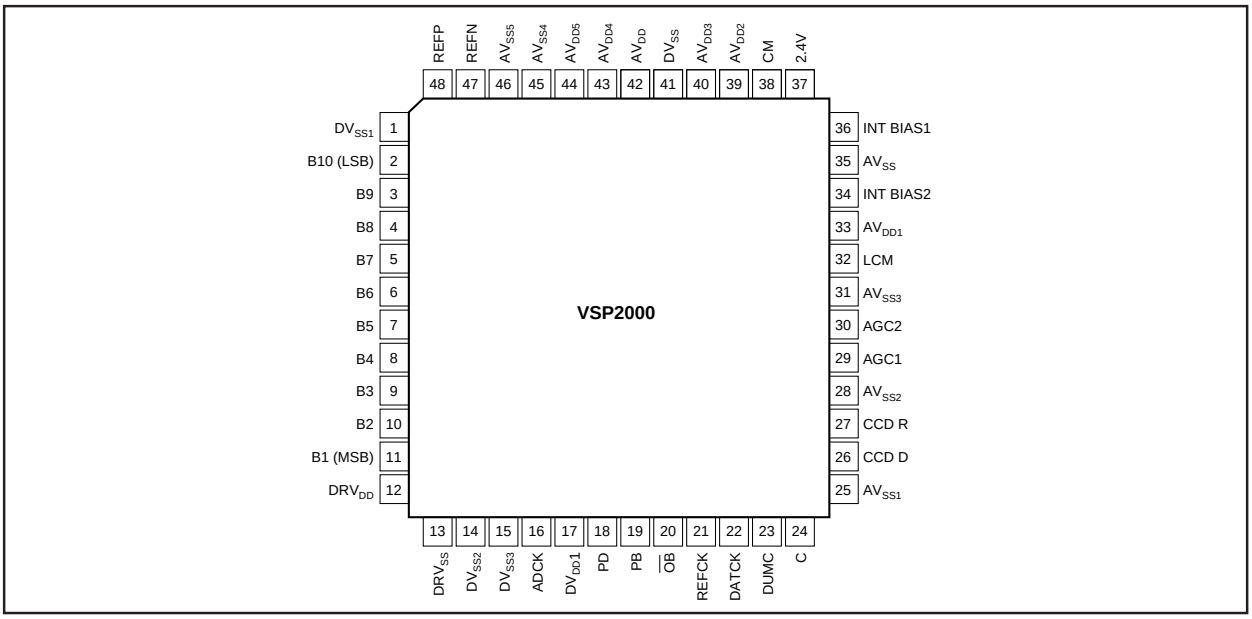
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PIN CONFIGURATION

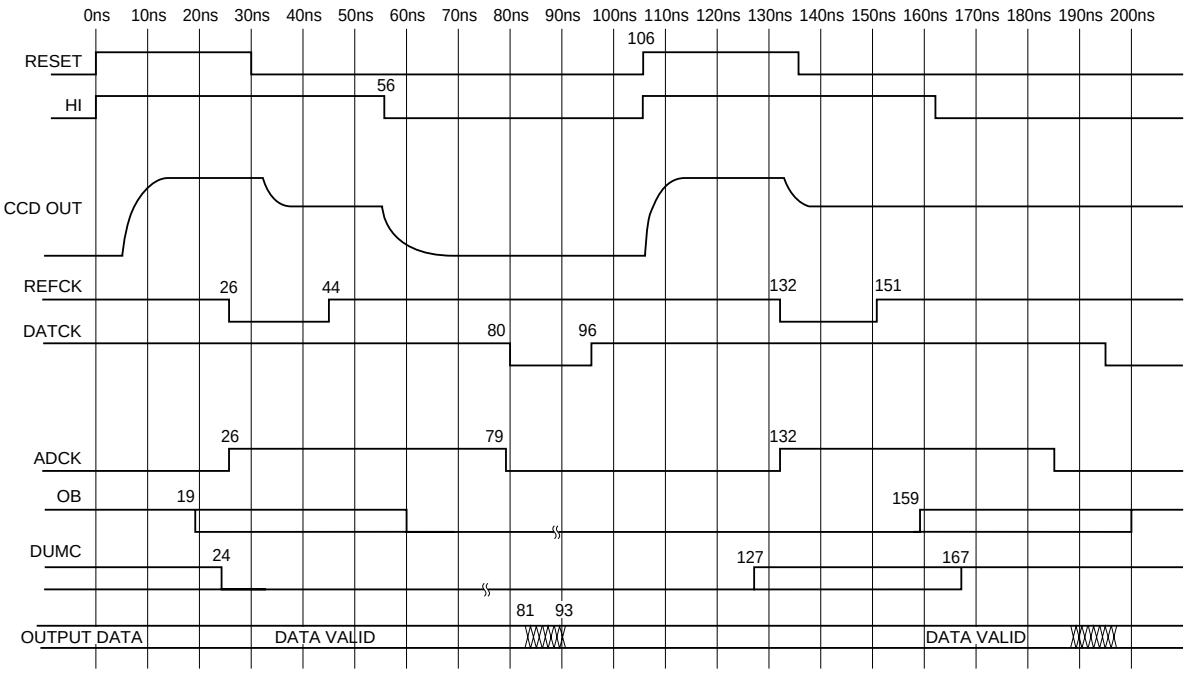


PIN DESCRIPTIONS

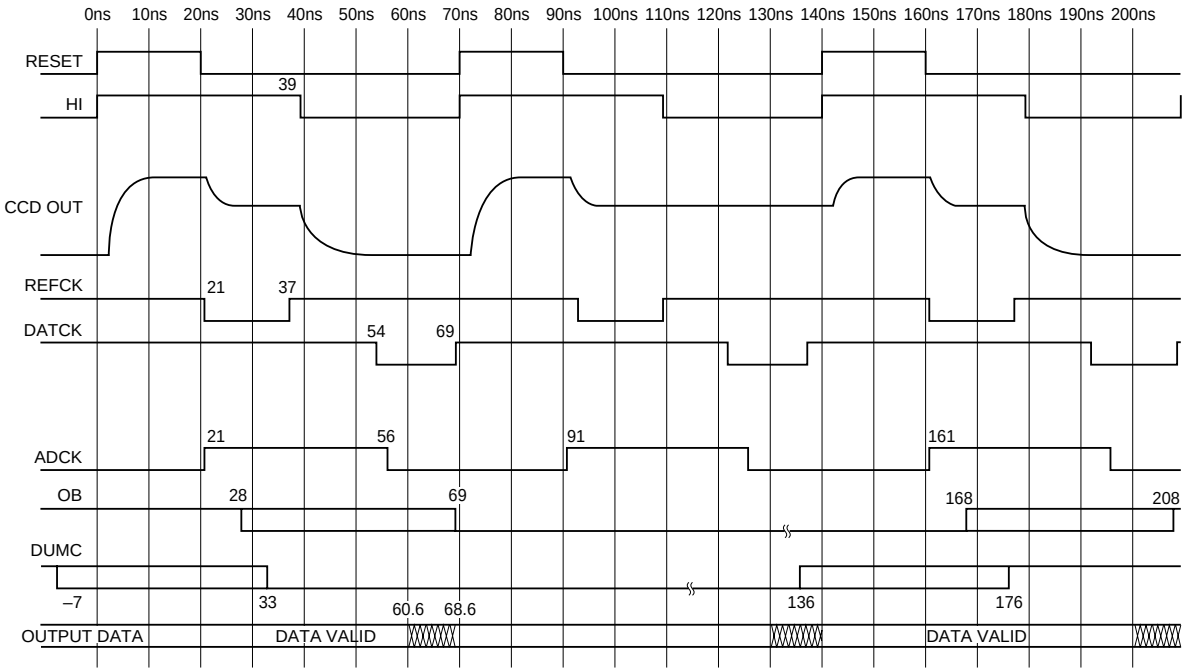
PIN	DESIGNATOR	DESCRIPTION	PIN	DESIGNATOR	DESCRIPTION
1	DV_{SS1}	Digital Ground	27	CCD R	Capacitor for Dummy Feedback Loop
2	B10 (LSB)	LSB of ADS	28	AV_{SS2}	Analog Ground
3	B9	Bit 9	29	AGC1	Sets Gain of CCD Channel, 1kΩ Resistor
4	B8	Bit 8	30	AGC2	Sets Gain of CCD Channel, 16kΩ Resistor
5	B7	Bit 7	31	AV_{SS3}	Analog Ground
6	B6	Bit 6	32	LCM	Attenuator Common-Mode Bypass
7	B5	Bit 5	33	AV_{DD1}	Analog +Supply
8	B4	Bit 4	34	INT BIAS 2	Internal Bias, should be connected to GND with 0.1µF Capacitor
9	B3	Bit 3	35	AV_{SS}	Analog Ground
10	B2	Bit 2	36	INT BIAS 1	Internal Bias, should be connected to GND with 0.1µF Capacitor
11	B1 (MSB)	MSB of ADS	37	2.4V	Attenuator Ladder Bypass
12	DRV_{DD}	Digital +Supply of ADS Output	38	CM	ADS Common-Mode Voltage
13	DRV_{SS}	Digital Ground for ADS Output	39	AV_{DD2}	Analog +Supply
14	DV_{SS2}	Digital Ground	40	AV_{DD3}	Analog +Supply
15	DV_{SS3}	Digital Ground	41	DV_{SS}	Digital Ground
16	ADCK	ADS Clock, Data Output on Falling Edge	42	AV_{DD}	Analog +Supply
17	DV_{DD1}	Digital +Supply	43	AV_{DD4}	Analog +Supply
18	PD	L = Normal Operation, H = Reduced Power	44	AV_{DD5}	Analog +Supply
19	PB	L = –FS + 32 LSB, H = Normal at CCD Mode	45	AV_{SS4}	Analog Ground
20	OB	Optical Black Clamp Pulse, Active LOW	46	AV_{SS5}	Analog Ground
21	REFCK	Neg Pulse, Trailing Edge Samples Reset	47	REFN	ADS –Reference, Bypass to Ground
22	DATCK	Neg Pulse, Trailing Edge Samples Data	48	REFP	ADS +Reference, Bypass to Ground
23	DUMC	Dummy Clamp, Active LOW			
24	C	Capacitor for Optical Feedback			
25	AV_{SS1}	Analog Ground			
26	CCD D	CCD Signal Input			

TIMING DIAGRAMS

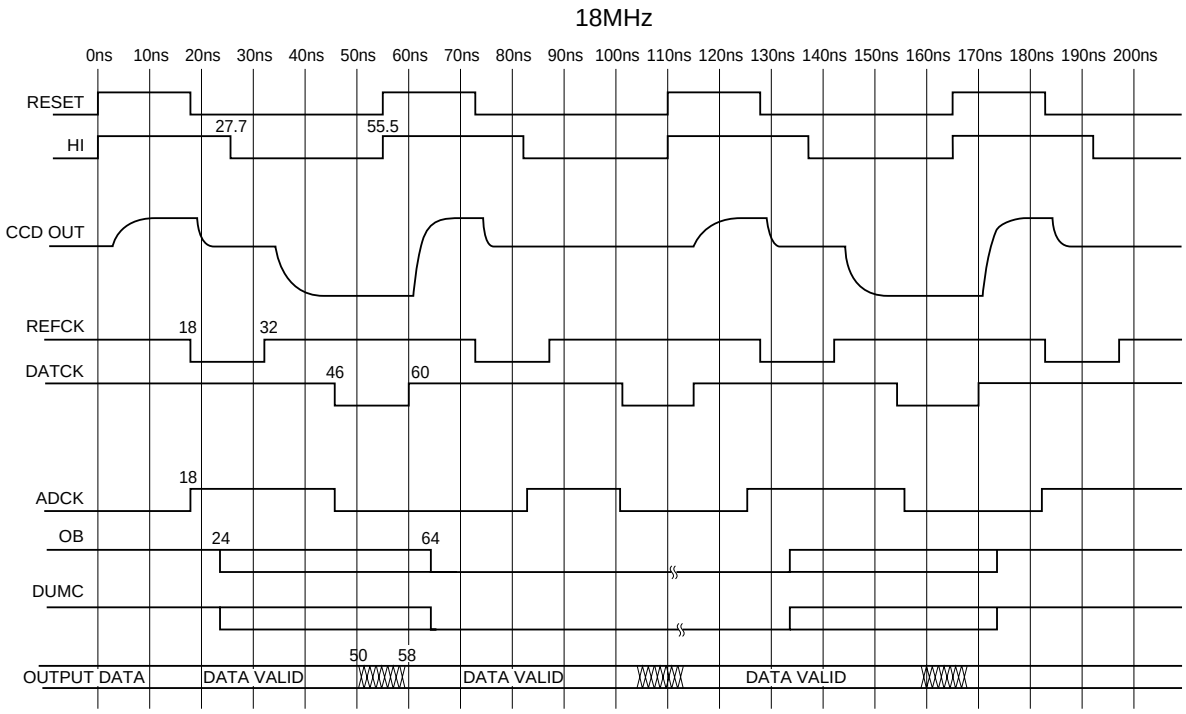
9.5MHz



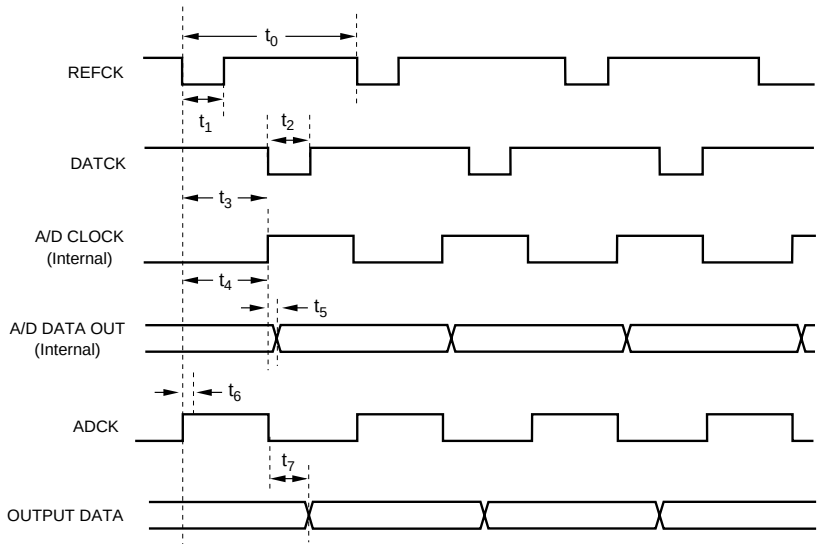
14MHz



TIMING DIAGRAMS (CONT)



ADCK OUTPUT TIMING



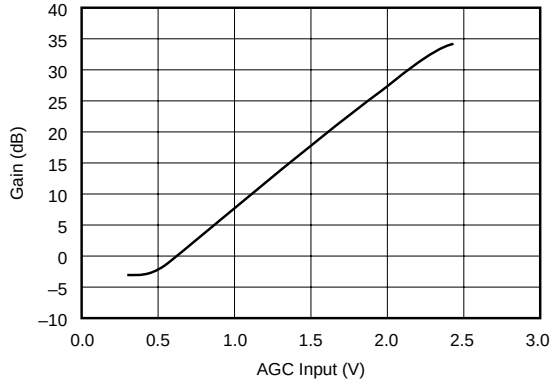
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_0	ADCK Clock Period	55.6			ns
t_1	REFCK Pulse Width		14		ns
t_2	DATCK Pulse Width		14		ns
t_3	DATCK Delay	27	28	29	ns
t_4	A/D Clock Delay (Internal)	26	28	30	ns
t_5	A/D Data Out Delay (Internal)	1.5	2.0	2.5	ns
t_6	ADCK Delay	–25	0	25	ns
t_7	Output Data Delay	7.1	8.3	9.5	ns

NOTE: Timing Specifications = T_{MIN} to T_{MAX} with DRV_{DD} = 3.0V, ADV_{DD} = 3.0V, DV_{DD} = 3.0V. 18MHz timing shown for reference.

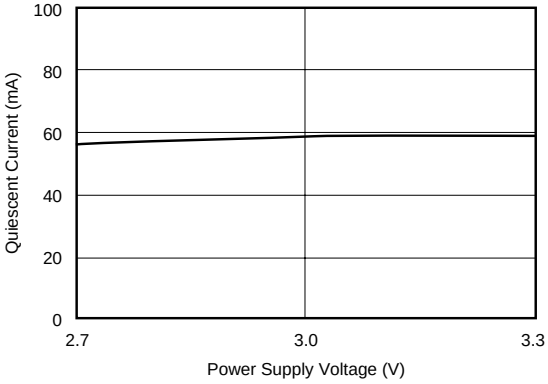
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, AV_{DD} = AV_{DD2} = +3.0V, DV_{DD} = DV_{DD1} = DRV_{DD1} = +3.0V, unless otherwise specified.

VCA CHARACTERISTICS



QUIESCENT CURRENT vs POWER SUPPLY



THEORY OF OPERATION

The VSP2000 is an integrated circuit that contains many of the key features associated with the processing of analog signals in a video camera or digital still camera. Figure 1 shows a simplified block diagram of the VSP2000.

The output from the CCD array is first sent to a correlated double sampler (CDS), a voltage-controlled attenuator with a logarithmic control characteristic, and an output amplifier prior to being applied to the input of a 10-bit analog-to-digital converter.

Two calibration cycles are employed to reduce the offset variation of the VSP2000. During the dummy pixel time, an input auto-zero circuit is activated that eliminates the offset of the correlated double sampler. During the optical black timing interval, another auto-zero circuit is employed to eliminate the offset associated with the output amplifier and the remaining offset from the CDS.

CORRELATED DOUBLE SAMPLER (CDS)

The CDS removes low frequency noise from the output of the image sensor. Refer to Figure 2 which shows a block diagram of the CDS. The output from the CCD array is sampled during the reference interval as well as during the data interval. Noise that is present at the input and is of a period greater than the pixel interval will be eliminated by subtraction.

The VSP2000 employs a three track/hold correlated double sampler architecture. Track/Hold 2 is sampled during the reference interval by the REFCK signal. Track/Hold 3 is resampled at the same time that the data Track/Hold 1 is sampled by the DATCK signal. This is done to remove large transients from Track/Hold 2 that results from a portion of the reset transient being present during the acquisition time of this track and hold. The output of Track/Hold 2 is buffered by a voltage follower.

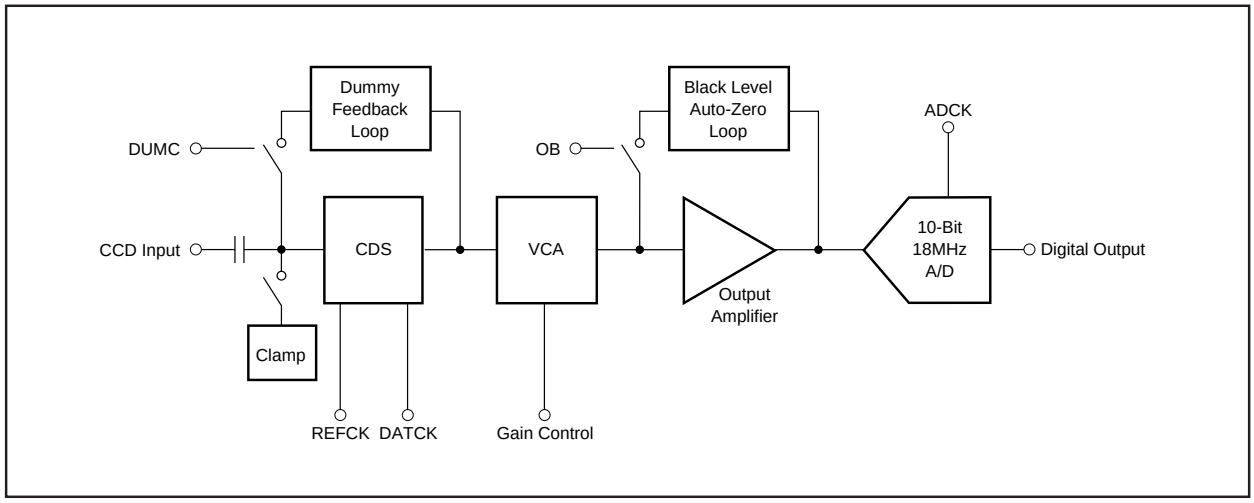


FIGURE 1. Simplified Block Diagram of VSP2000.

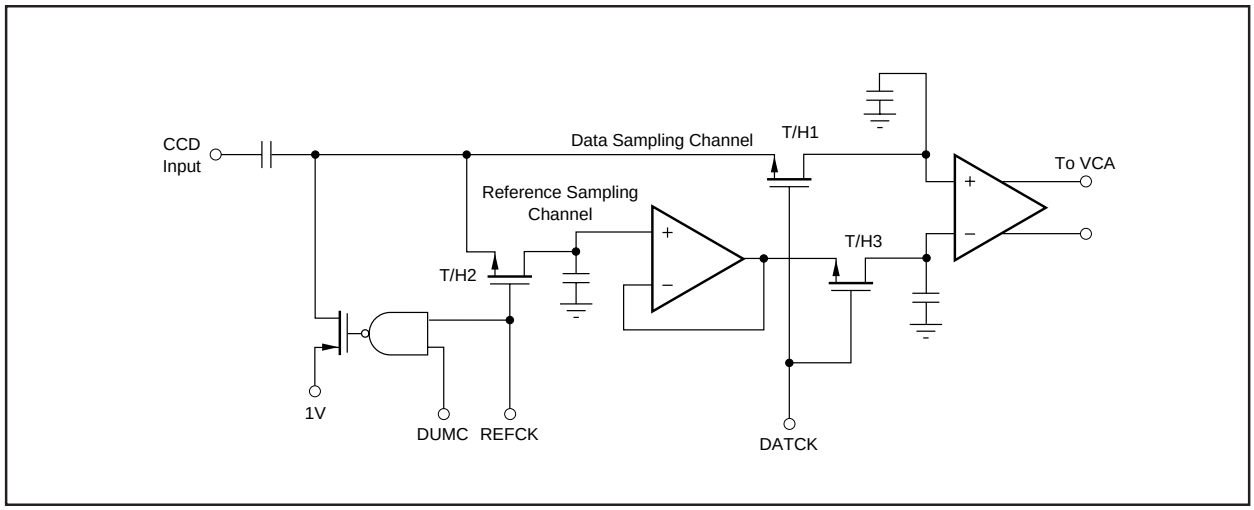


FIGURE 2. Block Diagram of Correlated Double Sampler.

DIFFERENCE AMPLIFIER

The correlated double sampler function is completed when the output of the data and reference channel are sent to the difference amplifier where the signals are subtracted. In addition to providing the difference function, the difference amplifier amplifies the signal by a factor of 2 which helps to improve the overall signal-to-noise ratio. The difference amplifier also generates a differential signal to drive the voltage-controlled attenuator.

INPUT CLAMP

The output from the CCD array is capacitively coupled to the VSP2000. To prevent shifts in the DC level from taking place due to varying input duty cycles, the input capacitor is clamped during the dummy pixel interval by the REFCK signal. A P-channel transistor is used for this input clamp switch to be able to allow a 2V negative change at the input that would bring the signal below ground by 1. Under typical conditions, the bias at the input to the VSP2000 is at 1V.

DUMMY PIXEL AUTO-ZERO LOOP

The output from the data and reference channel is processed by the previously mentioned difference amplifier. The differential output from the difference amplifier is sent to both the voltage-controlled logarithmic attenuator and to an error amplifier. The error amplifier amplifies and feeds a signal to the difference amplifier to drive the offset measured at the output of the difference amplifier to zero. A block diagram of this circuit is shown in Figure 3. This error amplifier serves the purpose of reducing the offset of the CDS to avoid a large offset from being amplified by the output amplifier.

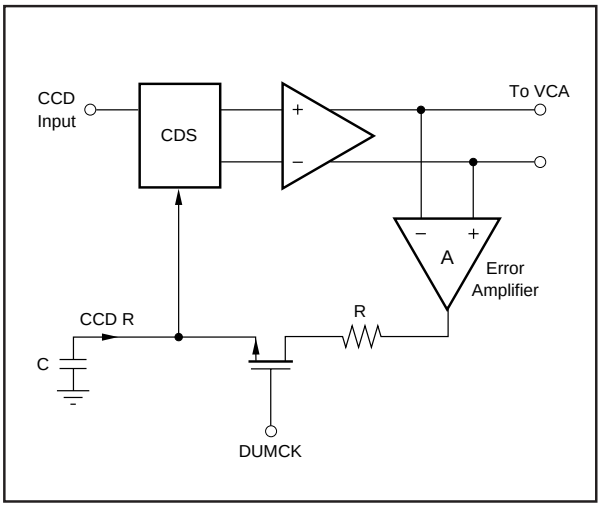


FIGURE 3. Block Diagram of Dummy Pixel Loop.

The effective time constant of this loop is given by:

$$T = \frac{RC}{AD}$$

where R is 10kΩ, C is an external capacitor connected to pin 27 (CCD R), A is the gain of the error amplifier with a value of 50, and D is the duty cycle of the time that the dummy pixel auto-zero loop is in operation. The duty cycle (D) must be considered as the loop operates in a sampled mode. Operation of the dummy auto-zero loop is activated by the DUMC signal that happens once during each horizontal line interval.

TIMING

The REFCK and DATCK signals are used to operate the CDS as previously explained. These same two signals are also used by internal timing circuitry to create the necessary timing signals for the A/D. The output from the A/D is read out to external circuitry by the ADCK signal. DUMC is used to activate the dummy pixel auto-zero loop and OB is used to activate the black level auto-zero loop. The input digital timing signals REFCK, DATCK, DUMC and OB are capable of being driven from either 3V or 5V logic levels.

VOLTAGE-CONTROLLED ATTENUATOR

To maximize the dynamic range of the VSP2000, a voltage-controlled attenuator is included with a control range from 0dB to –34dB. The gain control has a logarithmic relationship between the control voltage and the attenuation. The attenuator processes a differential signal from the difference amplifier to improve linearity and to reject both power supply and common-mode noise. The output from the attenuator is amplified by 28dB prior to being applied to the A/D. A typical gain control characteristic of the VSP2000 is shown in the typical performance curve, “VCA Characteristics”. AGC1 is a coarse gain control and AGC2 is a fine gain control. Figure 4 shows how the gain control signals are applied.

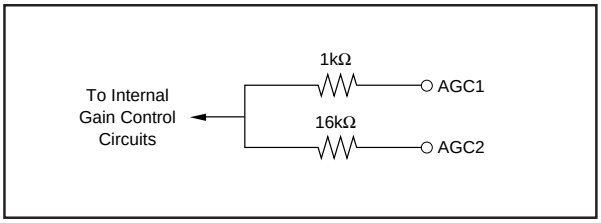


FIGURE 4. Gain Control Resistors.

BLACK LEVEL AUTO-ZERO LOOP

The black level auto-zero loop amplifies the difference between the output of the output amplifier and a reference signal during the dummy pixel interval. This difference signal is amplified and fed back into the output amplifier to correct the offset. In doing so, the output level of the entire CCD channel can be controlled to be approximately –FS + 32LSBs under zero signal conditions. The black level auto-zero loop is activated by the OB timing signal.

Figure 5 shows a block diagram of the black level auto-zero loop. The loop time constant is given by:

$$T = \frac{C}{(G_M)\,(D)}$$

where C is the external filter capacitance applied to pin 24 (C), G_M is .001Ω and D is the duty cycle of the time that the black level auto-zero loop is in operation. The duty cycle (D) must be considered as the loop operates in a sampled mode. Operation of the black level auto-zero loop is activated by the OB signal that happens once during each horizontal line interval.

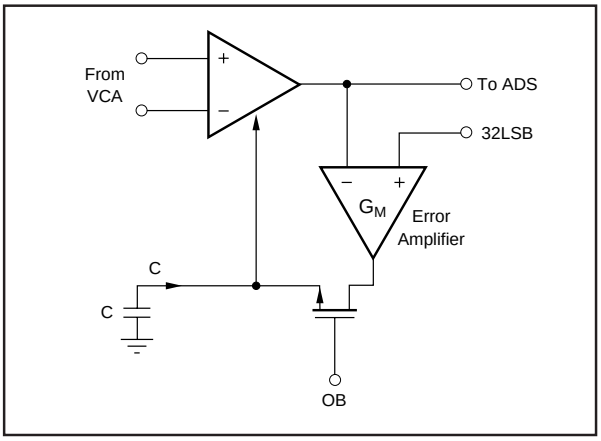


FIGURE 5. Black Level Auto-Zero Loop.

A/D CONVERTER

The A/D converter utilizes a pipline architecture. The fully differential topology and digital error correction guarantee 10-bit resolution. The A/D converter circuitry includes a reference circuit that provides bias voltages for the entire system.

DECOUPLING AND GROUNDING CONSIDERATIONS

The VSP2000 has several supply pins, one of which is dedicated to supply only the digital output driver (pin 17, DV_{DD1}). The remaining supply pins are not, as is often the case, divided into analog and digital supply pins since they are internally connected on the chip. For this reason, it is recommended that the VSP2000 be treated as an analog component and to power if from the analog supply only. Digital supply lines often carry high levels of wide band noise which can couple back into the VSP2000 and limit performance.

Figure 6 shows the recommended decoupling scheme for the VSP2000. In most cases, 0.1µF ceramic chip capacitors are adequate to keep the impedance low over a wide frequency range. Their effectiveness largely depends on the proximity to the individual pin. Therefore, they should be located as close as possible to the pins. In addition, one larger capacitor (1µF to 22µF) should be placed on the PC board in proximity of the VSP2000.

DEMONSTRATION BOARD

A demonstration board, DEM-VSP2000, is available to assist in the inital evaluation of the circuit performance using the VSP2000. The schematic and board layout of the DEM-VSP2000 are shown in Figure 6 and Figures 7a through 7d, respectively.

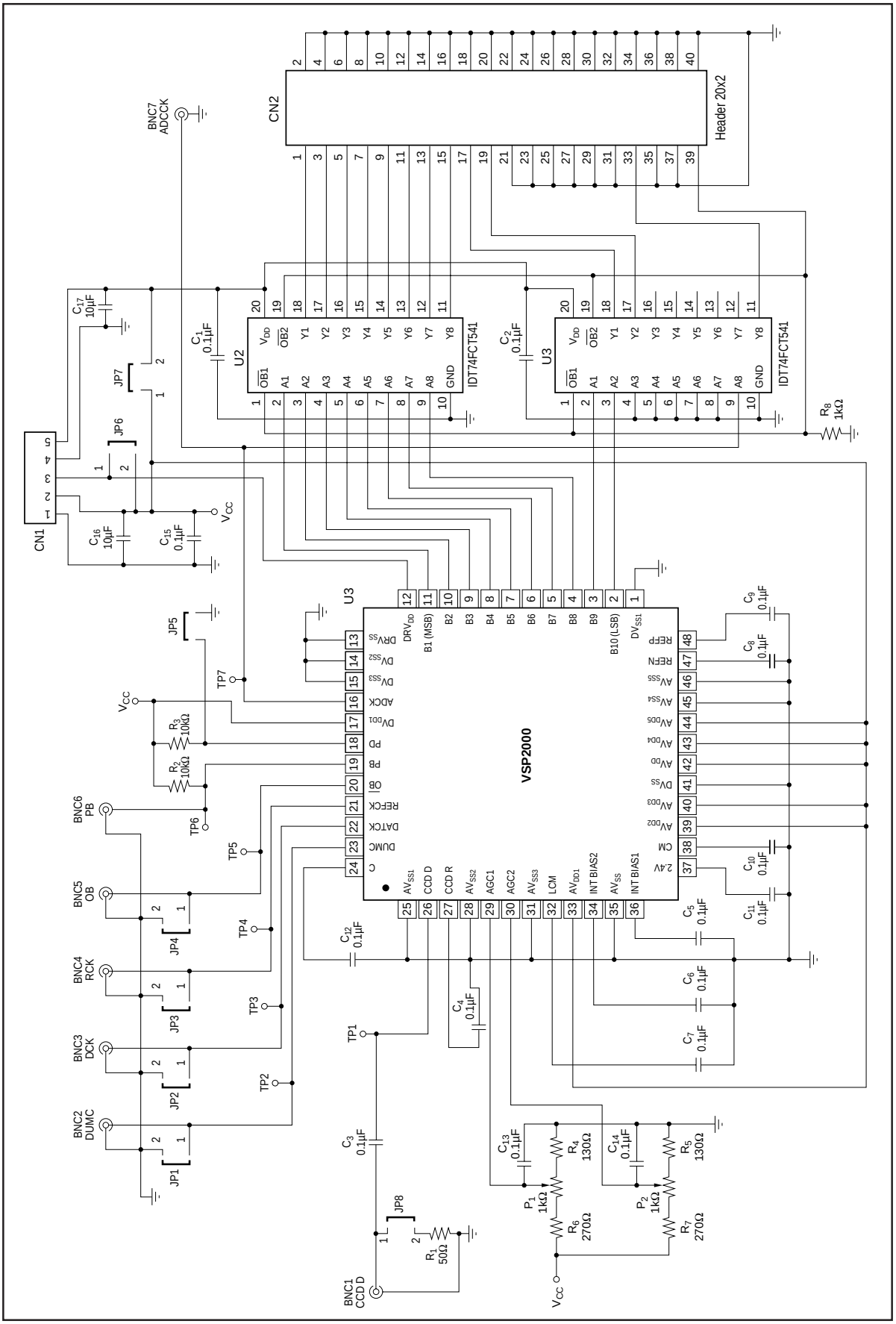


FIGURE 6. Evaluation Board Layout Detail.

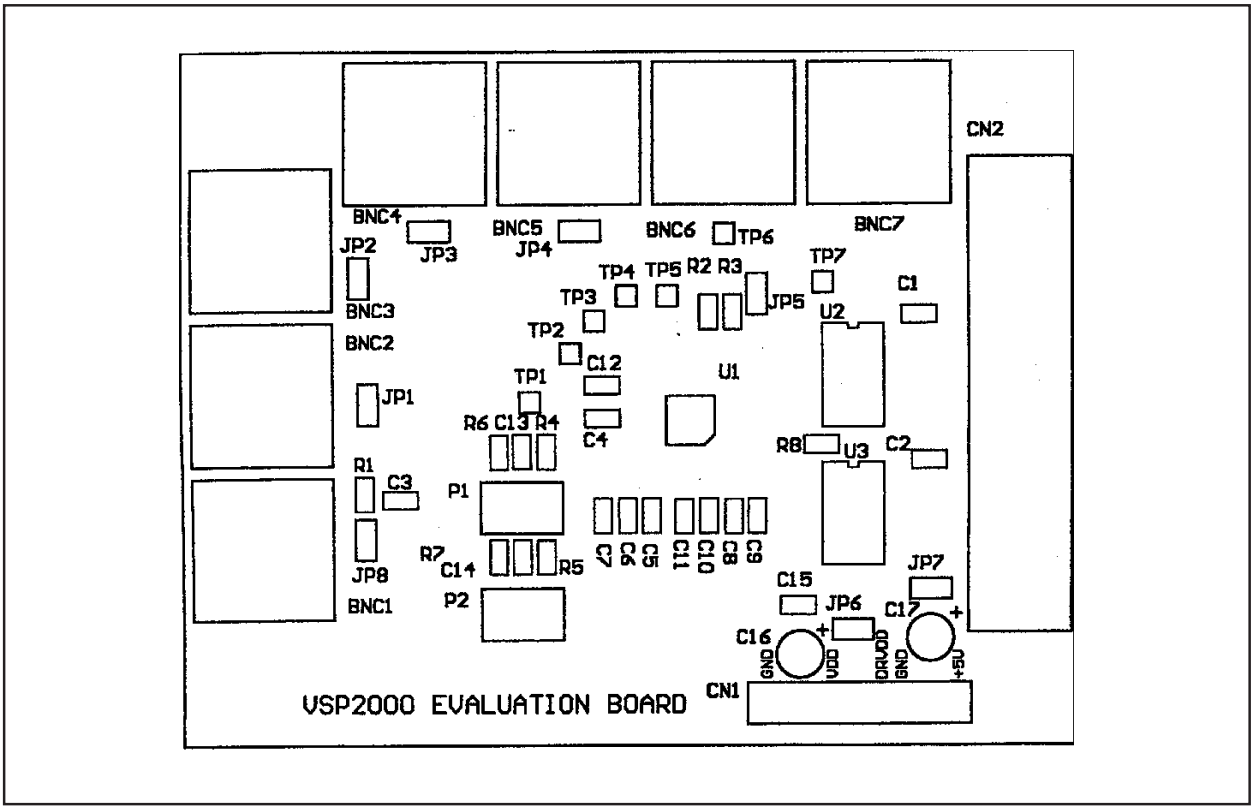


FIGURE 7a. Evaluation Board Silkscreen (top).

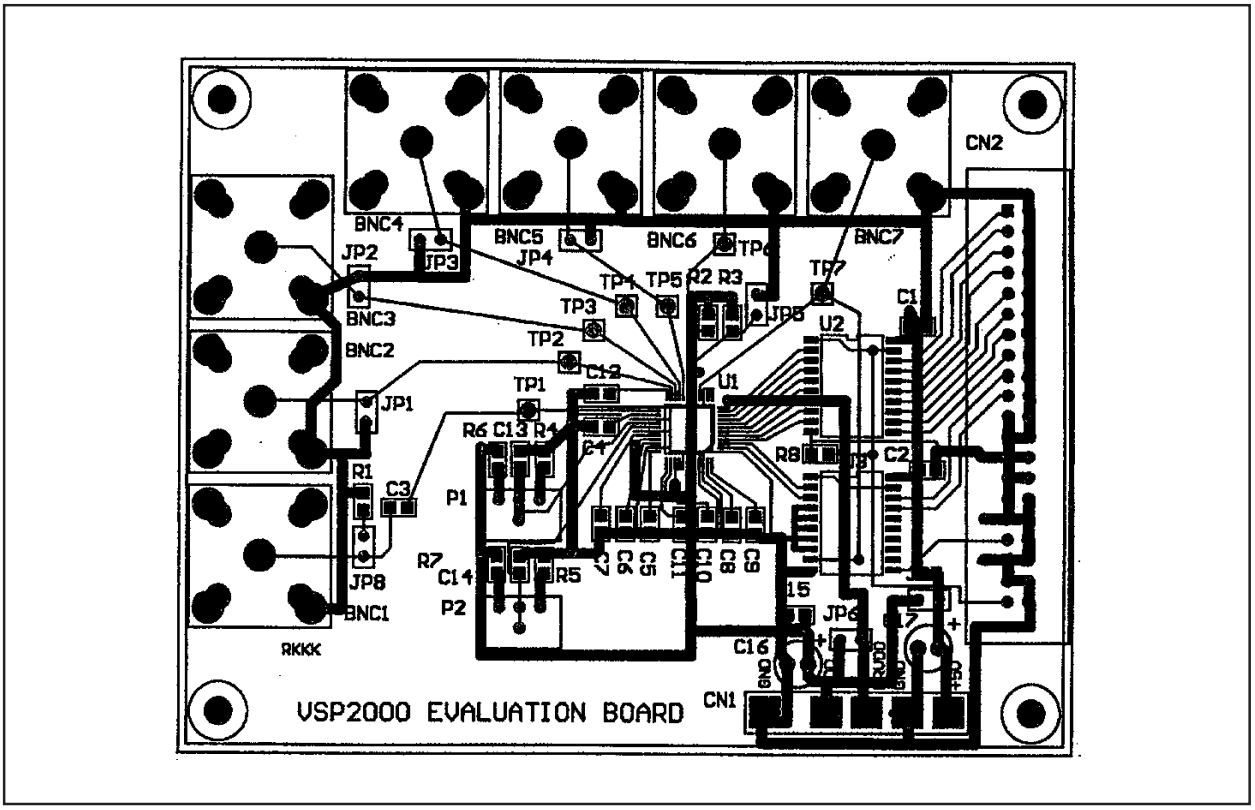


FIGURE 7b. Evaluation Board Layout.

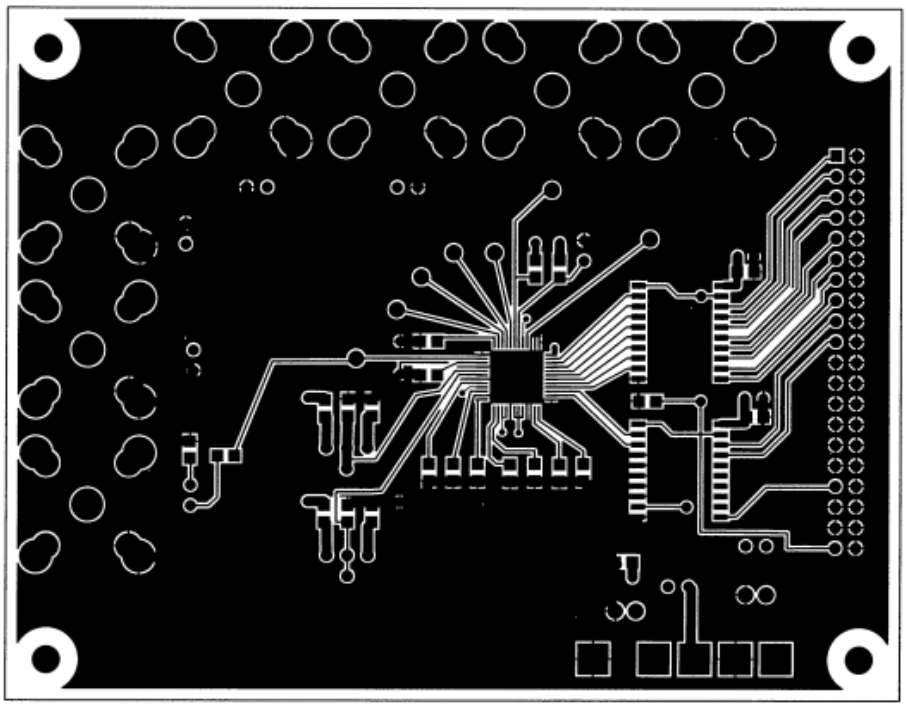


FIGURE 7c. Top Layer.

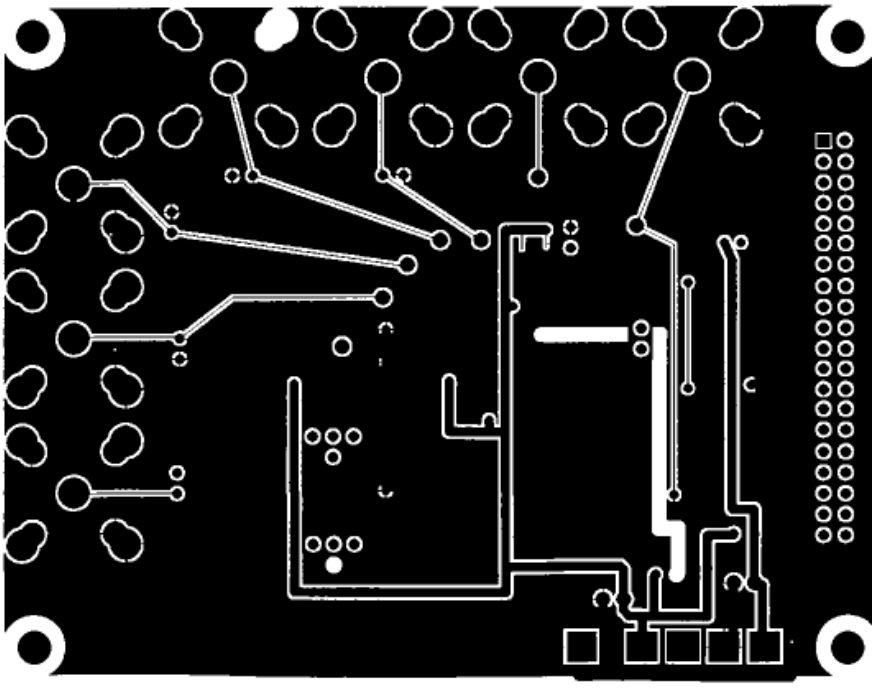


FIGURE 7d. Bottom Layer.