



Ultra Low Power/Voltage CMOS SRAM 512K x 16 or 1M x 8 bit switchable

BS616UV8021

FEATURES

- Ultra low operation voltage : 1.8 ~ 2.3V
- Ultra low power consumption :
V_{cc} = 2.0V C-grade: 20mA (Max.) operating current
I-grade : 25mA (Max.) operating current
0.6uA (Typ.) CMOS standby current
- High speed access time :
-70 70ns (Max.) at V_{cc}=2.0V
-10 100ns (Max.) at V_{cc}=2.0V
- Automatic power down when chip is deselected
- Three state outputs and TTL compatible
- Fully static operation
- Data retention supply voltage as low as 1.5V
- Easy expansion with $\overline{CE1}$, CE2 and \overline{OE} options
- I/O Configuration x8/x16 selectable by CIO, \overline{LB} and \overline{UB} pin

DESCRIPTION

The BS616UV8021 is a high performance, ultra low power CMOS Static Random Access Memory organized as 524,288 words by 16 bits or 1,048,576 bytes by 8 bits selectable by CIO pin and operates from a wide range of 1.8V to 2.3V supply voltage.

Advanced CMOS technology and circuit techniques provide both high speed and low power features with a typical CMOS standby current of 0.6uA and maximum access time of 70/100ns in 2.0V operation.

Easy memory expansion is provided by an active HIGH chip enable2(CE2), active LOW chip enable1(CE1), active LOW output enable(\overline{OE}) and three-state output drivers.

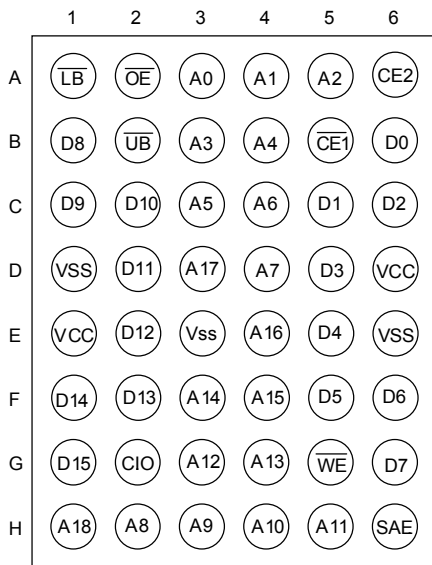
The BS616UV8021 has an automatic power down feature, reducing the power consumption significantly when chip is deselected.

The BS616UV8021 is available in DICE form and 48-pin BGA type.

PRODUCT FAMILY

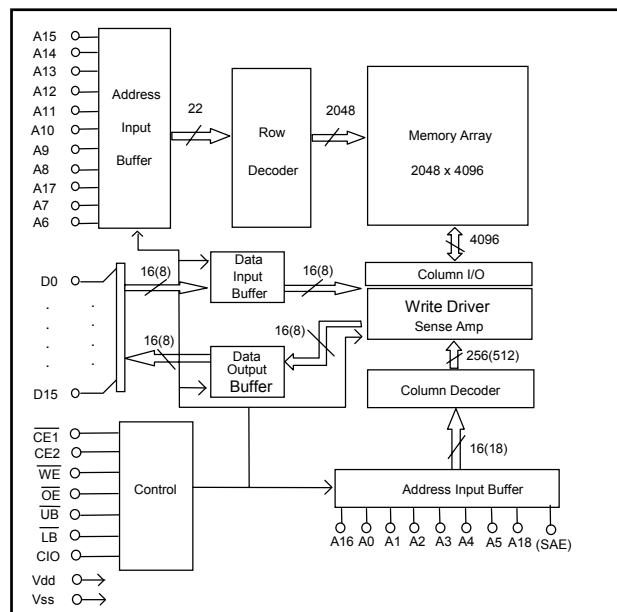
PRODUCT FAMILY	OPERATING TEMPERATURE	V _{cc} RANGE	SPEED (ns)	POWER DISSIPATION		PKG TYPE
				STANDBY (I _{ccsB1} , Max)	Operating (I _{cc} , Max)	
				V _{cc} =2.0V	V _{cc} =2.0V	
BS616UV8021DC	+0 °C to +70 °C	1.8V ~ 2.3V	70 / 100	15uA	20mA	DICE
BS616UV8021BC						BGA-48-0810
BS616UV8021FC						BGA-48-0912
BS616UV8021DI	-40 °C to +85 °C	1.8V ~ 2.3V	70 / 100	20uA	25mA	DICE
BS616UV8021BI						BGA-48-0810
BS616UV8021FI						BGA-48-0912

PIN CONFIGURATIONS



48-Ball CSP top View

BLOCK DIAGRAM



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■ PIN DESCRIPTIONS

Name	Function
A0-A18 Address Input	These 19 address inputs select one of the 524,288 x 16-bit words in the RAM.
SAE Address Input	This address input incorporate with the above 19 address inputs select one of the 1,048,576 x 8-bit bytes in the RAM if the CIO is LOW. Don't use when CIO is HIGH.
CIO x8/x16 select input	This input selects the organization of the SRAM. 524,288 x 16-bit words configuration is selected if CIO is HIGH. 1,048,576 x 8-bit bytes configuration is selected if CIO is LOW.
$\overline{CE1}$ Chip Enable 1 Input CE2 Chip Enable 2 Input	$\overline{CE1}$ is active LOW and CE2 is active HIGH. Both chip enables must be active when data read from or write to the device. If either chip enable is not active, the device is deselected and is in a standby power mode. The DQ pins will be in the high impedance state when the device is deselected.
\overline{WE} Write Enable Input	The write enable input is active LOW and controls read and write operations. With the chip selected, when \overline{WE} is HIGH and \overline{OE} is LOW, output data will be present on the DQ pins; when \overline{WE} is LOW, the data present on the DQ pins will be written into the selected memory location.
\overline{OE} Output Enable Input	The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the DQ pins and they will be enabled. The DQ pins will be in the high impedance state when \overline{OE} is inactive.
\overline{LB} and \overline{UB} Data Byte Control Input	Lower byte and upper byte data input/output control pins. The chip is deselected when both \overline{LB} and \overline{UB} pins are HIGH.
D0 - D15 Data Input/Output Ports	These 16 bi-directional ports are used to read data from or write data into the RAM.
Vcc	Power Supply
Gnd	Ground

■ TRUTH TABLE

MODE	$\overline{CE1}$	CE2	\overline{OE}	\overline{WE}	CIO	\overline{LB}	\overline{UB}	SAE	D0~7	D8~15	VCC Current
Fully Standby	H	X	X	X	X	X	X	X	High-Z	High-Z	I_{CCSB}, I_{CCSB1}
	X	L				X	X				
Output Disable	L	H	H	H	X	X	X	X	High-Z	High-Z	I_{CC}
Read from SRAM (WORD mode)	L	H	L	H	H	L	H	X	Dout	High-Z	I_{CC}
						H	L		High-Z	Dout	
						L	L		Dout	Dout	
Write to SRAM (WORD mode)	L	H	X	L	H	L	H	X	Din	X	I_{CC}
						H	L		X	Din	
						L	L		Din	Din	
Read from SRAM (BYTE Mode)	L	H	L	H	L	X	X	A-1	Dout	High-Z	I_{CC}
Write to SRAM (BYTE Mode)	L	H	X	L	L	X	X	A-1	Din	X	I_{CC}

■ ABSOLUTE MAXIMUM RATINGS⁽¹⁾

SYMBOL	PARAMETER	RATING	UNITS
V _{TERM}	Terminal Voltage with Respect to GND	-0.5 to V _{CC} +0.5	V
T _{BIAS}	Temperature Under Bias	-40 to +125	°C
T _{STG}	Storage Temperature	-60 to +150	°C
P _T	Power Dissipation	1.0	W
I _{OUT}	DC Output Current	20	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

■ OPERATING RANGE

RANGE	AMBIENT TEMPERATURE	V _{CC}
Commercial	0°C to +70°C	1.8V ~ 2.3V
Industrial	-40°C to +85°C	1.8V ~ 2.3V

■ CAPACITANCE⁽¹⁾ (TA = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C _{IN}	Input Capacitance	V _{IN} =0V	6	pF
C _{DQ}	Input/Output Capacitance	V _{I/O} =0V	8	pF

1. This parameter is guaranteed and not tested.

■ DC ELECTRICAL CHARACTERISTICS (TA = 0°C to + 70°C)

PARAMETER NAME	PARAMETER	TEST CONDITIONS	MIN.	TYP. ⁽¹⁾	MAX.	UNITS
V _{IL}	Guaranteed Input Low Voltage ⁽²⁾	V _{CC} =2.0V	-0.5	--	0.6	V
V _{IH}	Guaranteed Input High Voltage ⁽²⁾	V _{CC} =2.0V	1.4	--	V _{CC} +0.2	V
I _{IL}	Input Leakage Current	V _{CC} = Max, V _{IN} = 0V to V _{CC}	--	--	1	uA
I _{OL}	Output Leakage Current	V _{CC} = Max, $\overline{CE1} = V_{IH}$, or CE2 = V _{IL} , or OE = V _{IH} , V _{IO} = 0V to V _{CC}	--	--	1	uA
V _{OL}	Output Low Voltage	V _{CC} = max, I _{OL} = 1mA	V _{CC} =2.0V	--	0.4	V
V _{OH}	Output High Voltage	V _{CC} = Min, I _{OH} = -0.5mA	V _{CC} =2.0V	1.6	--	V
I _{CC}	Operating Power Supply Current	V _{CC} = max, $\overline{CE1} = V_{IL}$ and CE2 = V _{IH} , I _{IQ} = 0mA, F = F _{max} ⁽³⁾	V _{CC} =2.0V	--	20	mA
I _{CCSB}	Standby CurrentTTL	V _{CC} = max, $\overline{CE1} = V_{IH}$ or CE2 = V _{IL} , I _{IQ} = 0mA	V _{CC} =2.0V	--	0.6	mA
I _{CCSB1}	Standby CurrentCMOS	V _{CC} = max, $\overline{CE1} \geq V_{CC}-0.2V$, or CE2 $\leq 0.2V$; V _{IN} $\geq V_{CC} - 0.2V$ or V _{IN} $\leq 0.2V$	V _{CC} =2.0V	--	0.6	15 uA

1. Typical characteristics are at TA = 25°C.

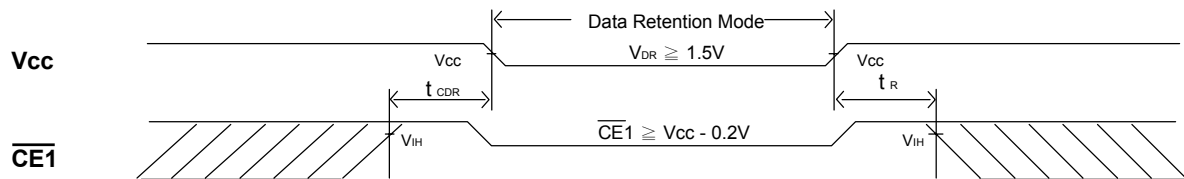
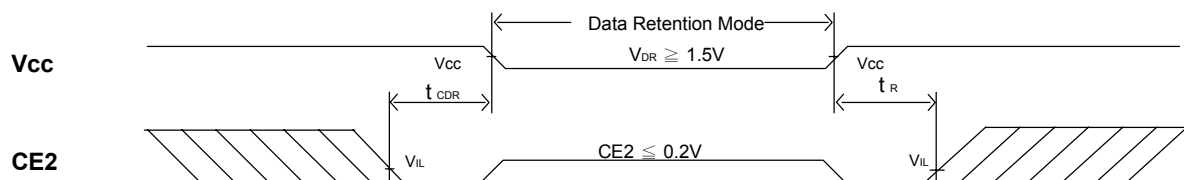
2. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.

3. F_{max} = 1/ t_{RC}.

DATA RETENTION CHARACTERISTICS (TA = 0°C to +70°C)

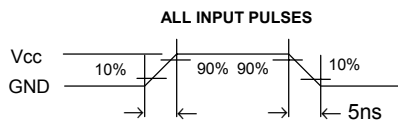
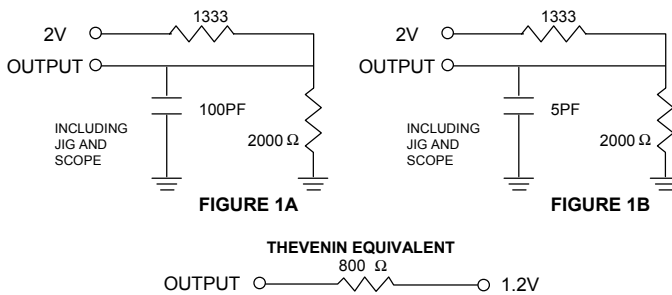
SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP. ⁽¹⁾	MAX.	UNITS
V _{DR}	V _{CC} for Data Retention	$\overline{CE1} \geq V_{CC} - 0.2V$ or $CE2 \leq 0.2V$; $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	1.5	--	--	V
I _{CCDR}	Data Retention Current	$\overline{CE1} \geq V_{CC} - 0.2V$ or $CE2 \leq 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	--	0.4	10	uA
t _{CDR}	Chip Deselect to Data Retention Time	See Retention Waveform	0	--	--	ns
t _R	Operation Recovery Time		T _{RC} ⁽²⁾	--	--	ns






1. V_{CC} = 1.5V, T_A = + 25°C
2. t_{RC} = Read Cycle Time

LOW V_{CC} DATA RETENTION WAVEFORM (1) ($\overline{CE1}$ Controlled)

LOW V_{CC} DATA RETENTION WAVEFORM (2) (CE2 Controlled)


■ AC TEST CONDITIONS

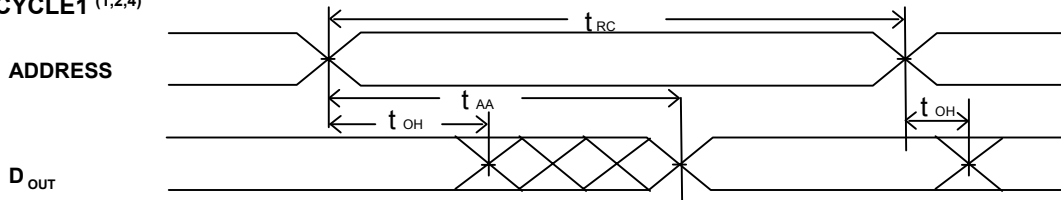
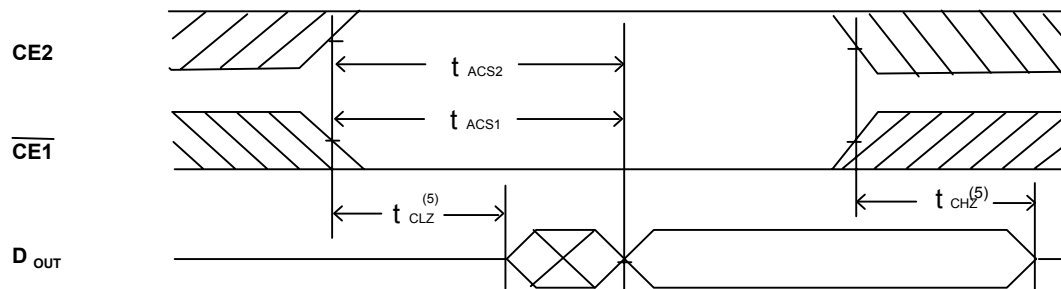
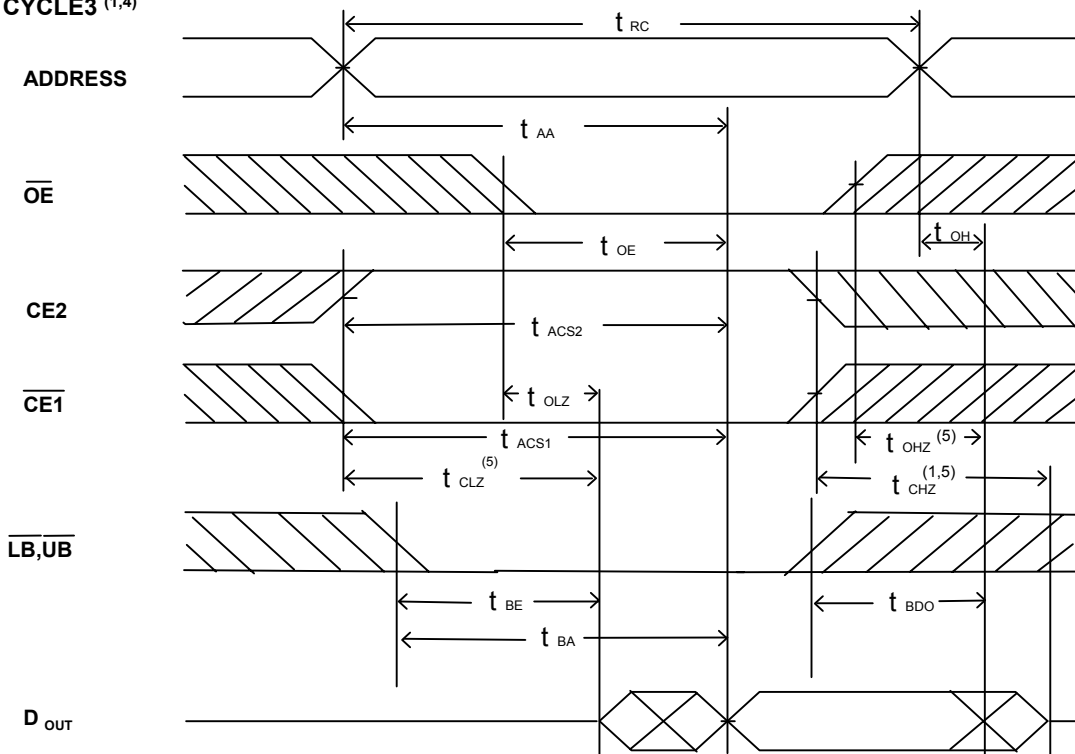
Input Pulse Levels	V _{cc} /0V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Level	0.5V _{cc}

■ AC TEST LOADS AND WAVEFORMS

FIGURE 2
■ KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	MUST BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGE FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGE FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGE: STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

■ AC ELECTRICAL CHARACTERISTICS (TA = 0°C to +70°C, V_{cc}=2.0V)
READ CYCLE

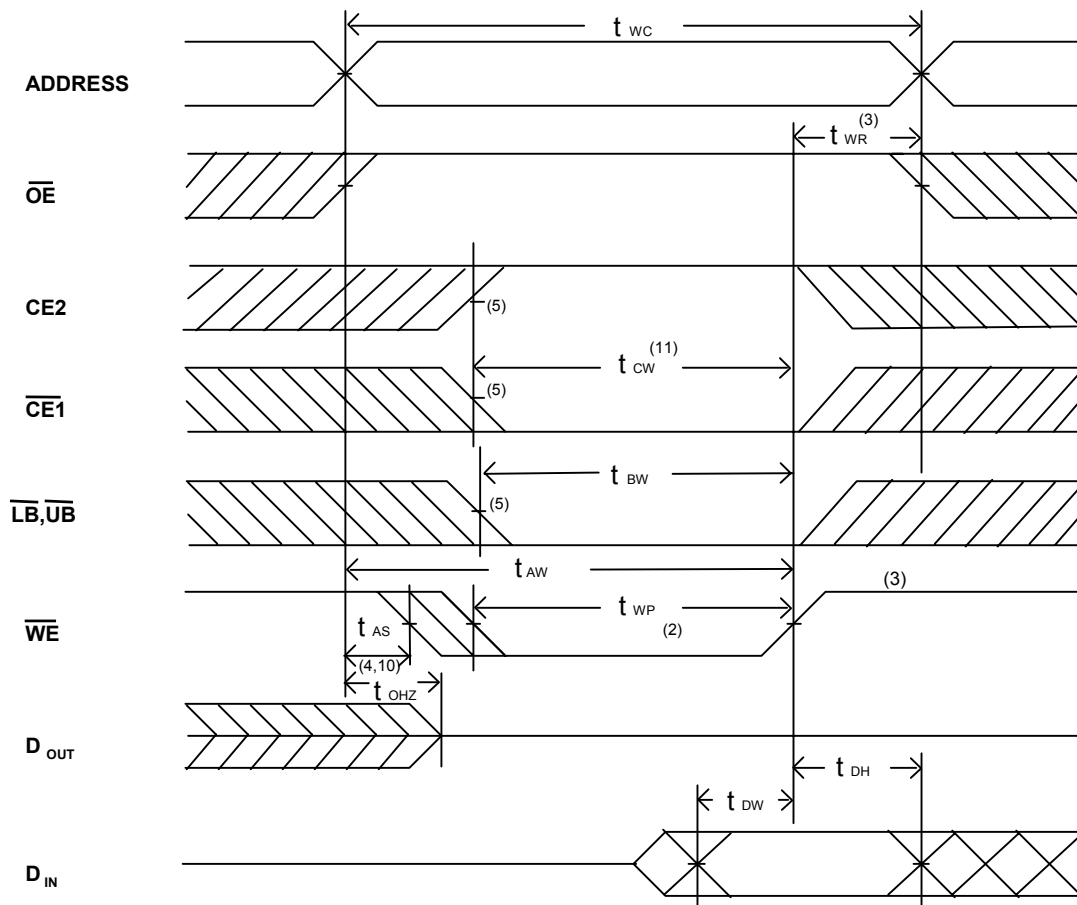
JEDEC PARAMETER NAME	PARAMETER NAME	DESCRIPTION	BS616UV8021-70			BS616UV8021-10			UNIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
t _{AVAX}	t _{RC}	Read Cycle Time	70	—	—	100	—	—	ns
t _{AVQV}	t _{AA}	Address Access Time	—	—	70	—	—	100	ns
t _{E1LQV}	t _{ACS1}	Chip Select Access Time (CE1)	—	—	70	—	—	100	ns
t _{E2LQV}	t _{ACS2}	Chip Select Access Time (CE2)	—	—	70	—	—	100	ns
t _{BA}	t _{BA}	Data Byte Control Access Time (LB,UB)	—	—	50	—	—	60	ns
t _{GLQV}	t _{OE}	Output Enable to Output Valid	—	—	50	—	—	60	ns
t _{ELQX}	t _{CLZ}	Chip Select to Output Low Z (CE2,CE1)	10	—	—	15	—	—	ns
t _{BE}	t _{BE}	Data Byte Control to Output Low Z (LB,UB)	10	—	—	15	—	—	ns
t _{GLQX}	t _{OLZ}	Output Enable to Output in Low Z	10	—	—	15	—	—	ns
t _{EHQZ}	t _{CHZ}	Chip Deselect to Output in High Z (CE2,CE1)	0	—	35	0	—	40	ns
t _{BDO}	t _{BDO}	Data Byte Control to Output High Z (LB,UB)	0	—	30	0	—	35	ns
t _{GHQZ}	t _{OHZ}	Output Disable to Output in High Z	0	—	30	0	—	35	ns
t _{AXQX}	t _{OH}	Output Disable to Output Address Change	10	—	—	15	—	—	ns

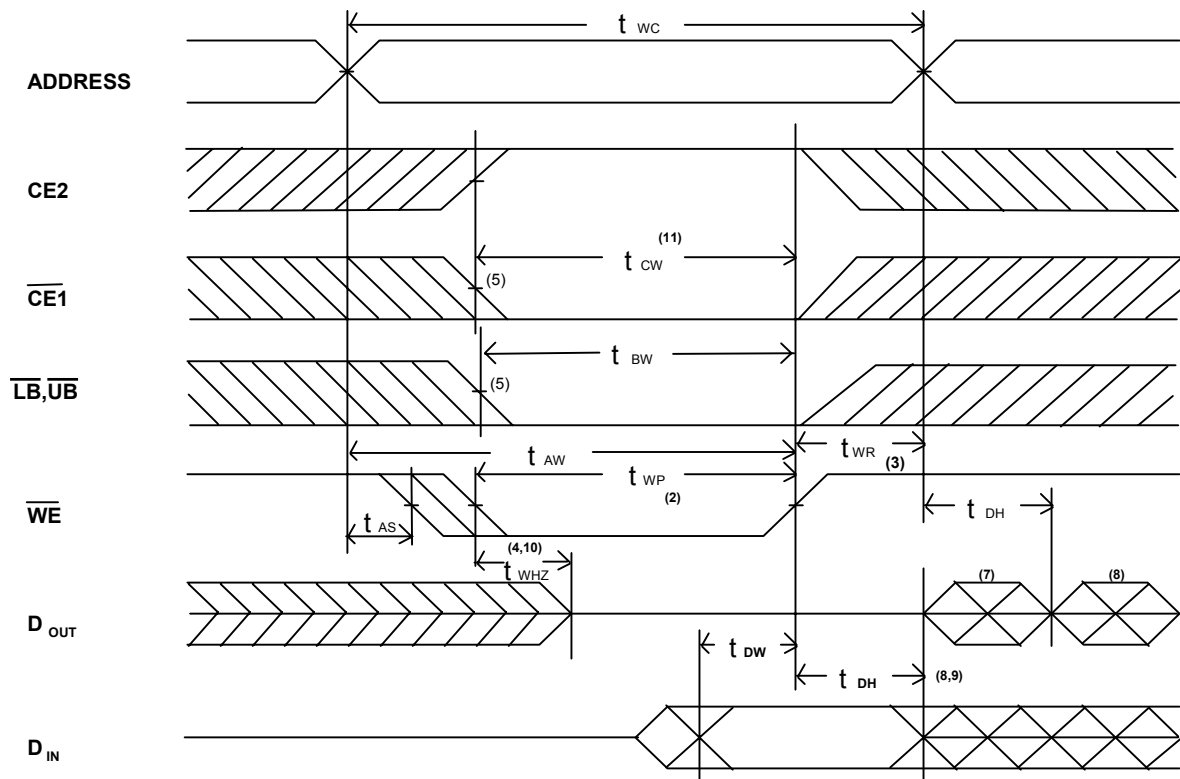
SWITCHING WAVEFORMS (READ CYCLE)
READ CYCLE1 (1,2,4)

READ CYCLE2 (1,3,4)

READ CYCLE3 (1,4)

NOTES:

1. \overline{WE} is high in read Cycle.
2. Device is continuously selected when $\overline{CE1} = V_{IL}$ and $CE2 = V_{IH}$.
3. Address valid prior to or coincident with $\overline{CE1}$ transition low and $CE2$ transition high.
4. $\overline{OE} = V_{IL}$.
5. Transition is measured $\pm 500mV$ from steady state with $CL = 30pF$ as shown in Figure 1B.
The parameter is guaranteed but not 100% tested.

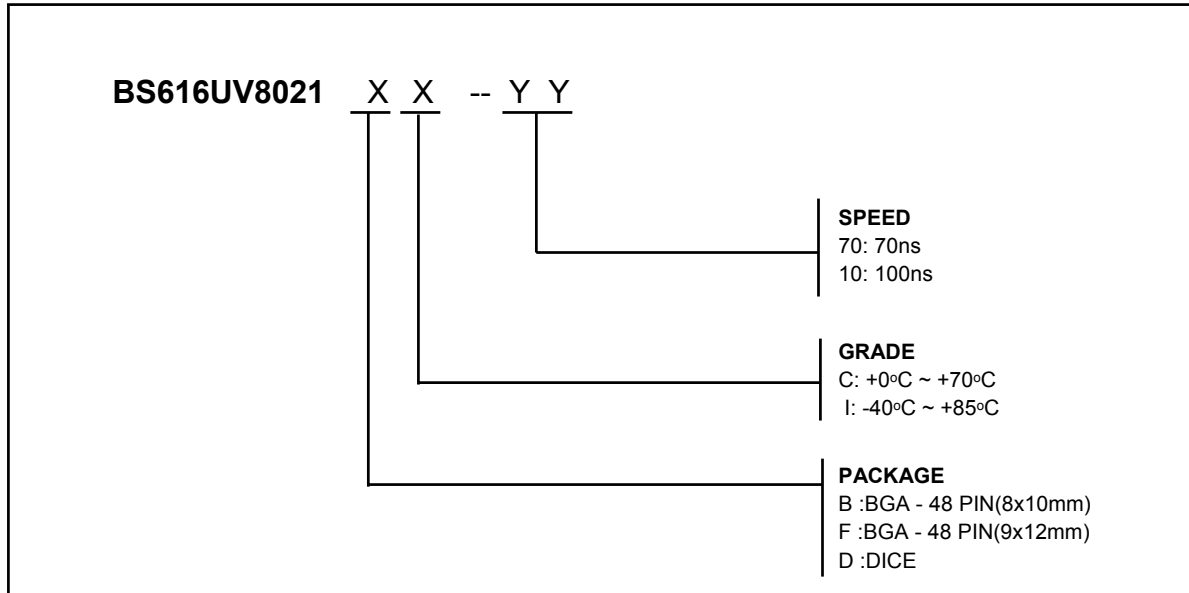
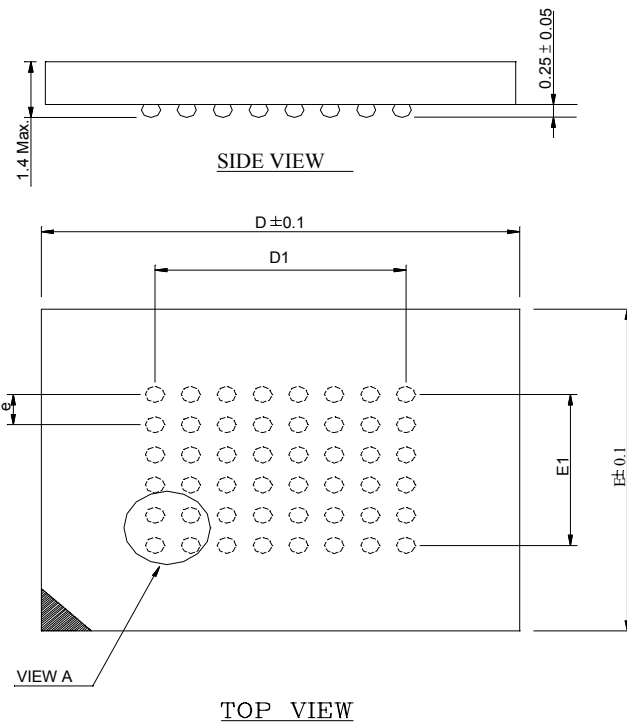
■ AC ELECTRICAL CHARACTERISTICS (TA = 0°C to +70°C, Vcc=2.0V)
WRITE CYCLE

JEDEC PARAMETER NAME	PARAMETER NAME	DESCRIPTION	BS616UV8021-70			BS616UV8021-10			UNIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
t_{AVAX}	t_{WC}	Write Cycle Time	70	-	-	100	-	-	ns
t_{E1LWH}	t_{CW}	Chip Select to End of Write	70	-	-	100	-	-	ns
t_{AVWL}	t_{AS}	Address Set up Time	0	-	-	0	-	-	ns
t_{AVWH}	t_{AW}	Address Valid to End of Write	70	-	-	100	-	-	ns
t_{WLWH}	t_{WP}	Write Pulse Width	50	-	-	70	-	-	ns
t_{WHAX}	t_{WR}	Write Recovery Time (CE2, $\overline{CE1}$, \overline{WE})	0	-	-	0	-	-	ns
t_{BW}	t_{BW}	Data Byte Control to End of Write (\overline{LB} , \overline{UB})	60	-	-	80	-	-	ns
t_{WLQZ}	t_{WHZ}	Write to Output in High Z	0	-	30	0	-	40	ns
t_{DVWH}	t_{DW}	Data to Write Time Overlap	30	-	-	40	-	-	ns
t_{WHDX}	t_{DH}	Data Hold from Write Time	0	-	-	0	-	-	ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output in High Z	0	-	30	0	-	40	ns
t_{WHQX}	t_{OW}	End of Write to Output Active	5	-	-	10	-	-	ns

■ SWITCHING WAVEFORMS (WRITE CYCLE)
WRITE CYCLE1 ⁽¹⁾


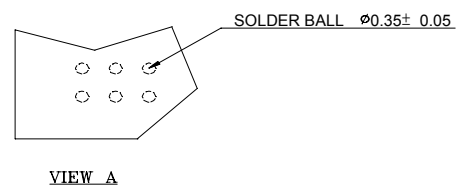
WRITE CYCLE2 (1,6)

NOTES:

1. \overline{WE} must be high during address transitions.
2. The internal write time of the memory is defined by the overlap of CE2, $\overline{CE1}$ and \overline{WE} low. All signals must be active to initiate a write and any one signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the second transition edge of the signal that terminates the write.
3. t_{wr} is measured from the earlier of CE2 going low, or $\overline{CE1}$ or \overline{WE} going high at the end of write cycle.
4. During this period, DQ pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the CE2 high transition or $\overline{CE1}$ low transition or $\overline{LB, UB}$ low transition occurs simultaneously with the \overline{WE} low transitions or after the \overline{WE} transition, output remain in a high impedance state.
6. \overline{OE} is continuously low ($\overline{OE} = V_{IL}$).
7. D_{OUT} is the same phase of write data of this write cycle.
8. D_{OUT} is the read data of next address.
9. If CE2 is high or $\overline{CE1}$ is low during this period, DQ pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. Transition is measured $\pm 500mV$ from steady state with $CL = 30pF$ as shown in Figure 1B. The parameter is guaranteed but not 100% tested.
11. t_{cw} is measured from the later of CE2 going high or $\overline{CE1}$ going low to the end of write.

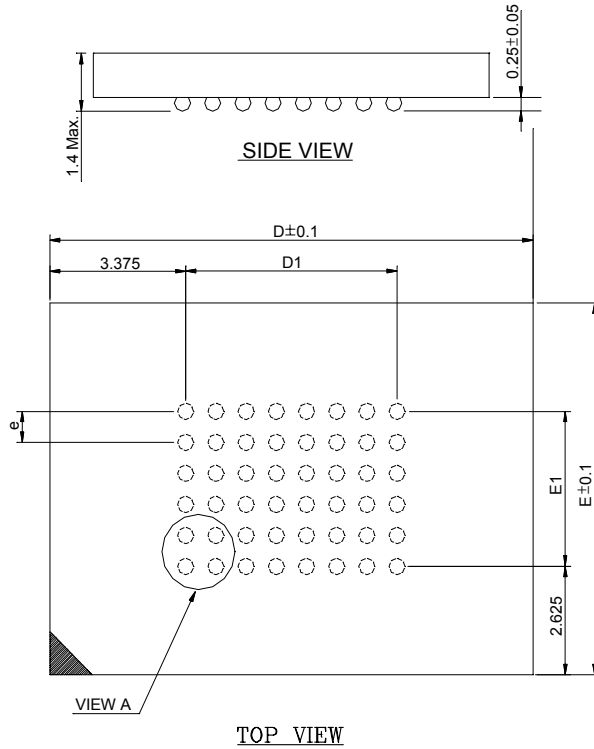
ORDERING INFORMATION

PACKAGE DIMENSIONS


NOTES:
1: CONTROLLING DIMENSIONS ARE IN MILLIMETERS.
2: PIN#1 DOT MARKING BY LASER OR PAD PRINT.
3: SYMBOL "N" IS THE NUMBER OF SOLDER BALLS.

N	D	E	D1	E1	e
48	10.0	8.0	5.25	3.75	0.75

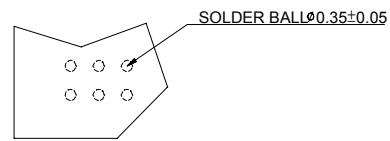


48 mini-BGA (8 x 10mm)

■ PACKAGE DIMENSIONS (continued)


NOTES:
 1: CONTROLLING DIMENSIONS ARE IN MILLIMETERS.
 2: PIN#1 DOT MARKING BY LASER OR PAD PRINT.
 3: SYMBOL "N" IS THE NUMBER OF SOLDER BALLS.

N	D	E	D1	E1	e
48	12.0	9.0	5.25	3.75	0.75



VIEW A

TOP VIEW
48 mini-BGA (9 x 12mm)

REVISION HISTORY

Revision	Description	Date	Note
2.2	2001 Data Sheet release	Apr. 15, 2001	