

# N-Channel JFET Switch

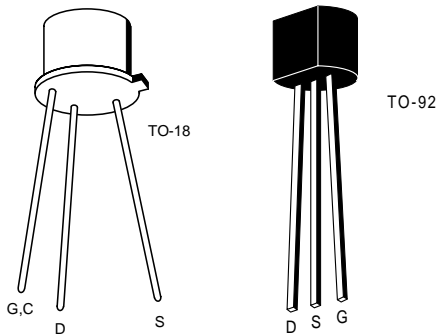


## 2N4391 – 2N4393 / PN4391 – PN4393 / SST4391 – SST4393

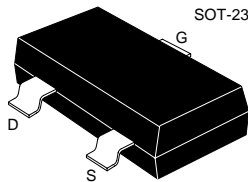
### FEATURES

- $r_{ds(on)} < 300$  Ohms (2N4391)
- $I_{D(OFF)} < 100$  pA
- Switches  $\pm 10$ VAC With  $\pm 15$ V Supplies (4392, 4393)

### PIN CONFIGURATION



5001



PRODUCT MARKING (SOT-23)	
SST4391	N01
SST4392	N02
SST4393	N03

### ABSOLUTE MAXIMUM RATINGS

( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Gate-Source or Gate-Drain Voltage ..... -40V  
 Gate Current ..... 10mA  
 Storage Temperature Range .....  $-65^\circ\text{C}$  to  $+200^\circ\text{C}$   
 Operating Temperature Range .....  $-55^\circ\text{C}$  to  $+200^\circ\text{C}$   
 Lead Temperature (Soldering, 10sec) .....  $+300^\circ\text{C}$

	TO-18	TO-92	SOT-23
Power Dissipation	1.8W	360mW	350mW
Derate above $25^\circ\text{C}$	10mW/ $^\circ\text{C}$	3.3mW/ $^\circ\text{C}$	2.8mW/ $^\circ\text{C}$

Plastic

Storage .....  $-55^\circ\text{C}$  to  $+150^\circ\text{C}$   
 Operating .....  $-55^\circ\text{C}$  to  $+135^\circ\text{C}$

**NOTE:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### ORDERING INFORMATION

Part	Package	Temperature Range
2N4391/93	Hermetic TO-18	$-55^\circ\text{C}$ to $+200^\circ\text{C}$
PN4391/93	Plastic TO-92	$-55^\circ\text{C}$ to $+135^\circ\text{C}$
SST4391/93	Plastic SOT-23	$-55^\circ\text{C}$ to $+135^\circ\text{C}$
X2N4391/93	Sorted Chips in Carriers	$-55^\circ\text{C}$ to $+200^\circ\text{C}$

**ELECTRICAL CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$  unless otherwise specified)

SYMBOL	PARAMETER	4391		4392		4393		UNITS	TEST CONDITIONS	
		MIN	MAX	MIN	MAX	MIN	MAX			
I <sub>GSS</sub>	Gate Reverse Current		-100		-100		-100	pA	V <sub>GS</sub> = -20V, V <sub>DS</sub> = 0	
			-200		-200		-200			T <sub>A</sub> = 150°C
BV <sub>GSS</sub>	Gate-Source Breakdown Voltage	-40		-40		-40		V	I <sub>G</sub> = -1μA, V <sub>DS</sub> = 0	
I <sub>D(off)</sub>	Drain Cutoff Current		100		100		100	pA	V <sub>DS</sub> = 20V	
			200		200		200			nA
V <sub>GS(f)</sub>	Gate-Source Forward Voltage		1		1		1	V	I <sub>G</sub> = 1mA, V <sub>DS</sub> = 0	
V <sub>GS(off)</sub>	Gate-Source Cutoff Voltage	-4	-10	-2	-5	-0.5	-3		V <sub>DS</sub> = 20V, I <sub>D</sub> = 1mA	
I <sub>DSS</sub>	Saturation Drain Current (Note 1)	50	150	25	75	5	30	mA	V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0	
V <sub>DS(on)</sub>	Drain-Source ON Voltage		0.4		0.4		0.4	V	V <sub>GS</sub> = 0 I <sub>D</sub> = 3mA (4393) I <sub>D</sub> = 6mA (4392) I <sub>D</sub> = 12mA (4391)	
r <sub>DS(on)</sub>	Static Drain-Source ON Resistance		30		60		100	Ω	V <sub>GS</sub> = 0, I <sub>D</sub> = 1mA	
r <sub>ds(on)</sub>	Drain-Source ON Resistance		30		60		100		V <sub>GS</sub> = 0, I <sub>D</sub> = 0	f = 1kHz
C <sub>iss</sub>	Common-Source Input Capacitance (Note 2)		14		14		14	pF	V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0	
C <sub>rss</sub>	Common-Source Reverse Transfer Capacitance (Note 2)				3.5				V <sub>DS</sub> = 0	V <sub>GS</sub> = -5V
										V <sub>GS</sub> = -7V
			3.5						V <sub>GS</sub> = -12V	
t <sub>d</sub>	Turn-ON Delay Time (Note 2)		15		15		15	ns	V <sub>DD</sub> = 10V, V <sub>GS(on)</sub> = 0	
t <sub>r</sub>	Rise Time (Note 2)		5		5		5		I <sub>D(on)</sub> 4391 12mA 4392 6 4393 3	V <sub>GS(off)</sub> -12V -7 -5
t <sub>off</sub>	Turn-OFF Delay Time (Note 2)		20		35		50			
t <sub>f</sub>	Fall Time (Note 2)		15		20		30			

**NOTES:** 1. Pulse test required, pulse width = 300μs, duty cycle ≤3%.  
2. For design reference only, not 100% tested.

**SWITCHING TIMES TEST CIRCUIT**

