N-Channel Depletion-Mode 4-Channel DMOS FET Array

SD5501

FEATURES

- **Normally ON Configuration**
- **Low Interelectrode Capacitances**
- **High-Speed Switching**
- **Wide Dynamic Range**

APPLICATIONS

- **High-Speed Analog Switches**
- **Wide-Band Dual Differential Amplifiers**
- **Dual Cascode Amplifiers**
- **High Intercept Point Double Balanced Mixers**

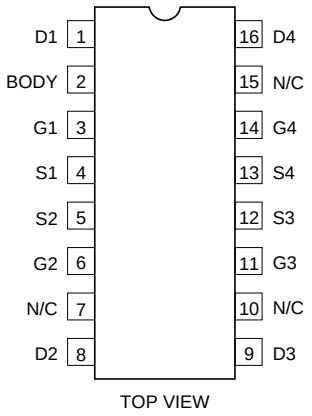
DESCRIPTION

The SD5501 is manufactured utilizing Calogic's proprietary high speed, low capacitance DMOS process featuring an N-Channel depletion-mode design. This "normally-ON" device is well suited for high speed instrumentation and communication systems where multiple channels are required for fast switching or dual amplification. Available in a 16-pin plastic dual in-line plastic package or chip form.

ORDERING INFORMATION

Part	Package	Temperature Range
SD5501N	Plastic	-55°C to +125°C
XSD5501	Sorted Chips in Carriers	-55°C to +125°C

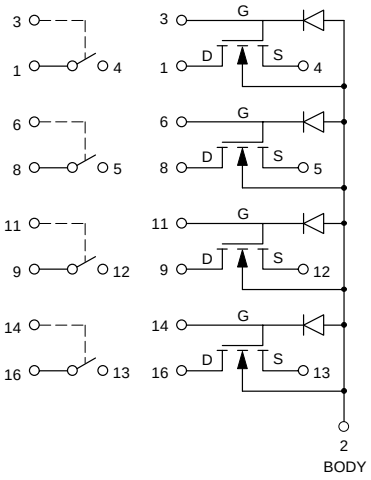
PIN CONFIGURATION



TOP VIEW

CD2

SCHEMATIC DIAGRAM



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ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

V_{DS}	Drain-Source Voltage	+30 Vdc	P_D	Total Package Power Dissipation
V_{SD}	Source-Drain Voltage	+0.5 Vdc		(at or below TA = +25°C) 640 mW
V_{DB}	Drain-Body Voltage	+30 Vdc		Linear Derating Factor 10.7 mW/°C
V_{SB}	Source-Body Voltage	+15 Vdc	P_D	Single Device Power Dissipation
V_{GS}	Gate-Source Voltage	+25 Vdc		(at or below TA = +25°C) 300 mW
V_{GB}	Gate-Body Voltage	+25 Vdc		Linear Derating Factor 5.0 mW/°C
	Gate-Body Voltage	-0.3 Vdc	T_j	Operating Junction Temperature Range -55 to +85°C
V_{GD}	Gate-Drain Voltage	+25 Vdc	T_S	Storage Temperature Range -55 to + 150°C
I_D	Continuous Drain Current	50 mA		

ELECTRICAL CHARACTERISTCIS (T_A = +25°C unless otherwise noted)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	TEST CONDITIONS	
STATIC							
B_{VDS}	Drain-Source Breakdown Voltage	20			V	I_D = 10 nA, V_{GS} = V_{BS} = -5.6V	
B_{VSD}	Source-Drain Breakdown Voltage	10				I_S = 10 nA, V_{GD} = V_{BD} = -5.6V	
B_{VDB}	Drain-Body Breakdown Voltage	25				I_D = 10nA, V_{GB} = 0, Source Open	
B_{VSB}	Source-Body Breakdown Voltage	15				I_S = 10µA, V_{GB} = 0, Drain Open	
$I_{GSS(fwd)}$	Forward Gate Leakage Current			1.0	nA	V_{GS} = 25V, V_{DS} = V_{BS} = 0	
I_G	Gate Operating Current		-3.0	-100	pA	V_{DG} = 15V, I_D = 5.0 mA, V_{BS} = -5.6V	
			-0.7	-10	nA		T_A = +125°C
$V_{GS\ (off)}$	Gate - Source Cutoff Voltage	-1.0		-5.0	V	V_{DS} = 10V, I_D = 1.0µA, V_{BS} = 5.6V	
$V_{GS\ (on)}$	Gate-Source On Voltage	-0.3		-3.0		V_{DG} = 10V, I_D = 5mA, V_{SB} = -5.6V	
I_{DSX}	Zero Gate Voltage Drain Current	7.0		40	mA	V_{DS} = 10V, V_{GS} = 0, V_{BS} = -5.6V	
		5.0					T_A = +125°C
$r_{DS\ (ON)}$	Drain-Source On Resistance		100	150	ohms	I_D = 1.0mA, V_{GS} = 0, V_{BS} = -5.6V	
DYNAMIC							
g_{fs}	Common-Source Forward Transconductance (1)	6.0	7.5	12	mS	V_{DG} = 10V I_D = 5.0mA V_{BS} = -5.6V	f = 1 KHz
g_{os}	Common-Source Output Conductance		200	350	µS		
C_{iss}	Common-Source Input Capacitance		3.5		pF		f = 1 MHz
C_{oss}	Common-Source Output Capacitance		1.2				
C_{rss}	Common-Source Reverse Transfer Capacitance		0.3				
$C_{(gs + sb)}$	Source Node Capacitance		4.5				
MATCHING							
V_{GSM}	Gate Source Voltage Match			50	mV	V_{DG} = 10V, I_D = 5.0mA, V_{BS} = -5.6V	
$r_{DS(on)}$	Drain-Source On Resistance Match			10%		I_D = 1.0 mA, V_{GS} = 0, V_{BS} = 5.6V	
I_{DXSM}	Zero Gate Voltage Drain Current Match			10%		V_{DG} = 10V, I_D = 5.0 mA, V_{BS} = -5.6V	
g_{fsm}	Transconductance Match (1), (2)			10%			f = 1 KHz

Note 1: Pulse Test, 80 sec, 1% Duty Cycle
Note 2: Match of 4 channels