N-Channel JFET Monolithic Dual

calogic CORPORATION

SST5912

FEATURES

- **High Gain . . . . . g_{fs} > 6 mS**
- **Low Leakage . . . . . I_G < 1pA typical**
- **Low Noise**
- **Surface Mount Package**

APPLICATIONS

- **Differential Wideband Amplifier**
- **VHF/UHF Amplifiers**
- **Test and Measurement**

DESCRIPTION

The SST5912 is a High Speed N-Channel Monolithic JFET pair encapsulated in a surface mount plastic SO-8 package. The device is designed for high gain (typically > 6000 mmhos), low leakage (< 1pA typically) and low noise, The SST5912 is an excellent choice for differential wideband amplifiers, VHF/UHF amplifiers and test and measurement.

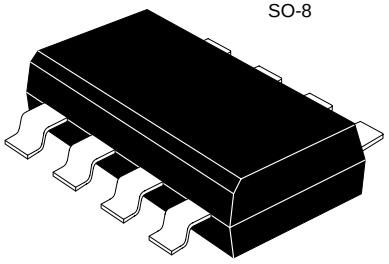
ORDERING INFORMATION

Part	Package	Temperature Range
SST5912	Plastic SO-8 Package	-55°C to +150°C

NOTE: For Sorted Chips in Carriers, See 2N5911 Series

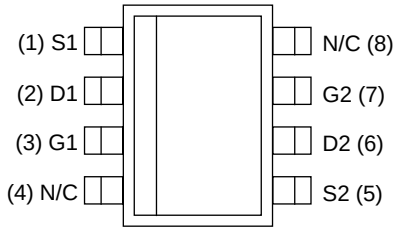
PIN CONFIGURATION

SO-8



CJ1

TOP VIEW



PRODUCT MARKING	
SST5912	SST5912

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Parameter/Test Condition	Symbol	Limit	Unit
Gate-Drain Voltage	V_{GD}	-25	V
Gate-Source Voltage	V_{GS}	-25	V
Forward Gate Current	I_G	50	mA
Power Dissipation (per side)	P_D	300	mW
(total)		500	mW
Power Derating (per side)		2.4	mW/ °C
(total)		4	mW/ °C
Operating Junction Temperature	T_J	-55 to 150	°C
Storage Temperature	T_{stg}	-65 to 150	°C
Lead Temperature (1/16" from case for 10 seconds)	T_L	300	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

SYMBOL	CHARACTERISTCS	TYP[1]	SST5912		UNIT	TEST CONDITIONS
			MIN	MAX		
STATIC						
$V_{(BR)GSS}$	Gate-Source Breakdown Voltage	-35	-25		V	I_G = -1mA, V_{DS} = 0V
$V_{GS(OFF)}$	Gate-Source Cut off Voltage	-3.5	-1	-5	V	V_{DS} = 10V, I_D = 1nA
I_{DSS}	Saturation Drain Current [2]	15	7	40	mA	V_{DS} = 10V, V_{GS} = 0V
I_{GSS}	Gate Reverse Current	-1		-100	pA	V_{GS} = -15V, V_{DS} = 0V
		-0.2			nA	T_A = 125°C
I_G	Gate Operating Current	-1		-100	pA	V_{DG} = 10V, I_D = 5mA
		-0.2			nA	T_A = 125°C
V_{GS}	Gate-Source Voltage	-1.5	-0.3	-4	V	V_{DG} = 10V, I_D = 5mA
$V_{GS(F)}$	Gate-Source Forward Voltage	0.7			V	I_G = 1mA, V_{DS} = 0V
DYNAMIC						
g_{fs}	Common-Source Forward Transconductance	6	5	10	mS	V_{DG} = 10V, I_D = 5mA f = 1kHz
g_{os}	Common-Source Output Conductance	20		100	mS	
g_{fs}	Common-Source Forward Transconductance	6	5	10	mS	V_{DG} = 10V, I_D = 5mA f = 100MHz
g_{os}	Common-Source Output Conductance	30		150	mS	
C_{iss}	Common-Source Input Capacitance	3.5		5	pF	V_{DG} = 10V, I_D = 5mA f = 1MHz
C_{rss}	Common-Source Reverse Transfer Capacitance	1		1.2		
$\overline{e}_n$	Equivalent Input Noise Voltage	4		20	nV/$\sqrt{Hz}$	V_{DG} = 10V, I_D = 5mA, f = 10kHz
NF	Noise Figure	0.1		1	dB	V_{DG} = 10V, I_D = 5mA, f = 10kHz, R_G = 100W
MATCHING						
$\lvert V_{GS1} - V_{GS2} \rvert$	Differential Gate Source Voltage	7		15	mV	V_{DG} = 10V, I_D = 5mA
$\frac{D \lvert V_{GS1} - V_{GS2} \rvert}{DT}$	Gate Source Voltage Differential Change with Temperature	10		40	mV/ °C	T = -55 to 25°C; V_{DG} = 10V, I_D = 5mA
		10		40		T = 25 to 125°C; V_{DG} = 10V, I_D = 5mA
$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio	0.98	0.95	1		V_{DS} = 10V, V_{GS} = 0V
$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio	0.98	0.95	1		V_{DG} = 10V, I_D = 5mA, f = 1kHz
$\lvert I_{G1} - I_{G2} \rvert$	Differential Gate Current	0.01		20	nA	V_{DG} = 10V, I_D = 5mA, T_A = 125°C
CMRR	Common Mode Rejection Ratio	90			dB	V_{DD} = 5 to 10V, I_D = 5mA

NOTES: 1. For design aid only, not subject to production testing.
2. Pulse test; PW = 300ms, duty cycle â 3%.