N-Channel Dual JFET

calogic
CORPORATION

U421 – U426

FEATURES

- **Ultra Low Input Bias Current . . . . . 250 Fempto Amps**
- **Low Operating Current**
- **Tight Matching Characteristics**

APPLICATIONS

- **Ultra Low Leakage FET Input Op Amps**
- **Electrometer**
- **Infrared Detectors**
- **pH Meters**

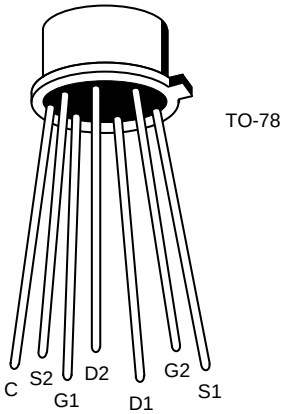
DESCRIPTION

The Calogic U421 Series are Dual N-Channel JFETs on a monolithic structure designed specifically for very high input impedance for differential amplification and impedance matching. This series features ultra low input bias current (250 fempto amps, U421) while offering high gain at low operating currents and tight matching characteristics. These devices are available in chip form for hybrid designs as well as a hermetic TO-78 package.

ORDERING INFORMATION

Part	Package	Temperature Range
U421-U426	TO-78 Hermetic Package	-55°C to +150°C
XU421-U426	Sorted Chips in Carriers	-55°C to +150°C

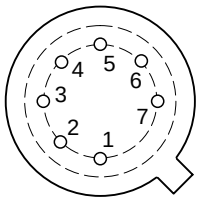
PIN CONFIGURATION



TO-78

CJ4

1 SOURCE 1
2 DRAIN 1
3 GATE 1
4 CASE/BODY
5 SOURCE 2
6 DRAIN 2
7 GATE 2



BOTTOM VIEW

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Gate-to-Gate Voltage . . . . . ±40V
Gate-Drain or Gate-Source Voltage . . . . . -40V
Gate Current 10mA
Device Dissipation (Each Side), T_A = 25°C
(Derate 3.2 mW/ °C to 150°C) 400mW
Total Device Dissipation, T_A = 25°C
(Derate 6.0 mW/ °C to 150°C) . . . . . 750 mW
Storage Temperature Range . . . . . -65°C to +150°C

ELECTRICAL CHARACTERISTICS (25°C Unless otherwise noted)

SYMBOL	CHARACTERISTIC	U421-3			U424-6			UNIT	TEST CONDITIONS	
		MIN	TYP	MAX	MIN	TYP	MAX			
STATIC										
BV_{GSS}	Gate-Source Breakdown Voltage	-40	-60		-40	-60		V	I_G = -1µA, V_{DS} = 0	
BV_{G1G2}	Gate-Gate Breakdown Voltage	±40			±40				I_G = -1µA, I_D = 0, I_S = 0	
I_{GSS}	Gate Reverse Current (1)			1.0			3.0	pA	T = +25°C	V_{GS} = -20V, V_{DS} = 0
				1.0			3.0	nA	T = +125°C	
I_G	Gate Operating Current (1)			.25			0.5	pA	T = +25°C	V_{DG} = 10V, I_D = 30µA
				.250			-500		T = +125°C	
$V_{GS\ (off)}$	Gate-Source Cutoff Voltage	-0.4		-2.0	-0.4		-2.0	V	V_{DS} = 10V, I_D = 1nA	
V_{GS}	Gate-Source Voltage			-1.8			-2.9		V_{DG} = 10V, I_D = 30µA	
I_{DSS}	Saturation Drain Current	60		1000	60		1800	µA	V_{DS} = 10V, V_{GS} = 0	
DYNAMIC										
g_{fs}	Common-Source Forward Transconductance	300		1500	300		1500		V_{DS} = 10V, V_{GS} = 0	f = 1 kHz
g_{os}	Common-Source Output Conductance			10			10			
C_{iss}	Common-Source Input Capacitance			3.0			3.0	pF		f = 1MHz
C_{rss}	Common-Source Reverse Transfer Capacitance			1.5			1.5			
g_{fs}	Common-Source Forward Transconductance	120		350	120		350		V_{DG} = 10V, I_D = 30µA	f = 1kHz
g_{os}	Common-Source Output Conductance			3.0			3.0			
$\bar{e}_n$	Equivalent Short Circuit Input		20	70		20	70	nV/√Hz		f = 10Hz
			10			10				f = 1kHz
NF	Noise Figure			1.0			1.0	dB		f = 10 Hz R_G = 10 MΩ

SYMBOL	CHARACTERISTIC	U421,4			U422,5			U423,6			UNIT	TEST CONDITIONS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
MATCH												
$\lvert V_{GS1}-V_{GS2} \rvert$	Differential Gate-Source Voltage			10			15			25	mV	V_{DG} = 10V, I_D = 30µA
$\frac{\lvert V_{GS1}-V_{GS2} \rvert}{\Delta T}$	Differential Gate-Source Voltage Change with Temperature (2)			10			25			40	V/ °C	V_{DG} = 10V, I_D = 30µA, T_A = -55°C, T_B = 25°C, T_C = 125°C
C_{MRR}	Common Mode Rejection Ratio (3)	90	95		80	90		80	90		dB	I_D = 30µA, V_{DG} = 10 to 20 V

NOTES:
1. Approximately doubles for every 10°C increase in T_A.
2. Measured at endpoints T_A, T_B and T_C.
3. $CMRR = 20\log_{10}\left[\frac{V_{DD}}{V_{GS1}-V_{GS2}}\right]$ V_{DD} = 10V.
4. Case lead not connected.