ESD Protection Arrays, Chip Scale Package

Features

- 4, 8, or 16 transient voltage suppressors in a single package
- In-system Electrostatic Discharge (ESD) protection to 18kV contact discharge per IEC 61000-4-2 international standard
- Compact Chip Scale Package (0.65mm pitch) format saves board space and eases layout in space critical applications compared to discrete solutions and traditional wire bonded packages

Applications

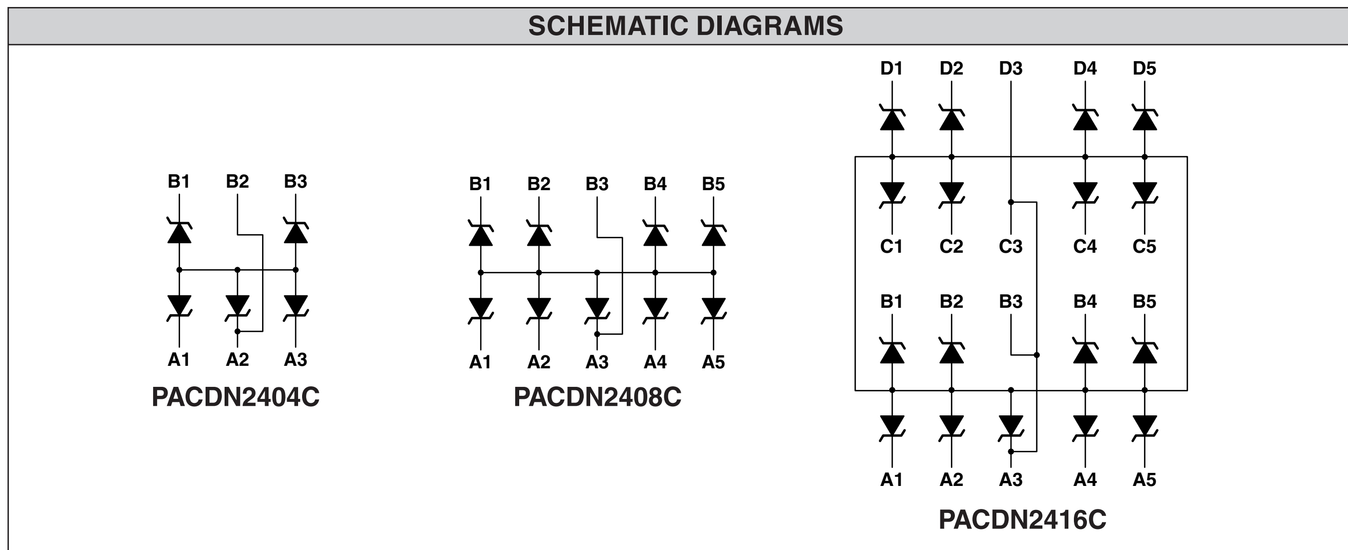
- ESD protection of I/O port connections, such as cellular phone, PDA, internet appliance and PC ports
- Protection of interface ports or IC pins which are exposed to high levels of ESD
- ESD protection of analog video and audio R, L, V (right, left, video) ports

Product Description

The PACDN2404C, PACDN2408C and PACDN2416C are transient voltage suppressor arrays that provide a very high level of protection for sensitive electronic components that may be subjected to ESD. The back-to-back zener connections provide ESD protection in cases where nodes with AC signals are present.

These devices are designed and characterized to safely dissipate ESD strikes at levels well beyond the maximum requirements set forth in the IEC 61000-4-2 international standard (Level 4, 8kV contact discharge). All I/Os are rated at 18kV using the IEC 61000-4-2 contact discharge method. Using the MIL-STD-883D (Method 3015) specification for Human Body Model (HBM) ESD, all pins are protected for contact discharges to greater than 30kV.

The Chip Scale Package format of these devices enable extremely small footprints that are necessary in portable electronics such as cellular phones, PDAs, internet appliances and PCs. The large solder bumps allow for standard attachment to laminate boards without the use of underfill.



STANDARD PART ORDERING INFORMATION		
Package		Ordering Part Number
Style	Bumps	Tape & Reel
Chip Scale	6	PACDN2404C/R
Chip Scale	10	PACDN2408C/R
Chip Scale	20	PACDN2416C/R

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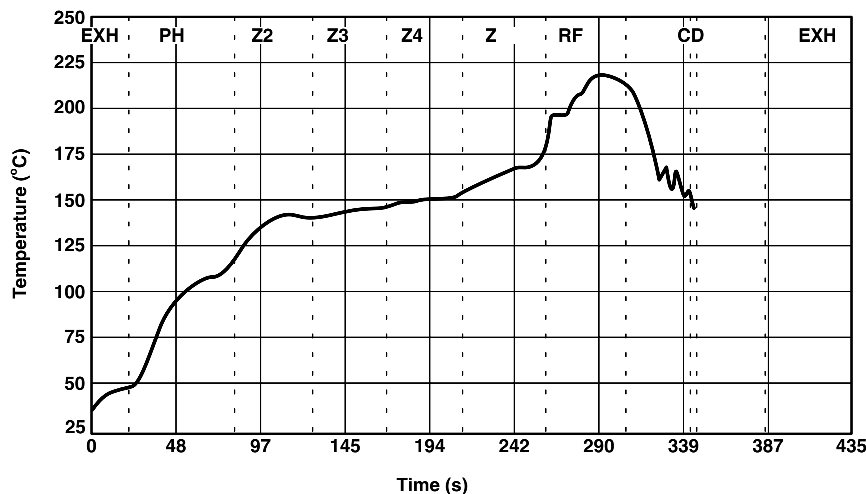
SPECIFICATIONS (At 25°C unless specified otherwise)				
	Min	Typ	Max	Unit
Reverse Stand-off Voltage, I = 10µA	±5.9			V
Signal Clamp Voltage:				
Positive Clamp, 10mA	6.0	7.6	9.2	V
Negative Clamp, 10mA	−9.2	−7.6	−6.0	V
In-system ESD withstand voltage*:				
Human Body Model (MIL-STD-883D, method 3015)		±30		kV
IEC 61000-4-2, contact discharge method		±18		kV
Clamping voltage during ESD discharge Positive		14		V
MIL-STD-883D (Method 3015), 8kV Negative		−14		V
Capacitance at 2.5V dc, 1MHz		39		pF
Temperature Range:				
Operating	−40		85	°C
Storage	−65		150	

* ESD applied between channel pin and ground, one at a time. All other channels are open. This parameter is guaranteed by design and characterization

PRINTED CIRCUIT BOARD RECOMMENDATIONS	
Pad Size on PCB	0.300mm
Pad Shape	Round
Pad Definition	Non Solder Mask Defined Pads (NSMD)
Solder Mask Opening	0.350mm
Solder Stencil Thickness	0.152mm
Solder Stencil Aperture Opening	0.360mm (sq.)
Solder Flux Ratio	50/50
Solder Paste	No Clean
Bond Trace Finish	OSP (Entek Cu Plus 106A)



Typical Solder Reflow Thermal Profile (No Clean Flux)

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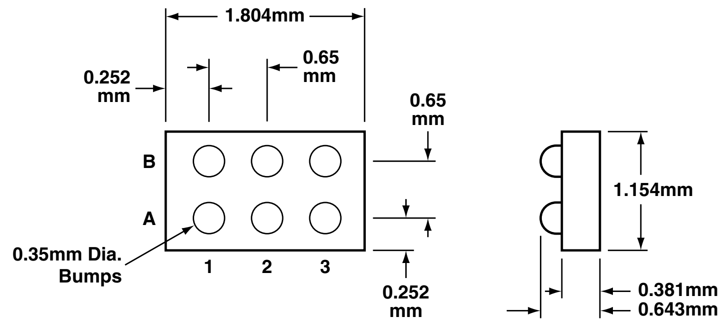
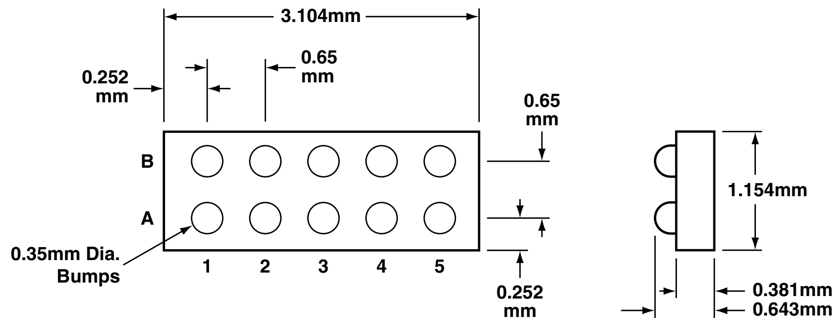
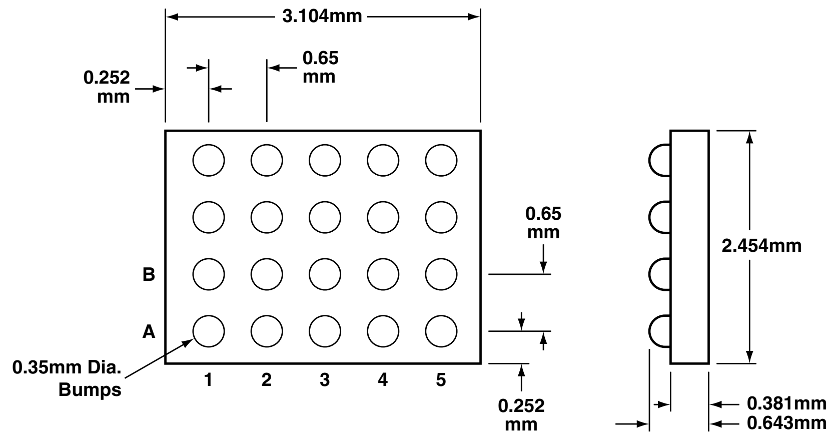
Package Diagrams



PACDN2404C



PACDN2408C



PACDN2416C

Pin Orientation

Components are symmetrical, and do not require orientation to pin-1 found in conventional semiconductors. The part may be rotated 180° without affecting operation.

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