

# CEP4050A/CEB4050A

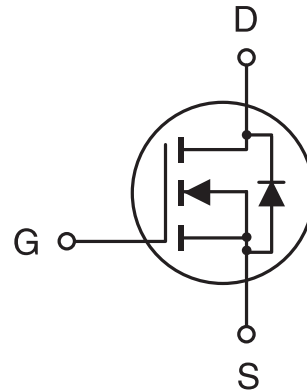
March 1998

## N-Channel Enhancement Mode Field Transistor

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### FEATURES

- 55V , 15A ,  $R_{DS(ON)}=85m\Omega$  @  $V_{GS}=10V$
- Super high dense cell design for extremely low  $R_{DS(ON)}$ .
- High power and current handling capability.
- TO-220 & TO-263 package.



### ABSOLUTE MAXIMUM RATINGS (Tc=25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V <sub>DS</sub>	55	V
Gate-Source Voltage	V <sub>GS</sub>	±20	V
Drain Current-Continuous -Pulsed	I <sub>D</sub>	15	A
	I <sub>DM</sub>	45	A
Drain-Source Diode Forward Current	I <sub>S</sub>	15	A
Maximum Power Dissipation @ T <sub>c</sub> =25°C Derate above 25°C	P <sub>D</sub>	50	W
		0.35	W/°C
Operating and Storage Temperature Range	T <sub>J</sub> , T <sub>STG</sub>	-65 to 175	°C

### THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Case	R <sub>θJC</sub>	3	°C/W
Thermal Resistance, Junction-to-Ambient	R <sub>θJA</sub>	62.5	°C/W

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## ELECTRICAL CHARACTERISTICS (Tc=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	55			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =55V, V <sub>GS</sub> =0V			25	μA
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V			±100	nA
<b>ON CHARACTERISTICS<sup>a</sup></b>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	2	2.8	4	V
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =7.5A		66	85	mΩ
On-State Drain Current	I <sub>D(ON)</sub>	V <sub>GS</sub> =10V, V <sub>DS</sub> =10V	15			A
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> =10V, I <sub>D</sub> =7.5A		6		S
<b>DYNAMIC CHARACTERISTICS<sup>b</sup></b>						
Input Capacitance	C <sub>ISS</sub>	V <sub>DS</sub> =25V, V <sub>GS</sub> =0V f=1.0MHz		292	400	pF
Output Capacitance	C <sub>OSS</sub>			130	200	pF
Reverse Transfer Capacitance	C <sub>RSS</sub>			36	50	pF
<b>SWITCHING CHARACTERISTICS<sup>b</sup></b>						
Turn-On Delay Time	t <sub>D(ON)</sub>	V <sub>DD</sub> =30V, I <sub>D</sub> =15A, V <sub>GS</sub> =10V, V <sub>GEN</sub> =25Ω		7	20	ns
Rise Time	t <sub>r</sub>			65	100	ns
Turn-Off Delay Time	t <sub>D(OFF)</sub>			15	30	ns
Fall Time	t <sub>f</sub>			35	50	ns
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =48V, I <sub>D</sub> =15A, V <sub>GS</sub> =10V		13	17	nC
Gate-Source Charge	Q <sub>gs</sub>			3		nC
Gate-Drain Charge	Q <sub>gd</sub>			7		nC

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Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>DRAIN-SOURCE DIODE CHARACTERISTICS<sup>b</sup></b>						
Diode Forward Voltage	$V_{SD}$	$V_{GS} = 0V, I_s = 7.5A$		0.8	1.3	V

### Notes

- a. Pulse Test: Pulse Width  $\leq 300 \mu s$ , Duty Cycle  $\leq 2\%$ .
- b. Guaranteed by design, not subject to production testing.

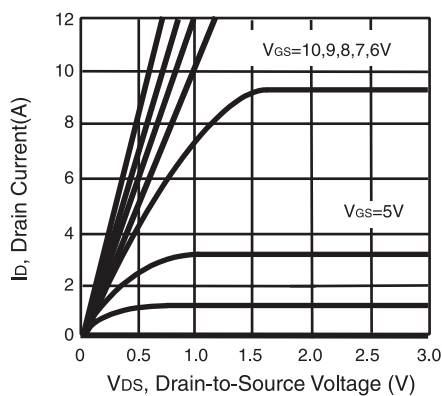


Figure 1. Output Characteristics

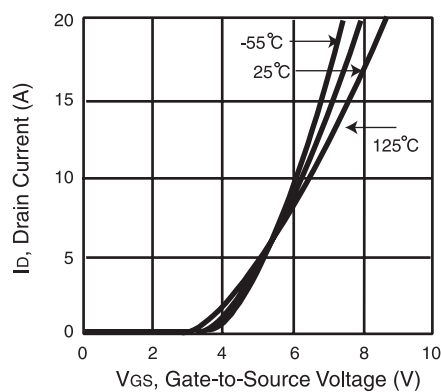


Figure 2. Transfer Characteristics

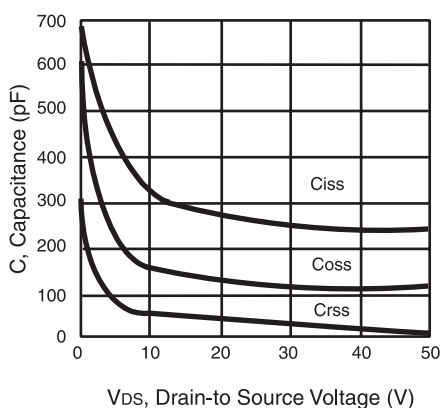


Figure 3. Capacitance

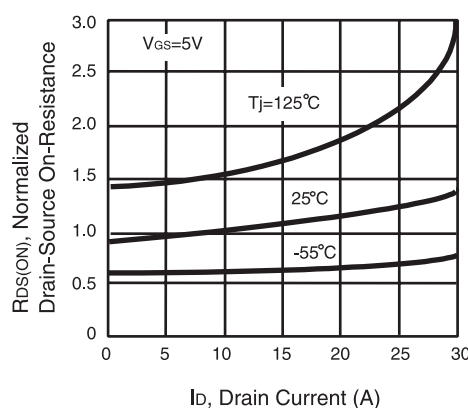
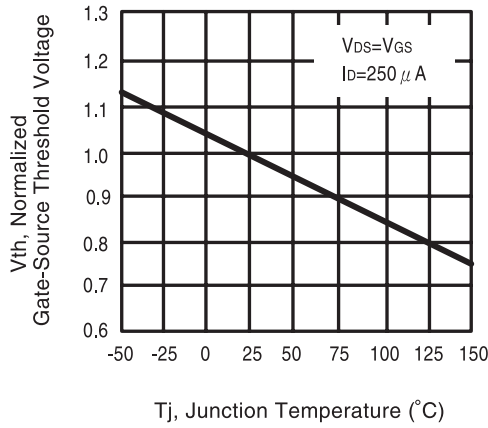


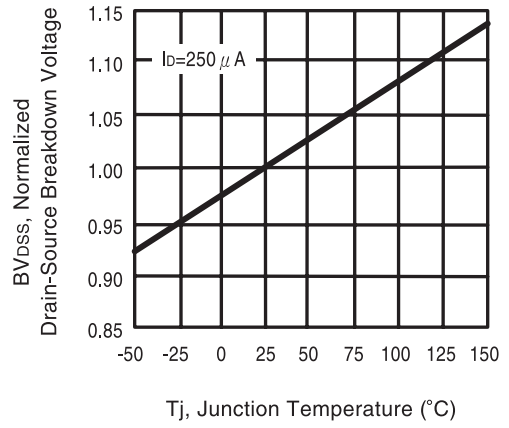
Figure 4. On-Resistance Variation with Drain Current and Temperature

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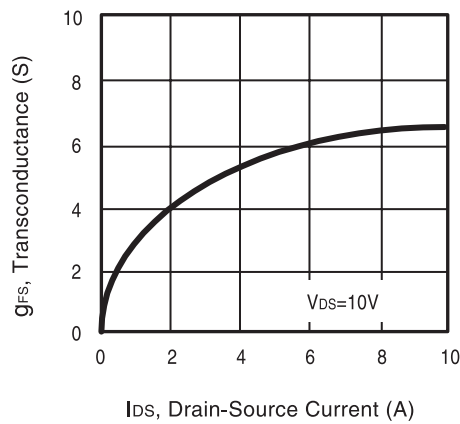
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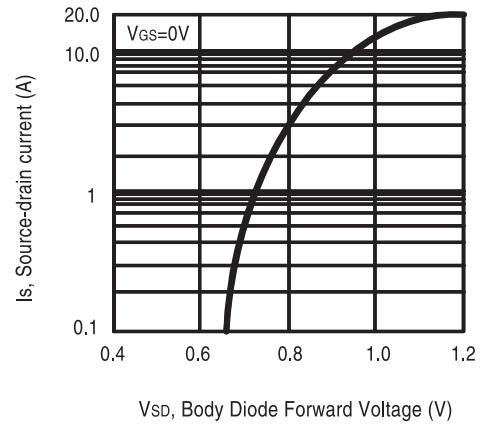
**Figure 5. Gate Threshold Variation with Temperature**



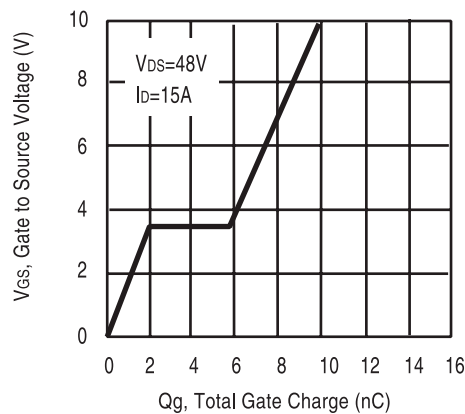
**Figure 6. Breakdown Voltage Variation with Temperature**



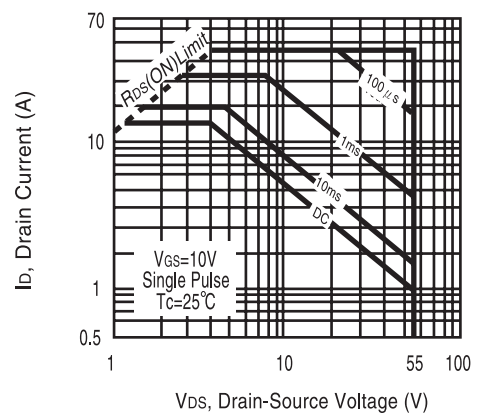
**Figure 7. Transconductance Variation with Drain Current**



**Figure 8. Body Diode Forward Voltage Variation with Source Current**



**Figure 9. Gate Charge**



**Figure 10. Maximum Safe Operating Area**

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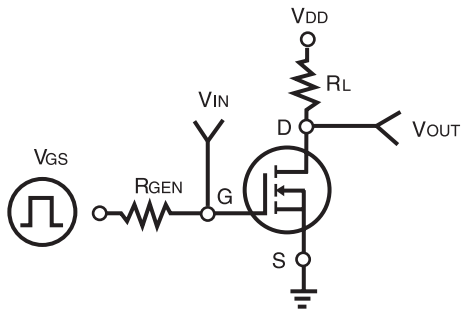


Figure 11. Switching Test Circuit

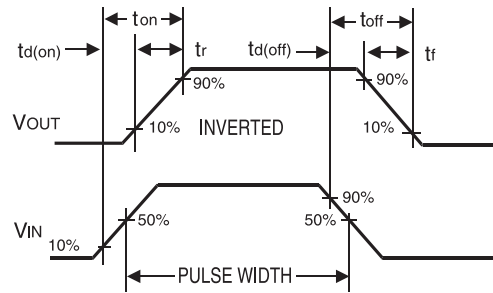


Figure 12. Switching Waveforms

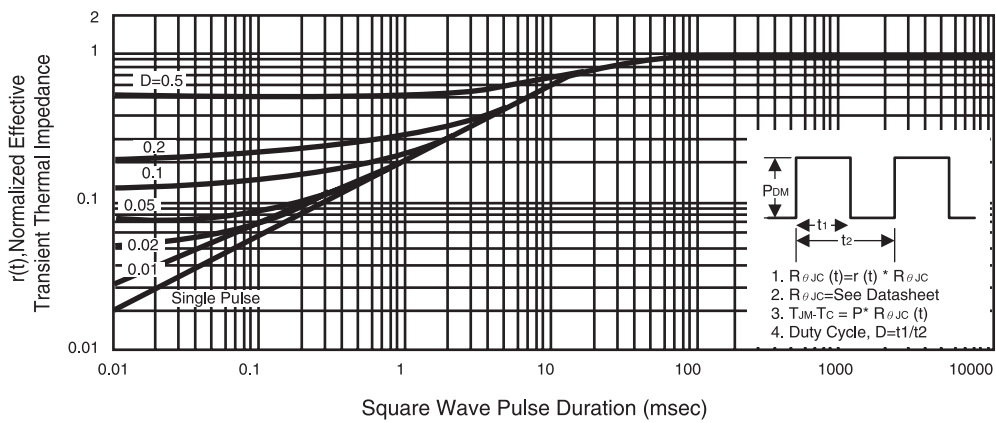


Figure 13. Normalized Thermal Transient Impedance Curve